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PbS Colloidal Quantum Dot Light Emitting Field-Effect Transistors

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Abstract

This research is dedicated to Light Emitting Transistors made with PbS quantum dots as active layer. PbS quantum dots with Oleic Acid as ligands were spin coated on a bottom gate bottom contact Si/SiO_2 substrate.

After deposition of a monolayer of QDs the Oleic Acid have been replaced by shorter and bi-functional molecules ethane dithiol. Afther ligand exchange the layer became conductive.

Electroluminescence has been detected clearly dependent on the drain current have been detected. This follows the expectation, since this dependence has been shown in organic light emitting transistors. However, no gate voltage dependence could be detected.

A huge redshift between photoluminescence on glass substrates and electroluminescence on silicon substrates was detected. This is probably due to different sintering rates caused by different heat conductions. It can be concluded that QD field-effect light emitting devices are promising but further investigation should be performed. The most important next step could be to prove gate voltage dependency and measure EQE, but also different device structures have to be investigated.

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1 Introduction

Quantum dots are semiconducting materials of Bohr radius dimensions. These particles have attained a lot of interest due to their size-dependent band gap. With the size of the particle the absorption and emission wavelength can be tuned and therefore the synthesis of these particles is more important than the semiconductor choice itself. They can therefore be used for multiple types of devices working on different wavelengths. Moreover, quantum dots can be solution processed due to the ligands on their surface.

If semiconductors of PbS are used, QDs active in the NIR can be obtained. NIR light emmission is widely used in many applications including optical data communication, night vision, touchscreen technology and biomedical imaging. However near-infrared (NIR) light is difficult to produce both with organic and inorganic materials [1]. This is due to low quantum yield in the NIR with respect to the visible spectrum of these materials. Very high photoluminescence quantum yield of 80% between 1100nm and 1300nm has been reported for PbS quantum dot, with a very narrow size distribution. Other quantum dot materials are less promising due to big size dispersion (PbTe)[2] and different band gap range (PbSe)[3].

PbS QD NIR LEDs have been reported with electroluminescent efficiencies comparable to state-of-the-art commercial direct-gap semiconductor LEDs. The latter are fabricated using planar epitaxy and are thus fairly hard to make. The devices could still be improved providing an alternative to current semiconductor devices. [4].

Field-Effect Transistors (FET) are not only the backbone of modern electronics, but because of the importance of electronics, they are also the backbone of our entire society. Today, it is very hard to imagine a world without transistors. Since Moore predicted his law in 1965, the number of transistors per unit area is doubled every 1,5 year. Because the production of Silicon transistors is almost at the edge of what is physically possible, quantum dot transistors are investigated as possibility for low cost applications. Work has been done on PbS ambipolar transistors to increase the on/off ratio and mobility of both charge carriers. However these transistors are not yet sufficient for applications in electronics, it is very likely that these properties will improve in the near future [5].

Even more, it would be very nice if the optical properties of the quantum dot LED could be used together with the switching opportunities FETs have. Therefore, Quantum Dot Light Emitting FETs (QD-LET) are investigated in this research. These devices have never been reported before. However, due to the ambipolar characteristics it is very likely that they will be able to combine properties of LEDs and FETs.

Examples of LETs that already have been reported are[6]:

Si Nanocrystals & InGaP/GaAs heterojunction Silicon nanocrystals are kept in the gate oxide of the FET. With both the nanocrystals and heterojunction the electroluminescence was reported with an alternating electric field applied to the gate. Besides the non-continuous light emission, the production of these devices is rather complicated and only a specific class of crystalline substrates can be used.

Carbon nanotubes Carbon nanotubes have the same size-dependent properties as quantum dots have, but also these devices are not easily produced.

Organics The most promising LETs are made of organic crystals or twin films. However, the organics used for these devices mainly have an emitting wavelength in the visible range.

In OLETs a couple of advantages have been reported with respect to LEDs using the same organic crystals. This includes the tunable emission-zone position by changing the gate voltage. This is very useful since exciton quenching mainly occurs at the electrodes, so moving the emission towards the centre of the channel can vastly improve the emission. Also the planar structure of LETs is advantegeous since the emitted light is not being reflected by a contact layer. The light intensity is proportional to the drain current since the probability of recombination is very high. [7][8].

2 Theory

2.1 Colloidal Quantum Dots

Nanocrystals are nanometer size single crystals of very small semiconducting materials. Due to their small dimensions, the energy levels are discrete. This property originates from quantum confinement of the electronic wavefunctions. The electronic configuration of the NCs is similar to that of atoms and molecules. Quantum Dots are confined in three dimensions and therefore seen as a 0D object. Other nanocrystals include nanowires (two confined dimensions, 1 Dimensional) and nanosheets (1 confined dimensions, 2 dimensional). This quantum confinement can be described with the standard particle in a box approximation. Bulk semiconductor has band like transport with a fixed band gap. In contrast, the colloidal quantum dot band gap can be altered by changing the size of the particles. The smaller the nanocrystals are, the more blueshifted the spectrum is as shown in figure 1. [9]

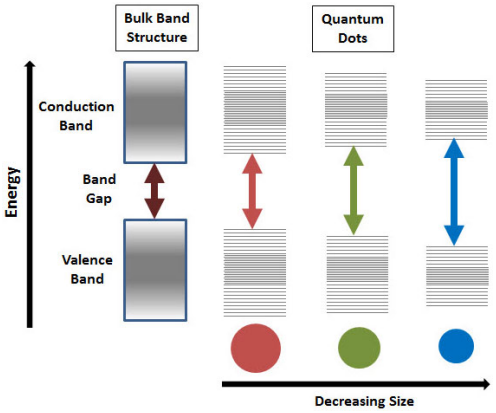

Figure 1: Quantum confinement effect in QDs. Smaller particals have bigger band gaps. (Sigma Aldrich)

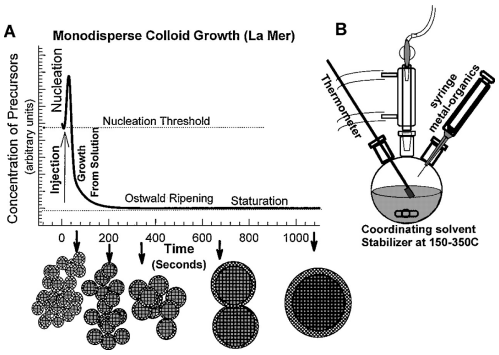

Figure 2: Schematized synthesis process [10]

Another big advantage of QDs is the cheap way they can be produced. Nowadays, QDs can be synthesised monodisperse in size and shape [10]. QDs are synthesised by the 'hot injection technique' as shown in figure 2. The lead and sulphur containing precursors are quickly put in a hot stirring solvent. The temperature must be lowered in order to separate the nucleation event and the nuclei growth. In this case the size distribution becomes very narrow [11]. The next step is to let the crystals grow where small crystals dissolve and redeposit on larger crystals, which is called Ostwald ripening. Oleic acid (OA, figure 3) is used as a surfactant to tune the nucleation and growth.

2.2 Quantum Dot Films

OA ensures solubility of QDs and colloidal stability. However, OA is a non-conductive molecule that acts as a very good (dielectric) insulator. Despite the high conductivity

of bulk PbS, the conductivity of a OA-capped PbS QD layer is strongly suppressed. In bulk material the carrier mobility is mostly affected by acoustic phonons and ionised impurities because these phenomena scatter the carriers in different directions [12]. Electrons need to tunnel between different QD when the QDs are deposited on a substrate. When two QDs are close to each other, their quantum confined wave functions combine and create a 'molecular orbital'. The coupling energy can be expressed as [11]

$$\beta \approx h \cdot e^{-2\Delta x\sqrt{\frac{2m^*\Delta E}{\hbar^2}}} \tag{1}$$

where m^* is the effective mass, ΔE and Δx are respectively the height of the tunnelling barrier and the shortest edge to edge distance between NCs. For good carrier transport between NCs a higher mobility, one of the latter two should be decreased.

The Δx can be decreased by replacing the OA by another ligand. Multiple options are possible, ranging from just shorter chain molecules that have only one bonding site till molecules that have two sides that can chemically bond to the surface of neighbouring QDs and can therefore cross-link PbS particles. In this case EDT is used (figure 4). Since these ligands have a bigger affinity to the QDs than OA has, the ligands just have to be deposited on the QD film. When ligands with two active sides are used, the QD will form a superlattice because the QDs are cross-linked trough the entire film.

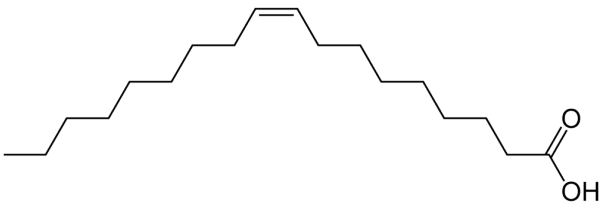

Figure 3: Oleic Acid

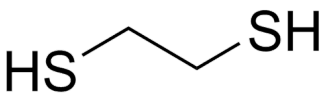

Figure 4: Ethane Dithiol

Also, coulomb blockade can play a role[11]. To charge a quantum dot with an extra electron, the energy should be higher than the coulomb energy which is

$$E_c = \frac{e^2}{4\pi\epsilon_m\epsilon_0 r} \tag{2}$$

When this is not the case, the resistivity increases to infinity and adding an electron is thus not possible. Since an electron moves from one QD to another, this barrier should be overcome twice, see figure 5. The coulomb blockade therefore has a negative effect on the current under all circumstances.

Besides the coupling and coulomb energy, there are other physical phenomena that can effect the transport in QD films[11]. The first originates from the dispersion of the QD size and shape. Since the QDs are very small, even one atomic layer is enough to change the energies sufficiently to stop resonant tunnelling. When resonant tunnelling is not possible, phonons are needed for the transition. From this, one can understand why the monodispersity is a very important property of QDs for electronic devices.

Second, it is nearly impossible to create a film which is completely well-ordered. Due to this, the spacing between different QDs is not constant. The fourth problem

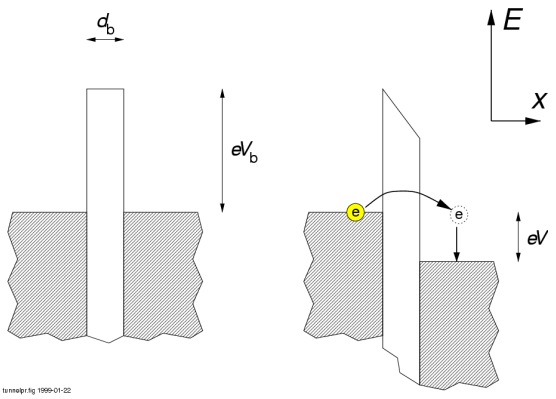

Figure 5: Schematic representation of the coulomb energy [13]

is the existence of interface traps, which are defects that give rise to some energy states within the band gap. These traps could be introduced in all stages of the device fabrication.

2.3 Field-Effect Transistor

A Field Effect Transistor (FET) is a device with three electrodes: drain, source and gate. There is a channel between the drain and source electrodes. The conductances can be tuned by the gate voltage. The transistor that has been used in this research has the same working principle as the MISFET (Metal Insulator Semiconductor FET). A dielectric insulator is placed between the quantum dot solid channel and the gate. Due to this insulator, (ideally) no current flows between the gate and contacts. When a gate voltage is applied, the insulator will be polarised inducing the change of the charge carrier concentration. For positive or negative gate voltages electrons and holes are induced respectively. The source and drain are named in this way because the electrons are injected at the source and extracted at the drain. However in the case of ambipolar transistors both charge carriers can be injected.

Due to the traps not every induced charge is mobile. These traps first have to be filled before charges can contribute to the current. The gate voltage where the charges are becoming mobile is called the threshold voltage (Vth). Donor and acceptor states and interface dipoles can cause changes in the channel without applying a gate voltage. This is the so called built-in channel.

2.4 Channel geometry

In figure 6a the standard operation mode for an applied gate voltage with a small voltage between the source and drain (Vds). The transistor is said to work in the linear regime and the drain current is directly proportional to Vds. When Vds becomes as big as the effective gate voltage, which is Vg-Vth, the channel is 'pinched off' as shown

in figure 6b. If Vds is even further increased, a depletion region is formed because the local voltage is below the effective gate voltage. In this case the drain current is not related to the drain voltage anymore, because the potential drop between the pinch-off point and the source electrode stays constant. The current is therefore called saturated as shown in figure 6c [14]. If the drain current is increased even more, the other charge carrier is also accumulated, see figure 6d. This leads to a higher drain current, which is the sum of both charge carrier types.

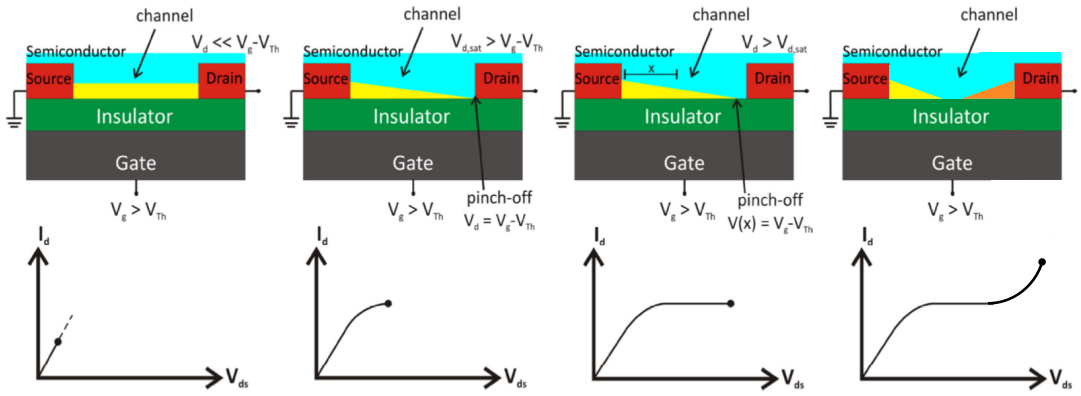

Figure 6: FET working principle with corresponding output characteristics. a) linear regime, b) pinch-off voltage, c) saturation regime, d) inversion regime ([7], modified)

2.5 Characterisation

Two types of measurements are performed to determine the FET. The first one is the transfer curve, the relation between the drain current and gate voltage. The other one is the output curve, which is the relation between drain current and drain voltage for different gate voltages. From these the most important features are the on/off ratio, threshold voltage of both charge carriers and the carrier mobilities which can be calculated. These measurements are needed to check the performance of the transistors and if they are ambipolar. The mobility in the linear regime can be calculated using the following equation [12]

$$\mu_{lin} = \frac{L_c}{W_c V_{ds} C} \cdot \frac{\delta Id}{\delta Vg} \tag{3}$$

Where L_c and W_c are respectively the channel length and the channel width and C is the capacitance. The channel length is defined as the distance between source and drain electrodes, the width is the other in-plane dimension.

2.6 Ambipolarity

Collodial quantum dots can be used for both n- and p- type transistors. Therefore, it is also possible to create one transistor which can operate in both regimes. However,

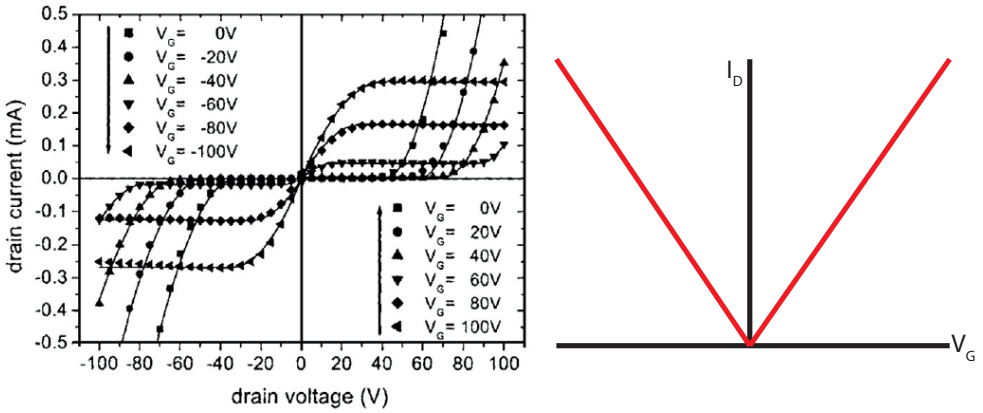

Figure 7: Ideal Ambipolar characteristics [15]

when the difference between the Fermi levels of the QD solid and electrode is too big or there are to many trap states for one charge carrier, the threshold gate voltage can become high. In this case, it is not possible to fulfil the strong inversion condition for the minority carrier and the device is thus a unipolar transistor. There are three requirements that should be fulfilled in order to make ambipolarity possible. First, the semiconducting layer should allow electron and holes to be mobile. Second, the electrodes needs to be capable to inject holes and electrons in the semiconductor film. Third, the semiconductor/ dielectric interface should have little carrier traps for both charge carriers [7]. The perfect characteristics for an ambipolar transistor are shown in figure 7.

In the ambipolar regime the transistor can be seen as a p-i-n junction. Different charge carriers are accumulated at both sides of the transistors , which represent the p and n type semiconductors. In between there is an area where the effective gate voltage is 0V. There is no charge accumulation is this region and therefore this region acts as an insulator.

2.7 Luminescence & Recombination

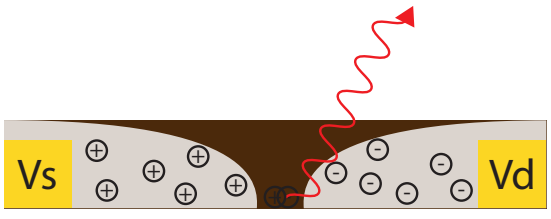

Figure 8: Accumulated carrier density in the active layer. Diffusion leads to recombination in the central region.

Light emission is called luminescence. This emission follows from an excited electron which recombines with a hole. In the case of photoluminescence (PL), this electron

is excited by a photon, as the name suggests. Another type of luminescence is electroluminescence (EL). EL is a current stimulated process and is the base of the LET. In a LET, both charge carriers accumulate in the inversion regime (figure 6d), which diffuse to the other side of the transistor. Between the electron and hole accumulation region, the charge carriers can meet each other and recombine here, producing a photon, see image 8. This light emission intensity depends on the current density. The current density mainly depends on the carrier mobilities and the ability of the semiconductor to produce excitons and therefore photons.

For perfect ambipolar transistors, one would expect that the light intensity is linearly dependent on the drain current. Even for ambipolar transistors with different mobilities for electrons and holes, it is not possible for a charge carrier to move trough an accumulation layer of the opposite charge carrier without recombining since the recombination probability is very high. However, according to Zaumseil [8], the light intensity is not linearly dependent on the drain current in the proximity of the electrode in Organic Single Crystal LETs (OSCLETs). Two possible explanations are given. Excitons could be quenched by the electrode leading to a non-radiative loss of energy. Also, the charge carriers could move to the electrode before recombining since the recombination area is very small. In these cases the drain current will be higher without having more light. Since the accumulation layers of both charge carriers can be altered by changing the gate voltage and drain-source voltage, it is thus possible to move the recombination zone away from the electrodes. However, also the large electric field in the channel and defects at the interface between the dielectric and active layer could quench excitons.

According to Bisri [7], in OSCLETs the width of the recombination zone doesn't depend on the bias voltage or on the position of the recombination zone. This suggests that the pn-junction model could not be used to describe the behaviour in an ambipolar LET. The width is controlled by the intrinsic semiconductor region between the hole and electron accumulation zones. Therefore, the LET can better be seen as a p-i-n junction. The relationship between the width of the undoped region (recombination zone) and the applied voltage when $W/L_a > 2$ is then

$$V = \frac{2kT\mu_p\mu_n}{q(\mu_p + \mu_n)^2} exp(W/2L_a) \tag{4}$$

and

$$V_{undoped} = |V_{Th,h}| + |V_{Th,e}| \tag{5}$$

Where $V_{th,h/e}$ are the threshold voltages for respectively holes and electrons. Which thus lead to the conclusion that the emission zone size (the undoped region in the pin-model) should be proportional to the sum of the threshold voltages. Also, in OSCLETs it is investigated that the material size influences the width of the recombination zone less than the device characteristics.

2.8 Dielectric

Different dielectrics can be used for FETs. The most common one is SiO2 thermally grown on Si. However, for measurement reasons a transparent device is more useful for

light emitting transistors. To create a good inversion layer channel, the capacitance should be high enough.

$$C = K \cdot \epsilon_0 \cdot \frac{A}{d} \tag{6}$$

shows the capacity for a parallel plate capacitor where K is the dielectric constant and ϵ_0 the permittivity of vacuum . A high-K gate dielectric has the advantage that it can be operated at low voltages which is very usefull for commercial application. Moreover, since commercial transistors are very small nowadays, the dielectric is becoming too thin. With a higher K the layer can be can be thicker without having a bigger capacitance. With a thicker layer, problems arising from defects in the layer become less influencing.

A couple of other properties are important in order to have a good dielectric. The interface between the gate metal and active layer must be good. Therefore a low surface roughness and surface traps density is needed. When a polymer is used, this must also be soluble in a solvent that is not damaging the active layer [16]. Polymer dielectrics can be easily processed and flexible. Some polymers also show ferroelectric behavior, which leads to a very big hysteresis due to the dipolar polarisation [15].

An important thing to consider is the effects of energetic carriers at high applied biases. When the bias is too big, some tunnelling current will flow throught the film, creating defects in the dielectric film. When there are too many defects, a chain could be formed leading to a breakdown current as shown in image 9. This leads to a leakage of the gate dielectric[12].

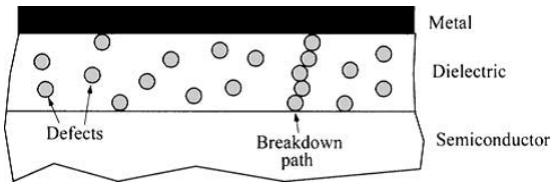

Figure 9: Breakdown path [12]

3 Experimental Setup

3.1 Device Structure

Two different substrates have been used. Silicon is smooth, flat, strong and relatively cheap since it is a widely used material in electronic circuits [17]. Moreover, it is very easy to grow a flat, uniform and high quality dielectric oxide layer on it. Also glass is used since a transparent device has advantages when measuring EL. The first substrate we used has a bottom gate bottom contact structure while the latter has a top gate bottom contact structure (figure 10c).

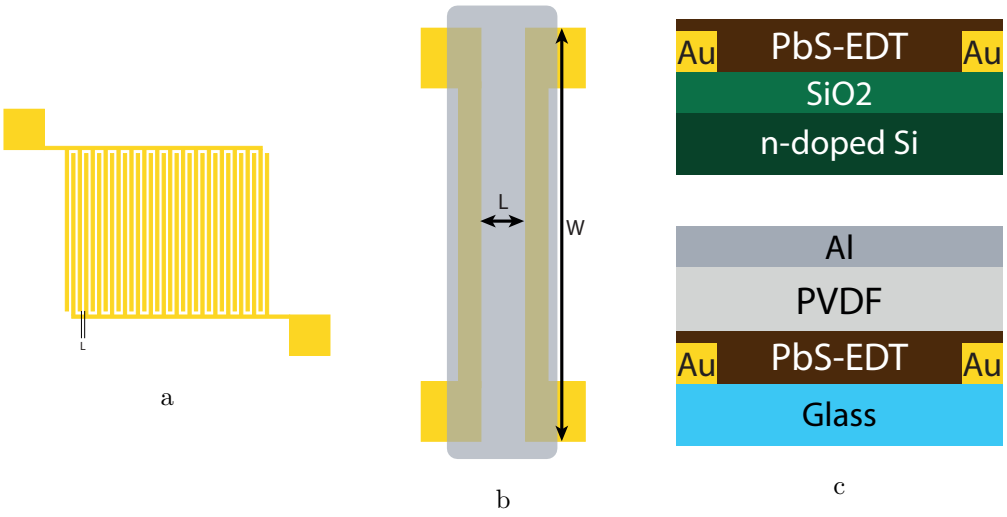

Figure 10: a) electrode lay-out on silicon substrate, b) electrode lay-out on glass substrate, c) side view of the transistors

3.1.1 Silicon

A heavily n-doped Silicon substrate is put in an oven at 900-1200 °C to thermally grow a 230 nm thick SiO_2 dielectric insulating layer. Since it is relatively easy to purify the silicon, the dielectric layer is of very high quality. The relative dielectric constant (K) is 3.9. On top of the dielectric layer, lithography is used to create interdigitated gold electrodes, see figure 10a. These interdigitated electrodes have a channel width of 10 mm, there are 16 devices on one substrate with channel lengths of 2.5 μm, 5 μm, 10 μm and 20 μm. The electrodes are 50 nm thick and are composed by about 5 nm ITO and 45 nm Au. Since the active layer is put on top of this device, the device structure is bottom gate bottom contact.

3.1.2 Glass

For the glass substrate the top gate bottom contact structure has been used. First, gold electrodes are deposited with an evaporator creating 3 channels. The pressure in this evaporator was 10^{-8} mbar. Then, a current is applied to a boat containing gold

droplets. The gold evaporates into a 100 nm thick gold electrode. A shadow mask is used to cover the places where the electrodes should not be deposited. Because of the resolution of this technique, the channel lengths are 100 μm, 200 μm and 300 μm. See figure 10b.

Afterwards, the active- and dielectric layers are deposited on the substrate by a spin coater. They have respectively a thickness of around 65 nm and 300 nm. At last, an 100 nm thick aluminium gate contact is deposited by evaporation.

3.2 Substrate Cleaning

Since glass isn't crystalline but amorphous, there are peaks on the surface which could influence the formation of the gold electrode and the deposition of the active layer. Therefore, the glass is scrubbed by a rubber glove with soapy water first. In figure 11 AFM pictures of microscope object carrier glass and polished glass are shown. It is clear that the polished glass is very flat and thus could better be used for device fabrication than the microscope-glass. The polished glass is cleaned as described before and afterwards the glass substrates are rinsed with type II water and placed on a holder, inside a bottle filled with milli-Q water. This bottle is placed inside a sonicator for 10 minutes. For SiO_2 the first step is to remove the residue of the photoresist with

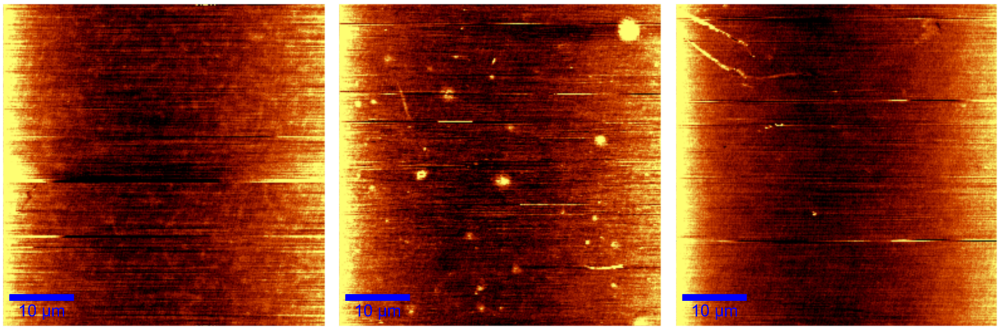

Figure 11: Left to right: polished glass, microscope glass and 5 minutes scrubbed microscope glass

a sonication for 10 minutes in acetone. After drying with a nitrogen gun an oxygen plasma cleaning step is performed. This plasma includes ions which break most organic residues which vapours are extracted by a vacuum pump.

Then, for both substrates the cleaning process of drying and sonication is done twice with acetone and isopropanol. At last, the substrates are baked in an 120°C oven for one hour.

3.3 Spin coating

3.3.1 PbS layer

As written in the theory part, the QDs are capped by OA which need to be displaced by smaller molecules. In this case, ethanedithiol (EDT) is used. When a thick layer of QDs is deposited on a substrate followed by ligand exchange with EDT, cracks appear

in the film due to settling. Therefore, the film is made by sequentially depositing nanocrystals and the new ligands. This is done with a spin coater in a N_2 filled glove box.

The spin coating process starts with covering the complete substrate with the solution. The substrate is rotated to get rid of the excess solution by centrifugal forces. Several settings influence the thickness and structure of the deposited film. These include rotation speed and acceleration speed, spinning time and multiple properties of the solution such as viscosity, solvent, QD-concentration etcetera. Also the surface energy of the different substrates has influence. Multiple batches of PbS in chloroform are used, which are made and cleaned with slightly different recipes and have therefore different sizes and qualities. After each PbS layer, ligand exchange is performed with 1 vol% of EDT in acetonenitrile (ACN). The film is covered by this solution and after ten seconds the substrate is spin. After another ten seconds, five droplets of ACN are dropped to remove the redundant EDT.

Between each spinning step, the device is annealed at 140°C. Between annealing and the next step the substrate is cooled down. Annealing leads to a smaller inter-particle distance, causing three effects: the excitonic peaks are redshifted and broaden. Moreover, the tunnelling rate is increased leading to a bigger current [18]. However, when the annealing temperature is too high, the QDs could start sintering leading to reduced quantum confinement and a smaller band gap. This can be used to increase the current, but this should be avoided for light emitting properties.

Since the surface energy of the substrate is different than that of the surface of a PbS film, the first and the other layers are prepared differently. For the first layer a 5 mg/mL solution is used with a closed lid at a speed of 4000 rpm with an acceleration of 800 rpms/s for 40 seconds. If this layer is to thick, the ligand exchange would create cracks in the film due to settling and the fact that the nanocrystals tend to group instead of sticking to the surface. A thinner layer doesn't settle that much and therefore this problem is reduced.

The second till the fourth layers the ligands are spin coated with open lid and a 10 mg/mL solution. The speed is 800 rpm, acceleration is 800 rpm/s and spinning time is 40 seconds.

3.3.2 Dielectric

As previously mentioned for the glass device a top gate architecture was chosen, therefore the dielectric has to be spin coated on top of the active layer. A solution of 50 mg/mL P(VDF-TrFe-CFE) (PVDF) in cyclohexane is stirred on a magnetic stirring hot plate overnight at 60°C at a speed of 50rpm. The solution is first filtered and then spin coated with open lid at a speed of 800 rpm and an acceleration rate of 800 rpm/s in 140 seconds. Different annealing temperatures and conditions were tested. The thickness of the dielectric on an ITO substrate is measured using a profilometer. This measurement is done by a low force stylus which is dragged across the surface. Also the impedance of the polymer has been measured by a complex impedance measurement in a parallel plate capacitor configuration with aluminium contacts. In figure 12 the simplified circuit is shown where R2 and C are respectively the resistance and

capacitance of the dielectric layer.

The resistivity and dielectric constant were calculated for bias voltages of 0,2.5,5,7.5,10,-2.5,-5.,-7.5,-10V. These were averaged. Interestingly annealing above or below the crystallisation temperature and faster extraction of the solvent by a vacuum can influence these properties a lot. Also different filter sizes of 0,45μm and 5μ are tested to check if there are still some PVDF powder residues or other impurities influencing the film properties in the solution.

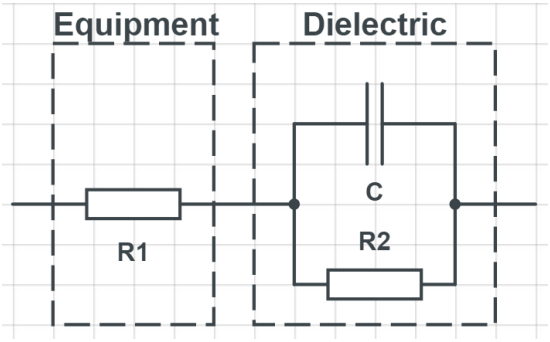

Figure 12: Simplified capacitance measurement circuit

3.4 Environment

The PbS film is very sensitive to ambient conditions since H_2O and O_2 can act as traps for electrons. The devices were therefore prepared, kept and measured inside nitrogen filled gloveboxes. The H_2O and O_2 concentrations were kept below 10 ppm. Performances decrease upon storage of the device, but annealing them for half an hour at 120°C help to reobtain the original performance [3].

3.5 Characteristics measurements

The transistor characteristics measurements are done in a glove box. Three probes are connected to the electrodes. Different sweeps can be performed, where the transfer and output curves are important for the device characteristics. When the devices are ambipolar, also light emission measurements are done.

3.5.1 Light

The PL and EL are measured using a spectrograph. For the PL, a laser is focused on the film (outside the channel). To align the device for EL measurement, the distance between the laser and the device is measured. The sample is displaced by this distance to get the device in focus. The gate source voltage is set arbitrarily constant, while the drain voltage is swept. Afterwards, the drain current and emission are compared.

Since there is no spectrograph inside the glove box, the devices must be placed in a vacuum chamber before taking it out the glove box and measuring the EL. The substrate is placed on an adaptor to make it fit in the vacuum chamber. The electrodes

and gates are connected by silver pasted gold wires to contacts. These are connected to a coaxial cable outside the chamber. This silver pasting process could be seen as 'cold soldering', because the solvent evaporates at room temperature leaving a silver conducting connection. Some devices were wire bonded and sealed between two pieces of glass. These two pieces of glass were glued with epoxy to protect the device from oxygen and water.

4 Results

4.1 PVDF layer

Table 1 shows the results of the measurements on different PVDF layers. As shown

sample	time (s)	temperature (°C)	filter size (um)	thickness (nm)	dielectric constant	resistivity ($\Omega \cdot m$)
1†	0		0,45	630	41,3	4,12E+10
2	20	85	0,45	580	35,5	2,76E+10
3	60	85	0,45	575	39,0	3,64E+10
4	60	85	5	575	40,9	3,54E+10
5	60	85 ^{vacuum}	0,45	585	38,9	3,51E+10
6††	60	135	0,45	580	14,1	3,08E+11

Table 1: Thickness, dielectric constant and resistivity for different annealing parameters. † V=5/7.5/10V are not taken into account. †† V=-7.5/10 are not taken into account.

in table 1, the not annealed sample had a very hazy looking layer of PVDF. When measuring the positive voltages, the circuit was shorted. These measurements were therefore not taken into account. More or less the same holds for sample 6, but in this case it was not completely shorted. From the other measurements of sample 6 one can see that the polymer doesn't behave as a good dielectric insulator anymore when it is heated till above the crystallisation temperature. This can be explained by the creation of crystalline domains in the layer.

The thicknesses of all annealed films are the same. From table 1 it is also shown that the electrical properties are better when the samples are annealed 60 minutes in comparison with 20 minutes. It is convenient to choose for a 5 micron filter since samples 3 and 4 have an equal dielectric constant and resistivity and it takes a lot of effort to put the PVDF through the 0,45 filter due to the high viscosity of the solution. Also the vacuum treatment doesn't influence the layer properties and is therefore not needed.

The annealing of PVDF on ITO should be done one hour at 85°C. When the layer thickness has to be changed, the spin coating settings need to be varied.

4.2 Active Layer Thickness

A bottom gate bottom contact Si/SiO_2 substrate was only partly covered by the third thick PbS layer. Therefore, it was possible to check if the properties of the FET are dependent on the number of deposited layers. In figures 15 and 16 it is shown that both devices showed saturation. All values in table 2 are deduced from the transfer curves of figures 13, 14, 17 and 18.

device	# thick layers	Carrier	Vd (V)	on/off ratio (10^)	mobility
3	2	p	2	1,2	4,73E-3
			5	1,9	5,1E-3
			10	1,7	5,91E-3
3	2	n	2	3,4	0,138
			5	3,2	0,392
			10	3,7	0,525
2	3	p	2	1,1	5,18E-3
			5	1,8	5,22E-3
			10	1,2	5,66E-3
2	3	n	2	3,3	0,177
			5	3,6	0,421
			10	3,6	0,632

Table 2: on/of ratios and mobilities of two devices with a channel length of 20 micron

As shown in table 2, the device characteristics are almost equal. However, all parameters increased a little bit after the third layer. The threshold voltages were more or less equal between 0 and 20V. The drain current is the most important for EL, in this case a minimum difference is observed. The mobility is however higher in the case of the 3 layer device

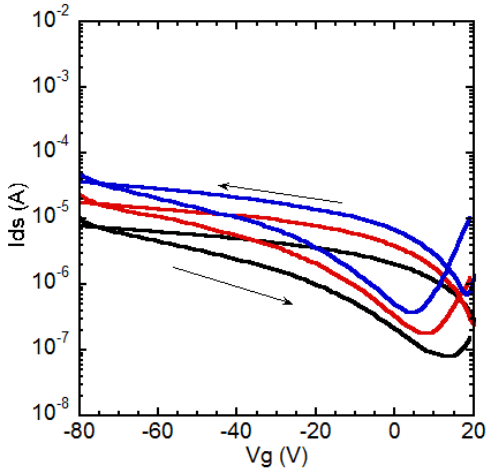

Figure 13: device 3:electron transfer curve for Vds=-2V,-5V,-10V

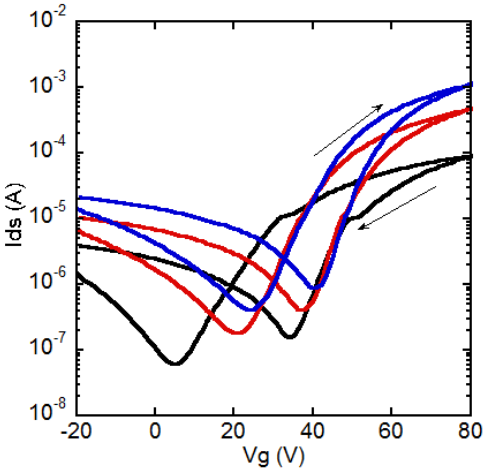

Figure 14: device 3:hole transfer curve for Vds=2V,5V,10V

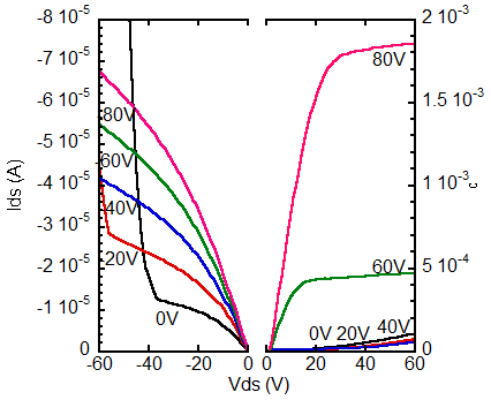

Figure 15: device 3:output curves

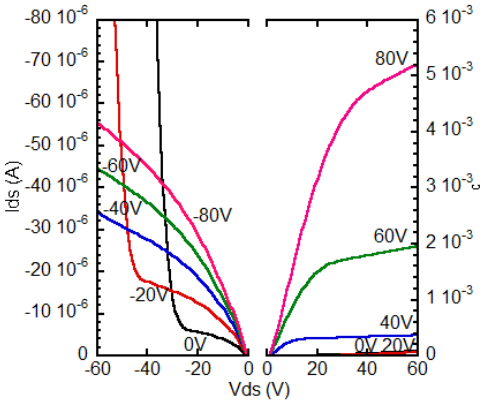

Figure 16: device 2:output curves

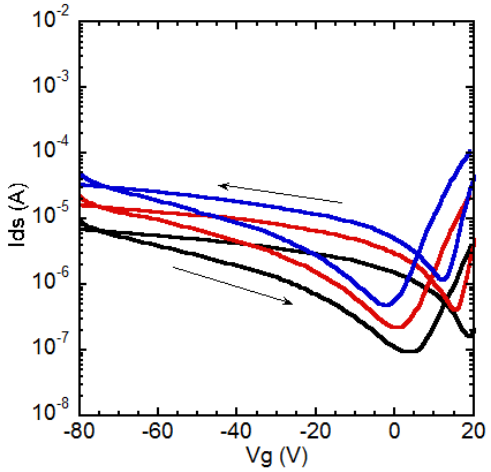

Figure 17: device 2:electron transfer curve for Vds=-2V,-5V,-10V

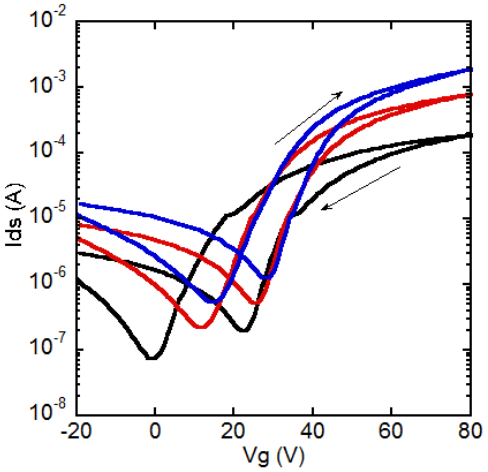

Figure 18: device 2:hole transfer curve for Vds=2V,5V,10V

4.3 Electroluminescence

The electroluminescence has been tried to be measured in different ways. None of the glass devices were working, because most devices had a shorted gate due to the deffects in the dielectric layer. The only working devices were on silicon making the measurement of the electroluminescence more complex. It was very hard to align them, since a laser can't go through the substrate. The other option was to align it using the reflection of the laser on the silicon substrate. However, the devices still had to be kept in an nitrogen atmosphere. No sample holders were available where the silicon was very close to the glass, which was needed to reflect the laser at 45°. Therefore a FET on a silicon substrate was wirebonded and sealed with epoxy between two pieces of glass. In this configuration the device could be aligned and the EL spectrum measured while the output curve was measured.

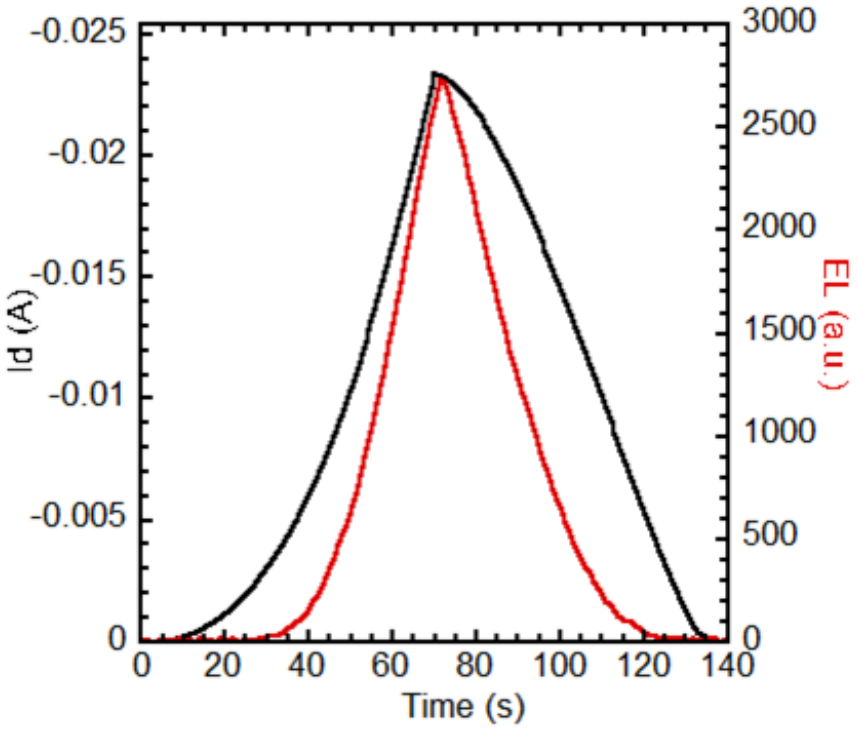

Figure 19: Uncalibrated electroluminescence at 1590 nm and draincurrent plotted versus time

It is clearly seen that the electroluminescence signal correlates with the drain current (figure 19). However, the drain current increases faster and decreases slower, but it is obvious that the EL is induced by this current. The difference is probably mostly created by charge traps. The silver paste could be a huge contributor to these charge traps, since the paste doesn't form a nice surface. There is also a small possibility that something else in the substrate is being measured, for example a plasma that is produced by the electrodes when a voltage is applied. For these small voltages (figure 22 however it is very likely that the recombination is measured.

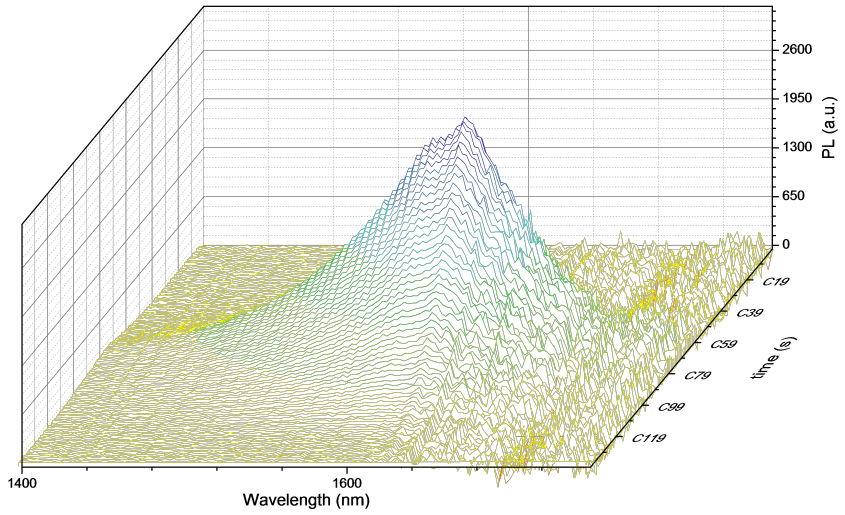

Figure 20: calibrated electroluminescence spectrum for sweep of figure 22.

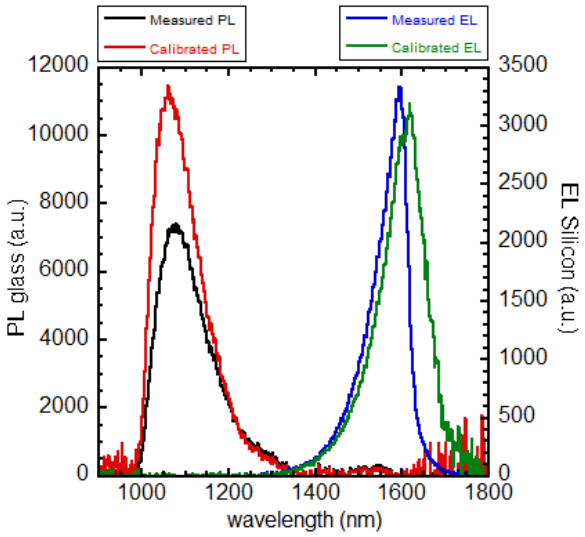

Figure 21: Photoluminescence compared with electroluminescence

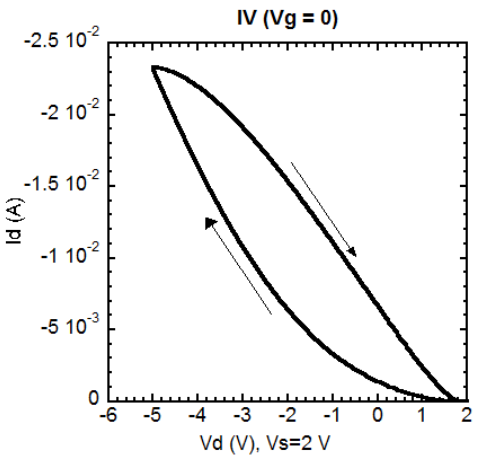

Figure 22: Output curve of the measured device with Vs=2V.

In figure 20, the electroluminescence is shown for the sweep of figure 22. The peak of the EL spectrum is around 1600 nm. This is a big redshift compared to the first excitonic peak of the quantum dots in solution, which is about 1200 nm. The most probable explanation for this is sintering of the quantum dots, which means that the substrate is annealed at temperatures that are too high or too long. Another explanation could be that there are some quenching effects at the electrodes/silver paste. Also this is not very likely since there would be still a small peak at the pristine wavelengths. From picture 20 we can conclude that the energy of the EL spectrum is not changed by different drain currents.

To check if the luminescence spectrum was indeed redshifted due to sintering, the PL of the active layer has to be measured. Since the substrate is not transparent and there was epoxy, silver paste and gold wire above the substrate this was not possible. A probe sample made on a glass substrate have been made simultaneously. The PL of these substrates could be measured, but the excitonic peak was still at 1100 on these devices, see figure 21. An explanation for this could be the heat conduction of glass, leading to a lower annealing temperature than that of the sample fabricated on the highly doped Si substrate.

However, this experiment can not be conclusive and more samples should be measured to ensure that the EL signal is related to the active layer. The gate voltage was not influencing the electronic characteristics of the device. This could be due to a high doping level of the active layer. Therefore, it was not possible to check if there was any gate dependence. Again more experiments should be performed to clarify the nature of these observations.

5 Conclusions

The aim of this project was to get a working light emmitting FET using Colloidal semiconductors as active material. Even if is has been proven that it is possible to have light emission using a Si/SiO2 bottom gate bottom contact FET, the dependence on different applied voltages has not been proved or even been measured.

First of all, PVDF has to be tested more in order to find the perfect recipe for this polymer. Instead of PVDF on glass also other substrates could be used, for example a transparent plastic substrate. Also different measurement setups should be tested.

Further research has to be done on these devices. First, the gate voltage need to be set constant in order to get a constant gate-source voltage. In this case, one charge carrier type will already form an accumulation layer. When the drain voltage is then changed, the other charge carrier also starts to be injected. This is in principle what was measured in this project, but it will be important to check if there is indeed light emission only when the FET is in ambipolar regime.

Also, pictures need to be taken in order to check if and how the recombination zone is moving with a changing gate voltage. This can be done by fixing the source-drain voltage and sweeping the gate voltage.

Another interesting measurement is when the drain current is fixed and the gate voltage is swept. Probably a 'plateau' will form in the plot of the EL for all gate voltages where the recombination zone is far away enough from the electrodes. When an integrating sphere is used, it is possible to measure all photons and the total EQE and correlation of the light emission and the drain current could be determined.

At last, also the frequency response could be measured, to know if the switching of the light emission could be used for high speed data transport.

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