UNIVERSITY OF GRONINGEN

MASTER'S THESIS

Utilizing polymer wrapped single-walled carbon nanotubes in neuromorphic and memory applications

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Abstract

Artificial Neural Networks recently became of great interest due to the upcoming field of machine learning. Using dedicated hardware that mimics the brain will revolutionize machine learning algorithms. In Artificial Neural Networks, designing Artificial synapses that can maintain several conductance state in a non-volatile way is a major challenge. In this work we present a proof-of-concept of a three terminal artificial synapse that utilizes common current hysteresis in s-SWCNT transistors. The device shows a strong plasticity with a dynamic range spanning several orders of magnitude. The conductance of the transistor can be tuned by applying pulses to the gate terminal of the device. The modulation of the conductance is, to some extent, non-volatile implying that these devices could be used in future artificial neural network.

Furthermore in this work we demonstrate that high-end binary memory elements can be designed when s-SWCNT transistors are gated by the ferroelectric polymer P(VDF-TrFE). These binary memory elements are made with solution processable materials, showing potential applications in flexible, low-cost and disposable electronics. The memory on/off ratio is around 10^4 with retention time larger than $10^4 s$ and read/write endurance $>$ 200s.

Acknowledgements

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Contents

Chapter 1

Prologue - Neuromorphic computing

Brain inspired computers

Computers, based on Von Neumann architectures, have become essential in all aspects of modern life. There are almost no processes in everyday life that do not to some extent involve the usage of a computer. These computers have not only been the engine for continuous improvement of modern civilization, but are also continuously improved themselves. This continuous improvement, partially dictated by Moore's law, which states that the number of transistors on a chip doubles every two years, has been going on for decades. Due to fundamental physical limitations Moore's law will end at some point in time, raising the question: how will computers evolve after Moore's law will break down?

This fundamental limitation in the fabrication of smaller and smaller transistors, combined with the development of new algorithms in the field of machine learning, calls for a new era of computers. In the early 1990s researchers started to investigate how to tackle this problem by developing "neuromorphic" computers. Like with many great inventions, the idea is to be able to fabricate computers which work as the brain works. Where a conventional computer based on CMOS technology works with transistors which make them a digital binary system, the brain works in an analogue fashion. Furthermore the human brain has the extreme advantage of a very low power consumption of around 20W[1]. This power efficiency combined with the massive parallelism that the brain has, makes it an ideal system for specific tasks like pattern recognition, decision making and (machine) learning.

The human brain is not yet fully understood by biologists and neurologists, however several ideas are postulated to be contributing to the way the brain learns and works. The brain consists out of 10^{12} neurons and 10^{15} synapses[2]. These neurons are connected in a complex network and have a connection that has a certain strength, which can be adjusted overtime and can be seen as the memory of the brain. The biological element that governs this strength is called the synapse. A famous theory on how these strengths changes over time is postulated by the Hebbian learning rule. The quote by Donald Hebb "neurons that fire together wire together", summarizes how STDP (Spike-time-dependent plasticity) works. The "firing" of a neuron is the way a neuron sends signals to other neurons. If two neurons, a pre-neuron and a post-neuron, are connected through a synapse and the pre-neuron firing results in the firing of the post neuron, then the connection between these

neurons is strengthened. The ability of the synapse to increase its strength is often referred to as Long Term Potentiation (LTP), the decrease of strength is called Long Term Depression (LTD). This potentiation and depression, also called plasticity, is one of the main mechanisms responsible for learning within the brain. A thorough explanation of these concepts will be given in chapter 3. Since the synapse is such a crucial element in neuromorphic computing, for which there is no artificial counterpart to-date, a large effort is concentrated on making devices that emulate the properties of a synapse. This work contributes to the field of artificial synapses by using devices based on highly purified polymer-wrapped semiconducting single-walled carbon nanotubes.

Thesis outline

This thesis reports a selection of the work performed in this master project and consists of two main topics, of which one relates to neuromorphic computing whereas the other to the development of binary memory elements. The reoccurring material in both chapters is the use of polymer-wrapped semiconducting single-walled carbon nanotubes as active material. In chapter 2, an introduction is given to neuromorphic computing and artificial neural networks. Here we also discuss technical requirements that memristive elements should posses for implementation in neuromorphic computers. Important learning mechanisms like LTP, LTD and STDP are discussed to give the reader a solid basis for understanding the further discussed results. In chapter 3 all necessary physical insights are treated for understanding carbon nanotube field-effect-transistors. Polymer-wrapping of carbon nanotubes is discussed and the electrical properties are described. In section 3.5 ferroelectric polymers are discussed, which were used to create binary memory elements in chapter 4.

Chapter 4 can be considered as a stand-alone chapter, where we demonstrate the use of ferroelectric polymers, specifically P(VDF-TrFE), as gate dielectric on s-SWCNT transistors to create high performance fully solution processable binary memory elements. The chapter is written in a manuscript style, so that it could be used as a startpoint for a possible future publication. In section 4.5 a discussion is dedicated to how and why this device is not suitable for applications as a synaptic transistor, which was the original goal of this investigation.

In chapter 5 we present a proof-of-concept study of a synaptic transistor that utilizes commonly seen current hysteresis in the transfer characteristics of s-SWCNT transistors. In this proof-of-concept we show the plasticity of the device and make comparisons between the characteristics of this device in a inert and ambient environment. In the last chapter a conclusion is drawn regarding the full research and some suggestions are provided to continue these investigations.

Since this master project was not only a jump in the dark for the writer of this thesis, but also for the entire research group, a large effort had to be concentrated on setting up a measurement environment. Therefore Appendix A gives a short overview of the measurement software that was build to characterize our devices. In this appendix we describe the choices we made and the work that was done controlling two Agilent semiconductor analyzers using Python and the PyVisa library to develop a variety of measurement protocols.

Chapter 2

Introduction to neuromorphic computing

The aim of this chapter is to give an overview of the requirements that should be met in order to successfully create new technology for artificial neural networks and furthermore to put the development of neuromorphic computing in perspective by answering the 'why?'-question. To discuss this, we first make the comparison between conventional Von-Neumann computers and the brain, which can be considered as te main inspiration for neuromorphic hardware. Secondly we discuss some specific abilities that neuromorphic hardware should posses. Here we also set research goals and discuss which physical parameters are important.

2.1 Human brain vs silicon

A comparison between the human brain and a conventional personal computer, based on binary logic using silicon chips, reveals several core differences. Three major differences that can be distilled from this are: the high amount of parallelism in the brain, the extremely low power consumption and the collocation of memory and computation[32]. The first difference is one of the main reasons the brain has such an efficient learning mechanism. In the early days of neuromorphic computing creating hardware that was able to perform parallel operations was therefore one of the key topics that was being investigated[33]. The low power consumption of the brain is something that became more and more important over the last years. The human brain, only consumes approximately 20W, which is a fraction of power compared to modern computer clusters that run neural networks and/or perform machine learning tasks. Lastly, a major difference is seen in the way computations are done. The human brain performs logic operations while reading memory elements, whereas conventional computers do not have CPU's and memory collocated. This limitation, known as the Von-Neumann bottleneck, fundamentally limits computational speeds and also the possibility to achieve low power consumption[34, 35].

2.2 An introduction to neural networks

There is a large variety of neural network models. A dense overview of available models related to neuromorphic hardware is given by Schuman et al [32]. In this review a large effort is focused on describing different neuron, synapse and network

models. Here we introduce a simplified neural network, referred to as a perceptron neural network, with an integrate-and-fire neuron, which is often considered as the basis of neural networks.

In biology a neuron usually consists out of a body, an axon and several dendrites. The dendrites are usually connected to synapses which are in turn connected to the axons of other neurons. Schematically this is depicted in figure 2.1. The axon of a neuron can be considered as the output of the neuron, whereas the dendrites are inputs connected to axons of other neurons. The element that makes this connection is called the synapse.

In Artificial Neural Networks (ANN) often several layers of neurons are connected in series, where each neuron in layer y_i receives inputs from all neurons x_i, here x_i corresponds to a layer of neurons and y_i as well. For simplicity only one neurone, named y_1, is depicted in figure 2.1. This neuron receives inputs from several inputs x_i which are weighted by w_i. In an ANN a common way to let the neuron handle the input is by using a (leaky-)integrate-and-fire circuit. This system integrates all its inputs and sends a signal to all Axon terminals if a threshold is reached. Mathematically this can be written as:

$$u(t) = \int_0^t \boldsymbol{x}(t) \cdot \boldsymbol{w}. \tag{2.1}$$

If $u(t)$ reaches a certain threshold value it resets u and sends a signal to a next layer of neurons, similar to how neurons x_n send signals to neuron y_1.

Several learning rules can be implemented to let the network learn. This learning relies for a large part on how the synaptic weight, in figure 2.1 w_i, changes. The ability to modulate the strength of a synapse is referred to as the plasticity of the synapse, this synaptic plasticity is believed to be a dominant mechanism for learning in the human brain[36, 37]. The synaptic weight should be seen as the strength of the connection between two neurons, i.e. the conductivity between the two neurons. In the next section one of the most important learning rules is explained as one of the hardware requirements a synapse should posses.

2.3 Neuromorphic hardware requirements

As mentioned a core feature of a neural network is the synapse. That is why this section will be mainly focused on the hardware requirements that artificial synapses should meet. To be able to implement learning rules, the artificial synapse should be able to change its conductivity in a non-volatile manner. Hereby it should range over tens to thousands of different states. Furthermore, it is necessary that these states have some retention time that is significantly larger than the average modulation time, which is the average time between the updating of the conductance state. Neuron spiking rates in the brain are in the order of several Hz[38, 39] so spanning seconds is a necessity, however, for most applications hours to days is preferred. In addition, an artificial synapse should posses a sufficient dynamic range[40]. This corresponds to the range in which the conductance is modulated, i.e. the largest conductance state divided by the lowest conductance states.

Besides the ability to be switched in different states the scalability of the device is of greatest importance. Dimensions of biological synapses are in the order of 20nm[41]. Scaling down devices to this size has shown to be doable, however

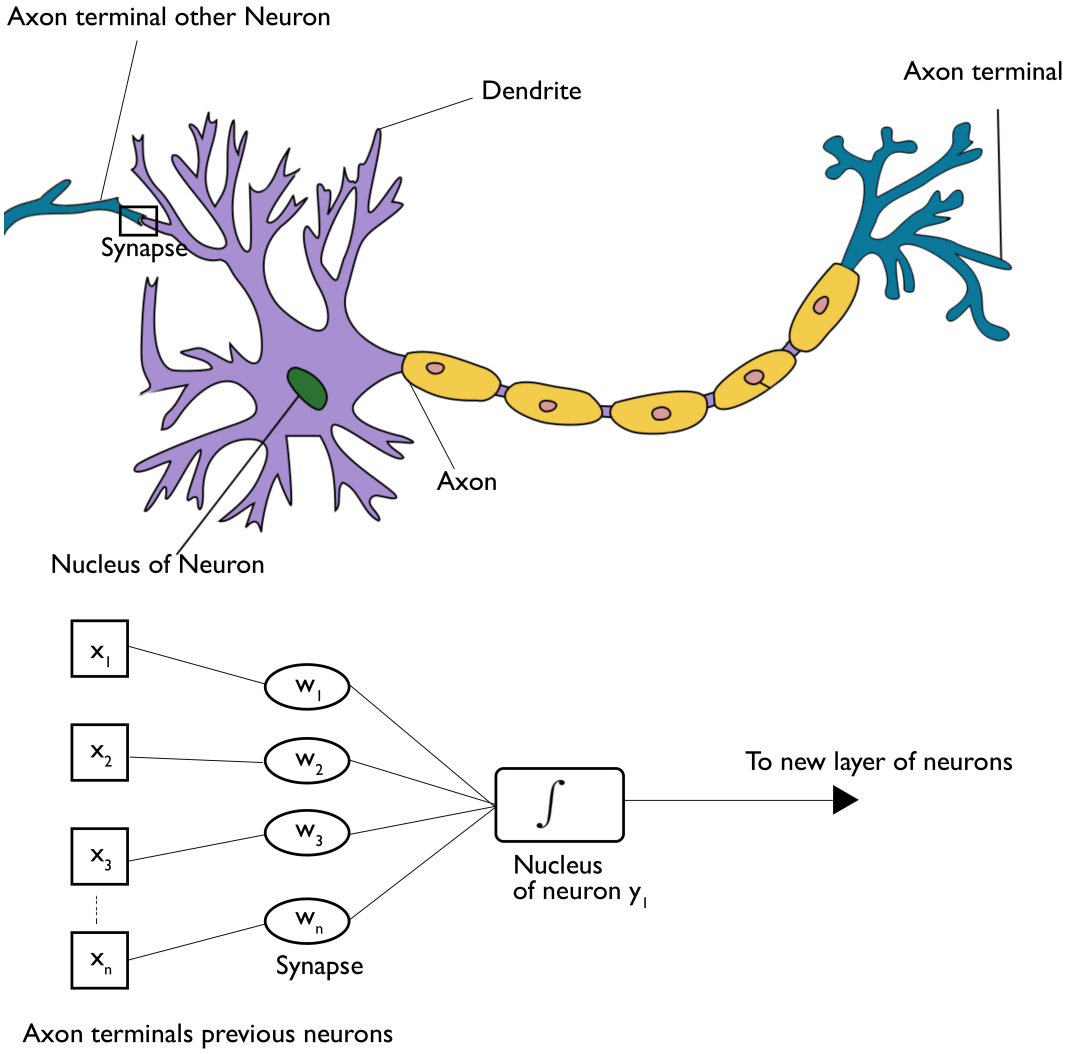


FIGURE 2.1: Schematic overview of a neuron and it's analogy to a neural network. On the top a biological neuron is depicted. The green Axon terminal from another neuron connects to a dendrite of the neuron via a synapse. The neuron has several inputs like this (only one synapse is depicted here), the output terminal of the neuron is an Axon that can connect to several other neurons via its axon terminals.

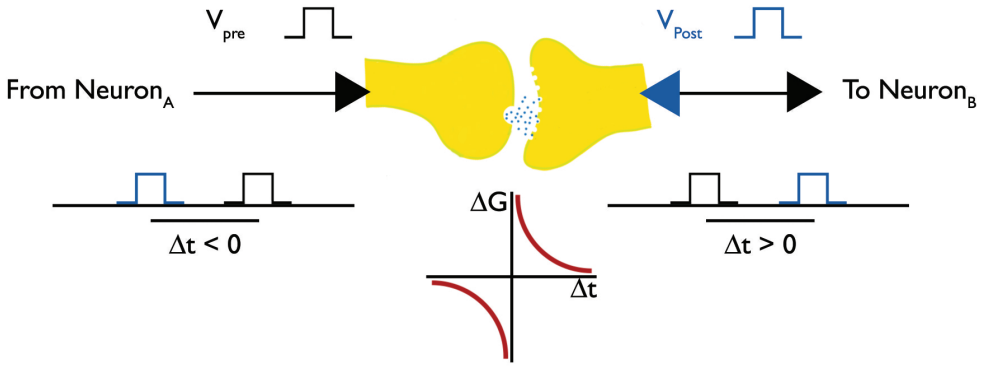


FIGURE 2.2: In the top of the figure a synapse is schematically drawn connecting $Neuron_A$ and $Neuron_B$. On the lefstside a pre-synaptic pulse is applied originating from $Neuron_A$ and is weighted by the synapse and converts to an IPSC (inhibitory post-synaptic current). If due to this IPSC, $Neuron_B$ fires, the Neuron sends a post-synaptic pulse back to the synapse. Based on the time difference, Δt between these two the synapse will be either depressed if $\Delta t < 0$ and potentiated when $\Delta t > 0$. The graph shows typical STDP behavior, where ΔG corresponds to the conductance modulation.

maintaining several conductance states having a large dynamic range is proven to be more difficult.

Remarkably there is a feature where requirements on artificial synapses are less strict than in common CMOS based computers. The fault tolerance in biological synapses is very high. It was shown that implementing large variations in device resistances can still make a neural network perform very well[42]. In contrast when single transistors in chips do not work properly whole parts of CPU's can be malfunctioning

Donald Hebb was the first to propose that synaptic plasticity is the core learning mechanism in the brain[43]. In the mean time this plasticity has become one of the most intensively researched topics within neuroscience. Different types of plasticity can be distinguished. Long Term Potentiation (LTP) and Long Term Depression (LTD) are features where the synaptic weight changes for a longer time. This longer time can be from seconds to minutes up to years. Next to LTP also short-term potentiation (STP) is observed in biological synapses. This is an effect where a pulse modulates the synaptic weight after which the synaptic weight slowly falls back to its original state. In biological synapses it is observed that multiple pulses that would normally induce short-term potentiation can induce long-term potentiation when they are fired in a short time frame. An often mentioned concept that is related to this is Paired Pulse Facilitation, also called Neural Facilitation. When two pulses are fired in a short time window, the response to the second pulse is enhanced by the first pulse. This mechanism can play a role in temporal information processing[44–46]. Whether artificial synapses should posses LTP, STP or PPF, and how long-term LTP should be, strongly depends on the type of application of the ANN.

One of the fundamental learning mechanisms that is related to LTP and LTD is Spike Time Dependent Plasticity (STDP)[47–49]. STDP is a type of "Hebbian Learning", named after the previously named Donald Hebb, which temporally correlates

pre-synaptic pulses and post-synaptic pulses. In the brain the synapse is a two terminal "device", where spikes are applied on both sides of the synapses, see also figure 2.2. If Neuron_A fires to Neuron_B then the spike passing through the synapse, that is connecting Neuron_A and Neuron_B, is referred to as the pre-synaptic spike. If in turn Neuron_B sends a spike further through the neural network it can also send a post-synaptic spike back to the synapse. If the pre-synaptic pulse, coming from Neuron_A proceeds the post-synaptic pulse, we can say that the pre-synaptic pulse contributed to the firing of Neuron_B . Therefore the strength between the two neurons will increase (i.e. LTP). If, however, the post-synaptic pulse proceeds the pre-synaptic pulse, we can be sure that the spike of Neuron_A did not contribute to the firing of Neuron_B and therefore the strength between both neurons is depressed (i.e. LTD). This process is schematically shown in figure 2.2. This process is considered to be the most important learning rule of the brain[49] and is therefore also one of the most researched topics in artificial synapses.

Chapter 3

Materials

3.1 Carbon nanotubes

The carbon nanotube is a one-dimensional material made out of only carbon atoms. Effectively one can think of a carbon nanotube as a cylindrically rolled up sheet of graphene. Carbon nanotubes can be synthesized as single walled structures, but also as multi-walled structures. In this work single-walled carbon nanotubes (SWCNTs) are used. Carbon nanotubes can have diameters as small as 0.4nm and length/diameter ratios up to 10^4, which makes them an ideal one-dimensional material [3]. Depending on the chirality of the nanotube (i.e. the way the nanotube is rolled from graphene) the nanotube is either semiconducting or metallic (actually, the metallic nanotubes are referred to as a zero-bandgap semiconductors). This bandgap gives the nanotube the possibility to be used in several electronic applications such as field-effect transistors[4], sensors[5] and computers[6]. Due to their tunable properties by quantum confinement, the excellent mobility, the solution processability[4] and possible bottom-up fabrication[7] it is often mentioned to be one of the most promising materials for future miniaturization of electronics.

3.2 Structure of carbon nanotubes

The chirality of the nanotube is specified by the chiral vector

$$\boldsymbol{C}_h = n\boldsymbol{a}_1 + m\boldsymbol{a}_2,$$

where the pair of indices (n, m) denote the number of unit vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$ in the hexagonal honeycomb lattice. As can be seen in figure 3.1 the chiral vector makes an angle with respect to $\boldsymbol{a}_1$. Three specific types of nanotubes can be distinguished. When $\theta = 0$ this corresponds to zigzag nanotubes, whereas $\theta = 30°$corresponds to armchair nanotubes. All other nanotubes with $0 < \theta < 30$ are called chiral nanotubes. The diameter of the nanotube can be related to the Chiral vector and to the integers n and m as

$$d_t = \frac{C_h}{\pi} = \sqrt{3}a_{C-C}(m^2 + mn + n^2)^{\frac{1}{2}}/\pi,$$

where a_{C-C} is the nearest neighbor distance between two carbon atoms.

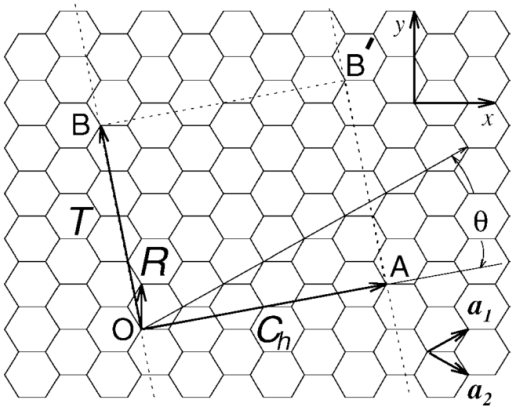


FIGURE 3.1: The unrolled honeycomb lattice of graphene. When the sites O and A are connected by the chiral vector and the same is done for B and B', a nanotube can be constructed by using this as the unit cell of the nanotube.The figure is constructed for an (n,m) = (4,2) nanotube

Omitting a long derivation, which is properly explained by Dresselhaus[3], it can be shown that SWCNTs with $n - m = 3j$ and $n \cdot m \neq 0$, where $j \in \mathbb{N}$, would be metallic nanotubes and SWCNTs with $n - m = 3j \pm 1$ are semiconductors. It should be noted here that this is derived from graphene and that the curvature is not taken into account, strictly speaking therefore a very small band-gap arises when $j \neq 0$[3]. Therefore metallic nanotubes with $j \neq 0$ are sometimes referred to as quasi-metallic.

A schematic overview of the Density of States (DOS) is given by figure 3.2. Here three different chiralities are depicted, respectively a zigzag tube, a chiral tube and an armchair nanotube. The spikes that can be seen in the DOS are called Van-Hove singularities and are characteristic for one-dimensional systems. The band gap, that arises in semiconducting nanotubes, can analytically be calculated by

$$E_g = \gamma(\frac{2a_{C-C}}{d_t})$$

, where γ is the hopping matrix element ($\approx 3eV$). The $1/d_t$ dependency shows that the bandgap can be controlled by the diameter of the nanotube and hence shows the tunability of carbon nanotubes.

3.3 Polymer wrapped Carbon nanotubes

There are different ways of creating SWCNTs. The first SWCNTs were synthesized using an arc-discharge method, properly explained by Arora et al[8]. After this method was demonstrated, several other methods were shown to produce SWCNT, such as chemical vapor deposition (CVD)[9] and laser ablation[10]. All these methods have their advantages and disadvantages, however the common problem with these methods is the production of both metallic and semiconducting nanotubes. For the fabrication of nanotube transistors it is of the most importance that the active material only consists of semiconducting tubes, otherwise this would produce a short in the channel.

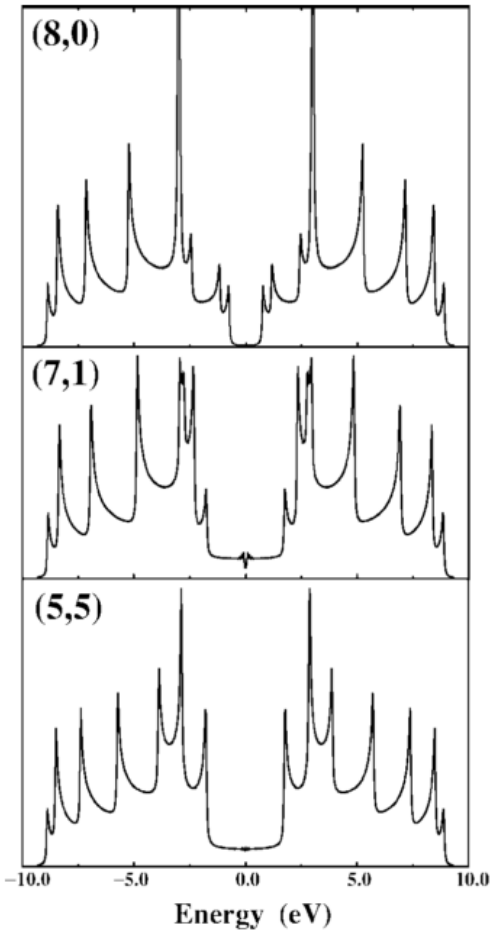


FIGURE 3.2: Electronic densities of states for different chiralties of nanotubes (5,5), (7,1), and (8,0). The DOS shows van Hove singularities characteristic of one-dimensional systems. Image adapted from: [3].

Various methods to discriminate between semiconducting (s-SWCNT) and metallic (m-SWCNT) SWCNTs have been investigated in the past. In general these methods can be divided into two main categories: covalent functionalization and non-covalent functionalization. Besides the discrimination between the s-SWCNT and the m-SWCNT, also the dispersion in solution is an issue, since the nanotubes tend to bundle in most solvents. Covalent functionalization could for example be done by selective reactions of diazonium salts with metallic tubes[4]. One of the problems with this technique is that covalent functionalization could alter the electronic properties of the tubes[4].

Non-covalent functionalization is preferred since it does not severely alter the physical properties of the nanotubes. Several techniques that have been investigated are density gradient ultracentrifugation (DGU)[11, 12], gel chromatography[13] and wrapping by conjugated polymers[4]. In this thesis only the later is used. Previous research in our group has shown that devices made from the the inks produced by this technique give high reproducibility and high on/off ratio's. Furthermore the ink itself shows a long shelf lifetime.

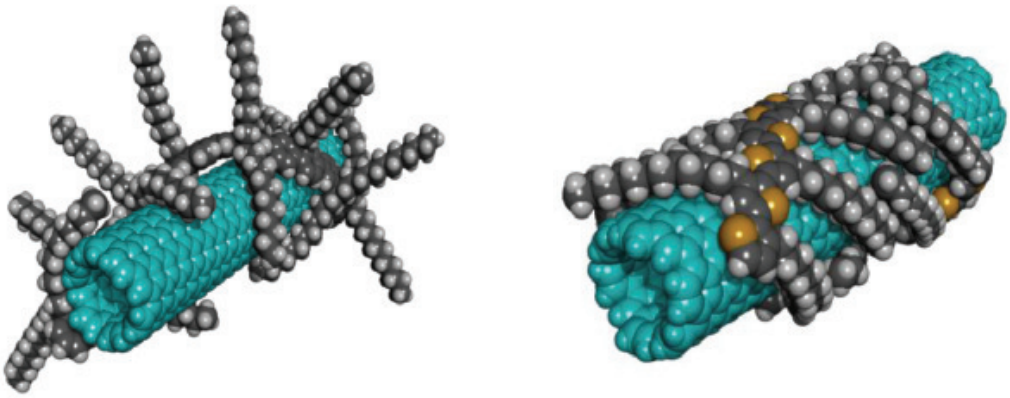


FIGURE 3.3: Molecular model of the wrapping of a nanotube (8,6). Wrapped by PF12 on the left and P3DDT on the right.[14]

The technique uses π-conjugated polymers which wrap around the nanotube due to $\pi - \pi$ interaction of the polymer backbone with the carbon nanotube wall. The long side chains of the polymer wrap around the nanotube by van der Waals interactions. When the nanotube is wrapped with a sufficiently long polymer backbone, the nanotubes can be individualized in solution, making a stable colloidal solution. The current understanding is that the wrapping screens the polarizability of the nanotube and thereby individualizes the nanotube. The metallic nanotubes which have a higher static polarizability (nearly three orders of magnitude higher[15]) can bundle and can therefore be extracted from the solution. The first work that shows this ability of conjugated polymers to select SWCNT was reported by Nish et al[16] using a polyfluorene derivative, (poly9,9-dioctylfluorene-2,7-diyl), also called PFO. Later it was shown that also polythiophene derivatives can be used for wrapping, selection and individualization of the nanotubes. In this work specifically the polythiophene derivate P3DDT (poly(3,dodecylthiophene-2,5-diyl))) was used, since it was shown that it capable of effectively wrapping smaller diameters nanotubes (HiPCO nanotubes)[14]. Figure 3.3 shows schematically the wrapping of PF12 and P3DDT on a (8,6)-SWCNT.

3.4 Field effect transistors

A field effect transistor is a three terminal device with a source, drain and gate electrode. There are different types of field effect transistors, in this research we use metals the source and drain electrodes to be metallic with a semiconducting material, carbon nanotubes, between them.

In field effect transistors (FET) the gate electrode controls the induced charge density in the channel which is formed between the source and the drain electrode. The gate electrode is separated from the semiconducting channel by a dielectric material, which is often an oxide layer. Schematically such a transistor is depicted in figure 3.4a.

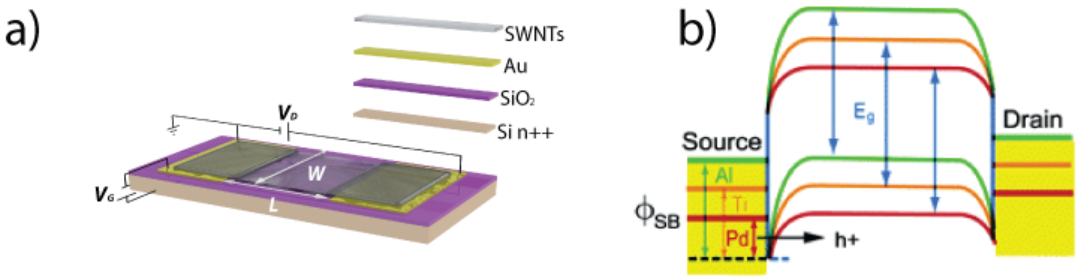


FIGURE 3.4: a) Schematic structure of a SWCNT Field-effect transistor. The channel is formed by the active material (SWCNT) and has a width W and length L. The gate electrode in this case is n++ doped silicon. b) Energy bands of carbon nanotube channel with the workfunctions of different electrodes, indicating the band bending with different workfunction electrodes. Images adapted from:[17]

The active channel is made of s-SWCNTs and is characterized by a width W and length L, which is formed by the separation of the source and drain electrodes. The electrodes are made of gold deposited on top of SiO_2 dielectric. The gate electrode in this case is an highly n++ doped silicon layer which behaves as a metal at this doping level. To inject carriers into the channel effectively the workfunction of the electrodes should be close to the HOMO level for holes and close to the LUMO level for electrons. A large energy difference between these two levels results in the formation of a Schottky barrier and limits the On-state conductance of the device. Some examples of common metals and their workfunction with respect to the HOMO and LUMO (valence band and conduction band) of carbon nanotubes are shown in figure 3.4b

The ambipolar properties of the nanotubes result in the possibility that both electrons and holes can be the main charge carrier, depending on the applied gate bias. However in this research and as often reported in literature, the dominant transport is by holes due to a variety of reasons. (i) The electron accepting behavior of the wrapping polymer can make the nanotube behave more p-type; (ii) the exposure to oxygen and water suppresses electron transport and (iii) the choice of gold electrodes make it easier to inject holes than electrons, since the workfunction of gold lies closer to the HOMO level (valence band) of the s-SWCNTs.

The transistor is operated by applying a gate voltage V_G on the gate electrode. The transistor channel will behave as a capacitor due to the non conducting dielectric layer. If the gate voltage is negative ($V_G < 0$) the fermi level of the SWCNTs decreases and positive charges will be accumulated in the channel. This leads to an increase of band bending at the SWCNT/source interface and will therefore reduce the width of the Schottky barrier formed on the SWCNT/electrode interface. This in turn will lead to an increased probability of holes tunneling through the barrier and therefore a hole current can flow between the two electrodes. Similarly when a positive gate voltage is applied an electron current can flow between the electrodes. This carrier tunneling through the Schottky Barrier is one of the main mechanisms for current flow in SWCNT-FETS[18].

Characterizing a transistor can be done by various measurements and parameters. Commonly the output characteristics and transfer characteristics are measured.

Output curves describe the dependency on the source-drain voltage, V_{DS}, at a fixed gate voltage V_G, whereas transfer curves are measured by sweeping the gate voltage at a fixed source-drain voltage. Parameters that are usually extracted out of these measurements are the on/off current ratio, sub-threshold swing, threshold voltage and mobility. These parameters can all be extracted from the transfer curve when the direct method is used. The threshold voltage, V_{TH}, is the gate voltage at which the device starts conducting either holes or electrons. The extraction of the threshold voltage can be done by several methods. The simplest method, which is also used in this research, is by fitting a line through the linear regime of the transfer curve and determining where it intersects with the line $I_{DS} = 0$. The slope of this line is called the transconductance, g_m and is used for calculating the linear mobility via,

$$\mu_{lin} = \frac{g_m L}{W C_i V_{DS}}, \tag{3.1}$$

where

$$g_m = \frac{dI_{DS}}{dV_G} \tag{3.2}$$

and L is the length of the transistor channel, W is the width of the channel and C is the capacitance of the dielectric. Another way of calculating the mobility is by using the saturation mobility, this is the mobility in the saturation regime. The saturation mobility is given by

$$\mu_{sat} = \frac{2L}{WC_i} \frac{dI_{DS}^{1/2}{}^2}{dV'_G}, \tag{3.3}$$

where V'_G is given by $V_G - V_{TH}$.

When we consider SWCNT transistors there are two different types of transistors. Transistors have been fabricated with single SWCNT[19], that can even show ballistic transport[20]. And SWCNT networks which exhibit at best diffusive transport[21]. In this research all transistors are based on networked s-SWCNT as active layer.

3.5 Ferroelectric dielectrics

A ferroelectric material maintains a permanent electric polarization that can be switched by applying a sufficiently large electric field on the material. These ferroelectric materials exhibit hysteresis loops which are analogous to magnetization-magnetic field hysteresis loops, see figure 3.5, which can be found in ferromagnetic materials.

Effectively the polarization state of such a material induces a positive charge on one side of the ferroelectric material and an equal but negative charge on the other side of the material. The ferroelectric material that we will be discussing in this work is the polymer P(VDF-TrFE), which is a copolymer of polyvinylidenefluoride and trifluoroethylene, schematically this polymer is depicted in figure 3.6. Besides the property of being ferroelectric these materials also have a very high dielectric constant up to 14[23]. For this reason several researchers have shown that this material is very suitable for being used as gate dielectric in a transistor configuration[24, 25]. The advantage of this high κ dielectrics is that the capacitance of the dielectric layer scales directly with the dielectric constant, κ, which enables low voltage, low leakage operation. Furthermore, the fact that this dielectric layer is a polymer and solution-processable makes it interesting for the fabrication of flexible.

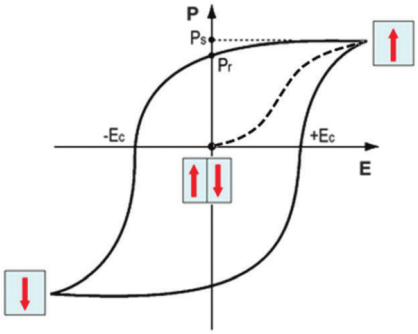


FIGURE 3.5: Ferroelectric hysteresis loop of a ferroelectric material. When an electric field, exceeding the coercive field, is applied on the material, the polarization switches. This induces a charge imbalance between both sides of the material, leaving a remanent polarization when the field is removed. Image adapted from: [22]

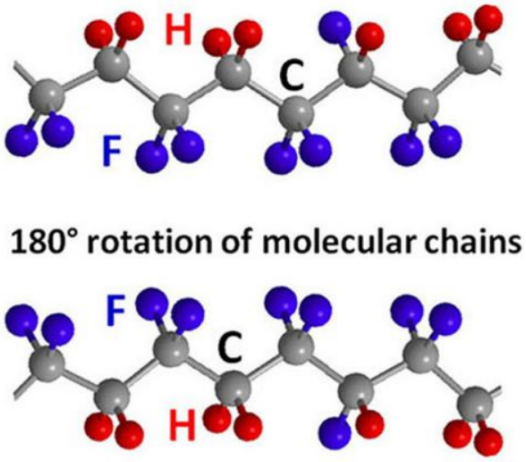


FIGURE 3.6: Structure of P(VDF-TrFE) and schematically showing the rotation of the chains as possible model for explaining the switching of the ferroelectric polarization. Image adapted from: [28]

P(VDF-TrFE)

The piezoelectric properties of PVDF, poly(vinylidene fluoride), were discovered in 1969 by Kawai et al[26]. A year later it was discovered by Glass et al that the material also possesses ferroelectric properties[27]. The discovery of these phenomena was essentially the start of ferroelectric polymers. Among all ferroelectric polymers known to date, P(VDF) and its co-polymers are considered to be the most promising due to their high remanent polarization and chemical stability. In this section the properties of the copolymer P(VDF-TrFE) will be discussed.

The ferroelectric properties of this copolymer arise from the strong difference in electronegativity between fluorine, carbon and hydrogen. The Curie temperature, usually used in the context of ferromagnetism, but also applied to ferroelectricity as the temperature at which a material switches from ferroelectric behavior to paraelectric behavior, is estimated to be above the melting temperature in the homopolymer P(VDF).[29, 30] The addition of P(TrFE) in the polymer lowers this Curie temperature to right below the melting temperature, making it easier to anneal the sample to

get proper ferroelectric behavior. The polymer PVDF can exist in four different types of crystalline phases. the β-phase, the α-phase, the γ phase and the δ-phase[31]. The phase configurations of P(VDF-TrFE) are very similar to the ones of the PVDF homopolymer. Of the four phases, the β is the most interesting since it is the polar ferroelectric phase. This phase is shown in figure 3.6.

Chapter 4

1T-type non-volatile memory using solution processable polymer wrapped s-SWCNT and P(VDF-TrFE)

4.1 Introduction

One-transistor (1T)-type nonvolatile memories, based on the non-volatile conductance state of a semiconductor gated by a functional dielectric have been of great interest due to their simple device architecture and the ability to be incorporated in high density memory arrays[50]. In general these devices can be categorized into three categories: ferroelectric, charge trapping and floating gate memories[51]. In the former one especially the combination with organic semiconductors have been of interest due to their low cost, solution processability and mechanical flexibility.

In this work the ferroelectric polymer P(VDF-TrFE) (70/30) is used as the functional dielectric. As active channel we used solution processable polymer-wrapped SWCNT ink, which contains $>$ 99.9% of semiconducting nanotubes[17]. These solution processable materials could be used in a variety of applications where there is need for easy to make, cheap, flexible and disposable electronics. These solution processable polymer wrapped s-SWCNT have shown to create very reproducible and high-performance devices[4, 52, 53], for these reasons they are often considered as the most promising material for future electronics[54–57]. By using the ferroelectric P(VDF-TrFE) as a gate dielectric on top of the s-SWCNT, the ferroelectric polarization state induces either extra positive charges or extra negative charges in the channel based on the different bistable polarization states. Our fabricated devices show an ON/OFF ratio of 10^4, data retention of $> 10^4 s$ and a write/read endurance of >200cycles.

The original goal was to try and partially polarize the ferroelectric polymer, thereby creating different non-volatile conductance states within the transistor. Section 4.5, of this chapter is dedicated to the attempts that have been made to set these different polarization states.

4.2 Experimental

Preperation of SWCNT ink

The HiPCO nanotubes used in this research were purchased from Unidyn Inc. The wrapping polymer P3DDT was synthesized via a GRIM method by our collaborator prof U. Scherf. The polymer is solubilized in toluene and stirred for one hour at 80°C. Sequentially the solution is stirred overnight at 50°C to guarantee full solubilization. The nanotubes are added at a weight ratio of 1:2 with respect to the polymer and are sonicated for 2 hours at 78W to promote proper dispersion and wrapping in the solution. During sonication the temperature is decreased from 25°C to 16°C. After the ultrasonication the dispersion is centrifuged at 30 000rpm for 1 hour(Beckman Coulter Optima XE-90) to remove all bundles of metallic nanotubes and other heavy weight impurities. To purify the solution from excess polymer, the supertnatant is centrifuged again at 55 000rpm for 5h. The semiconducting nanotubes which were initially individualized are now bundled in a pellet in the bottom of the centrifugation tube, whereas the excess polymer is still solubilized in the supernatant. The enriched pellet is now re-dispersed in o-xylene.

Fabrication of 1T memory elements

Field effect transistors are made on pre-patterned silicon substrates (Fraunhofer Institute for Photonic Microsystems) with thermally grown SiO_2 of 230nm. The pre-patterned source/drain electrodes consist out of 10nm ITO/30nm Au electrodes made in interdigitated channels of 2mm width and 20μm to 2.5μm length. In this research all results make use of the 20μm length channels, unless specified otherwise.

The s-SWCNT ink is deposited by using a blade coating technique (Zehtner ZAA 2300 Automatic film applicator coater), the blade speed is 3mm/s and the surface is heated to 70°C. During fabrication 8μL are deposited twice and spread by the blade over the surface of the substrate. Sequentially the film is annealed for one hour at 160°C. After this annealing a P(VDF-TrFE) layer is spincoated at 1500rpm for 60s with an acceleration of 3000rpm/s from a solution of 45mg/ml P(VDF-TrFE) in Methyl ethyl ketone (MEK). The spincoated layer is annealed at 140°C and afterwards a thin PMMA layer is spincoated from a solution of 5mg/ml in Toluene at 3000rpm for 60s with an acceleration of 3000rpm/s. The 45nm thick aluminum top contacts are evaporated through a shadow mask.

Characterization methods

The electrical characterization is done by using a probe station connected to a Agilent E5270B Precision IV Analyzer, which is controlled by a custom python code exploiting the PyVisa library, see also appendix A. XRD measurements are performed using a Bruker D8 ADVANCE X-ray powder diffractometer. AFM images are obtained by using a Bruker MultiMode 8 AFM. The P-E Hysteresis loops are measured with an aixACCT thin film analyzer in combination with a Radiant Precision Workstation.

4.3 Characterization of P(VDF-TrFE)

The P(VDF-TrFE) films were spin coated from a solution of MEK (Methyl Ethyl Ketone), since this would easily crystallize the P(VDF-TrFE) in the ferroelectric β-phase[30]. Furthermore literature indicates that 140°C is an optimal annealing temperature since it's above the Curie temperature, but below the melting temperature inducing crystallization in the β-phase[58].

To confirm proper crystallization in the ferroelectric β-phase, several characterization techniques were used. In figure 4.1a we see the XRD pattern of a spincoated P(VDF-TrFE) film on pristine sillicon. The characteristic peak at 19.7°is due to overlapping reflections of the (200) and (110) planes implying the presence of the β-phase [28, 60]

Topography examination shines light on the semi crystalline structure of the P(VDF-TrFE). AFM images shown in figure 4.1b show a rod shaped grain structure, which is also reported in the literature [30, 59]. We observed however that making thick layers introduced large surface roughnesses and pinholes, as can be observed in figure 4.1c, which resulted in shorts through the gate dielectric. Spincoating a thin layer of PMMA on top decreases the gate leakage, however it is difficult to observe the PMMA layer through AFM, since the PMMA produces a thin layer conformal to the grain structure of the P(VDF-TrFE) as can be seen in figure 4.1d.

To quantify the ferroelectric properties of the polymer, capacitors are made and a P-E hysteresis loop is measured. The P(VDF-TrFE) and PMMA layers are spin coated on top of a pre-patterned ITO/Glass substrate as explained in the experimental section. The P(VDF-TrFE) on the capacitor is annealed in the same way at 140°C for 1 hour and after the spincoating of the PMMA protection layer, the aluminum contact is evaporated through a shadow mask.

The resulting P-E loop is shown in figure 4.2. The measured coercive voltage is approximately 18V. The remnant polarization of $6\mu C/cm^2$ is slightly lower than reported values for pristine P(VDF-TrFE) in literature[58, 61]. This could be due to the additional PMMA layer, which appeared to be necessary to reduce leakage. Furthermore, it should be noted that the remnant polarization is also dependent on the sweeping voltage, since the polarization should be fully saturated. Besides optimization of the fabrication process the annealing could also be optimized, possibly resulting in higher remnant polarization. We observe also a very clear frequency dependence on the remnant polarization. The switching kinetics of P(VDF-TrFE) have been studied in more detail by Zhao et al[61] and Hu et al[28].

In this work the switching of the created memory is done by using square pulses, whereas the hysteresis loops of the capacitors are measured by using triangular waves.

4.4 Results and Discussion

First transistors were made with only the polymer wrapped s-SWCNT without any gate dielectric on top. The transistors are gated by the bottom gate composed by the highly n-doped silicon substrate and its thermally grown oxide. While the carbon nanotube is an intrinsic semiconductor, able of accumulating both holes and electrons, the transistor shows a p-type behavior instead of ambipolar transport.This has been reported often in literature [52, 62]. The origin of this p-type behavior is attributed to several factors. The workfunction of the gold electrodes lies closer to the

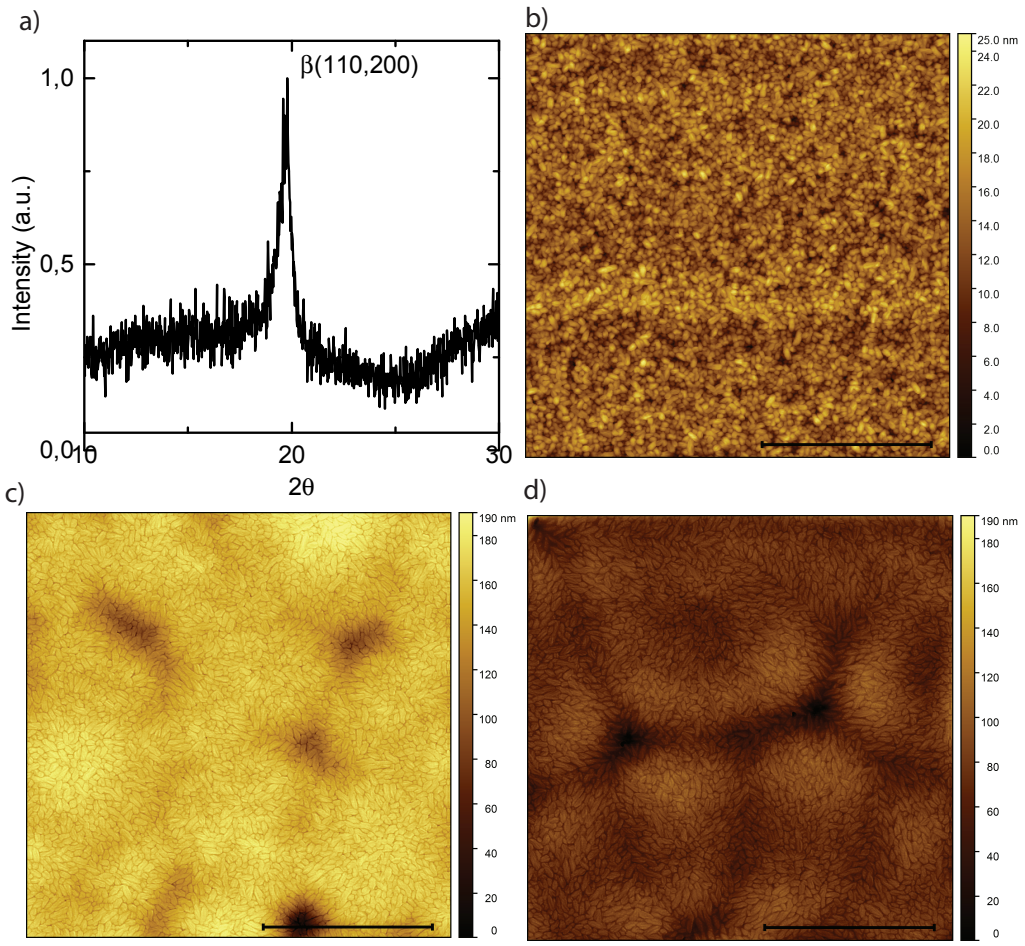


FIGURE 4.1: a)XRD spectrum of P(VDF-TrFE) on silicon. Annealed for 1 hours at 140°. The characteristic peak at 19.7°C is due to the (200) and (110) planes. b)AFM image of P(VDF-TrFE) on top of a carbon nanotube transistor annealed for 1 hour at 140°C. The rod shaped grain structure is similar to what is reported in the literature[30, 59]. The spincoated layer here has an average thickness of 70nm measured using profilometry. c) The spincoated layer here has an average thickness of 280nm measured using profilometry. High surface roughness and furthermore deep pinholes, responsible for shorting the dielectric when a gate electrode is applied, are observed. d) On top of the structure a thin layer of PMMA is deposited. The PMMA layer is conformal to the underneath grain structure. Still a large surface roughness is observed with numerous pinholes, however the leakage is significantly reduced with this addtional layer. The scale bar on all AFM images corresponds to 2μm

valence band of the nanotubes, therefore making it easier to inject holes[63]. Furthermore the wrapping polythiophene polymer strongly interacts with the nanotube[64] and therefore could have an electron acceptor behavior, since the polythiophene itself is also a p-type material.

The transfer curve shown in figure 4.3 confirms this p-type behavior besides

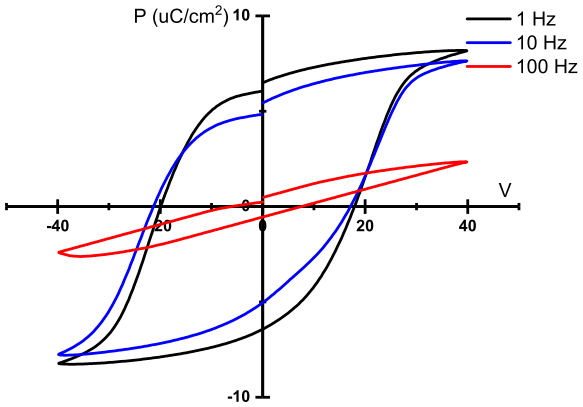


FIGURE 4.2: P-E Hysteresis loop of ITO/P(VDF-TrFE)/PMMA/Al capacitors, the coercive voltage is approxiametly 18V.

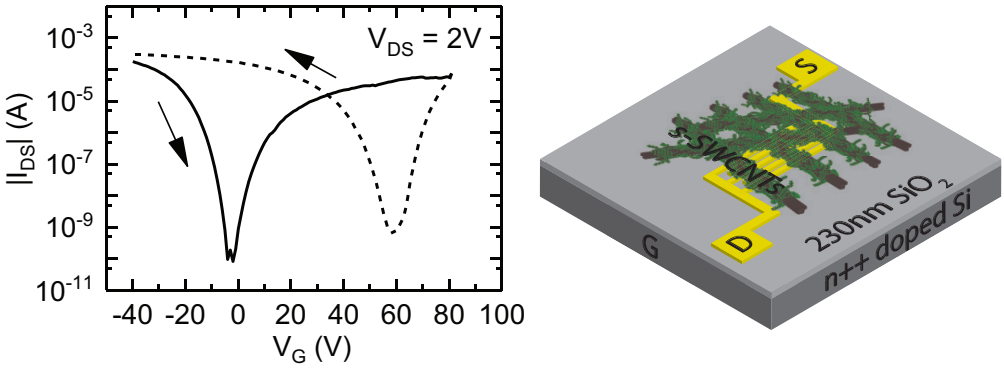


FIGURE 4.3: Transfer curve of s-SWCNT transistor using the n++ doped bottom gate below the SiO_2 dielectric. A counter clockwise hysteresis loop is observed.

showing large counter-clock-wise hysteresis. This hysteresis has been investigated in the past and is often attributed to a surface-bound water layer[65, 66] and the injection of screening charges into trap states[56, 67], these traps are especially formed due to the silanol groups on the surface of the silicon oxide[67]. As mentioned in the experimental section, in this work the nanotube ink is annealed at 160°C in a nitrogene environment. We therefore expect the later to be contributing the most to this effect.

In the past a similar device structure, as used in this research, has shown to counter and/or control the observed hysteresis by using the ferroelectricity of P(VDF-TrFE)[57, 68]. These works focus on counter balancing the hysteresis but not on creating non-volatile memories using the ferroelectricity of P(VDF-TrFE) as a functional dielectric. In figure 4.4 the transfer curve of the transistor top-gated with P(VDF-TrFE) is shown. Again here we see clear p-type behavior, however we observe a clockwise hysteresis loop. This observation is attributed to the switching of the ferroelectric layer. After a negative gate voltage is applied that exceeds the coercive field of the ferroelectric layer, the polarization will be in the upward direction. This

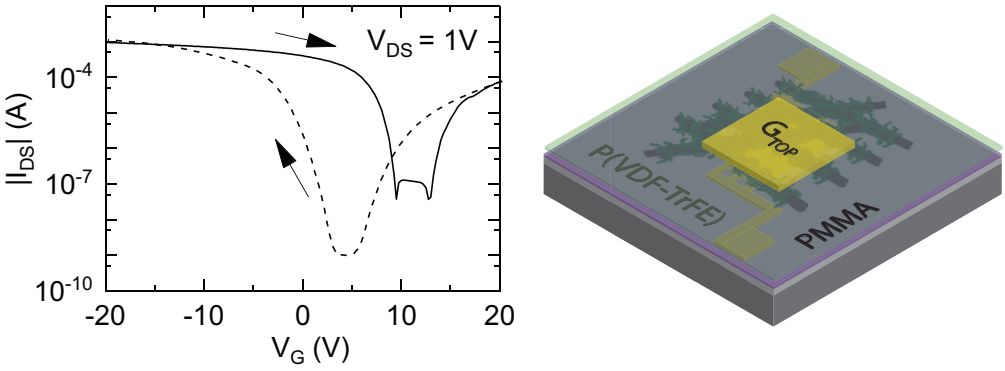
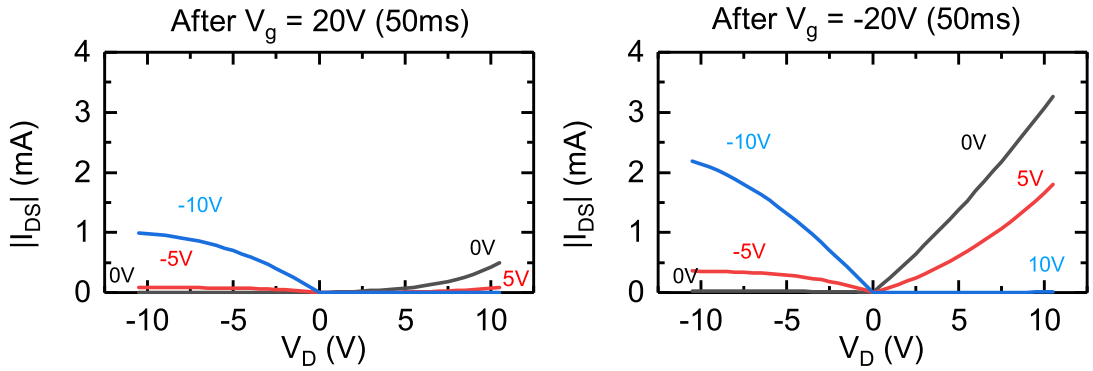


FIGURE 4.4: Transfer curve of the memory device using P(VDF-TrFE) and a small layer of PMMA as gate dielectric, the active layer is s-SWCNTs. Clockwise hysteresis is obsevered, attributed to the ferro-electric switching of the P(VDF-TrFE) polymer.



(A) (B)

FIGURE 4.5: A)Output curve of FeFET after a positive pulse of -20V of 50ms on the gate, effectively turning "Off" the memory element. B)Output curve of FeFET after a negative pulse of -20V of 50ms on the gate, effectively turning "On" the memory element.

polarization state induces extra holes in the channel and therefore increases the hole current. In the downward polarization, after a positive gate voltage exceeding the coercive voltage, the polarization state induces extra negative charge in the channel, suppressing the hole current and inducing a higher electron current at a lower gate voltage. In the transfer characteristics this results in a shift in the threshold voltage between the forward and backward scan.

To shine more light on the output characteristics of the device, two output curves are measured right after poling of the P(VDF-TrFE). The gate voltages used in the output curve stay below the coercive field and will therefore not depolarize the layer, nor switch the polarization state. The results in figures 4.5a and 4.5b exhibit a clear difference between negative poling and positive poling in the output characteristics. The poling is done by using a $\pm$20V pulse of 50ms. After the negative pulse we see a larger current due to the extra holes in the channel induced by the P(VDF-TrFE). While the output is suppressed after a positive pulse. The injection of charge carriers also appears to increase in the ON-state of the device.

Since the device exhibits p-type behavior, a negative voltage is used to switch

the memory element in the ON-state and a positive voltage to switch to the OFF-state. In figure 4.6a the device is switched 200 times and read out with a low read voltage of 1V. The delay between switch and read out is 20 seconds. The results show two conductance levels with an On/Off ratio over an order of magnitude. To show the non-volatile character the states are also measured over the course of a few hours, figure 4.6b shows that the states are stable for at least several hours. The small changes we see especially in the off state are attributed to charge trapping effects between the s-SWCNT/P(VDF-TrFE) interface and/or charge traps on the s-SWCNT/SiO_2 interface, which are discussed in more detail in section 4.5

As can be seen in figure 4.4 the memory window is larger when the read-out is performed at a higher voltage than at $V_G = 0V$. The maximum is reached around $V_G = 5V$, so to increase the On/Off ratio of this device the read-out is also performed at $V_G = 5V$. The results, shown in figure 4.6c, show a large On/Off ratio of 10^4 when reading the device with $V_G = 5V$ and $V_DS = 1V$. Here we also observe memory retention of at least an hour.

4.5 FeFET with P(VDF-TrFE)/s-SWCNT as artificial synapse

This section should be considered as a separate section, which relates this chapter to the topic of this thesis. The original idea was to create non-volatile memory with more than two conductance states by partially polarizing the P(VDF-TrFE) for use as an artificial synapse in a neuromorphic circuit as described in chapter 2. In this research it has been observed that it is very difficult to achieve more than two different non-volatile conductance states within the P(VDF-TrFE)/s-SWCNT MFS-FET (Metal-ferroelectric-semiconductor) structure.

In the literature it is described that the switching kinetics of P(VDF-TrFE) are dependent on the thickness of the layer. It was found that the switching time drastically increases when the layer is made with a thickness below a 100nm[30]. The idea was that these longer switching times would enable us to partially polarize the P(VDF-TrFE) by going over the coercive field with pulses which are smaller than the full switching time. This was reported in the literature by Kim et al[59], where the switching time was increased by incorporating PMMA in the P(VDF-TrFE) layer. A complete overview of the switching kinetics is not yet given in literature, however a lot of research on the switching behavior has been done by Zhao et al[61] and Hu et al[28]. In the first month(s) of our investigation we tried to make thin layers of P(VDF-TrFE) using the spincoating technique. Quickly it was found that these layers had a lot of pinholes and were shorted after the evaporation of a contact on the layer. Eventually this made measuring these (ultra) thin layers impossible. There is some research that shows it is possible to make defect free and thin layers of P(VDF-TrFE), however often the Langmuir-Blodgett technique is used for these layers[69, 70]. Eventually layers were made of a thickness around 250-300nm, with an extra PMMA layer, to reduce the leakage. These layers still had some defects, but could function as a dielectric. Unfortunately this did not make it possible to measure these longer switching times up to seconds[30].

One of the other major problems that we observed is the probable existence of charge traps on the P(VDF-TrFE)/s-SWCNT interface. The hysteresis observed in

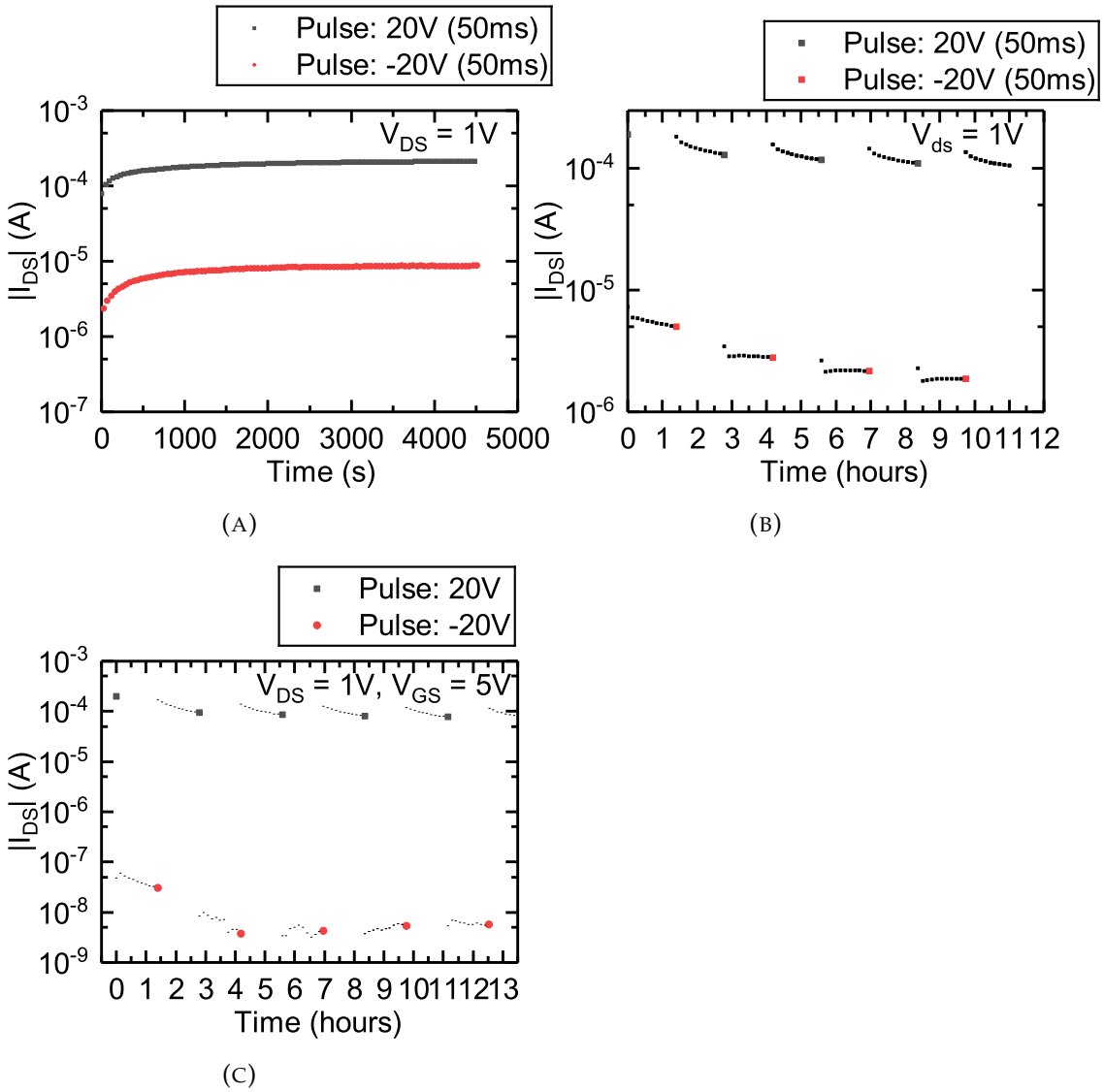
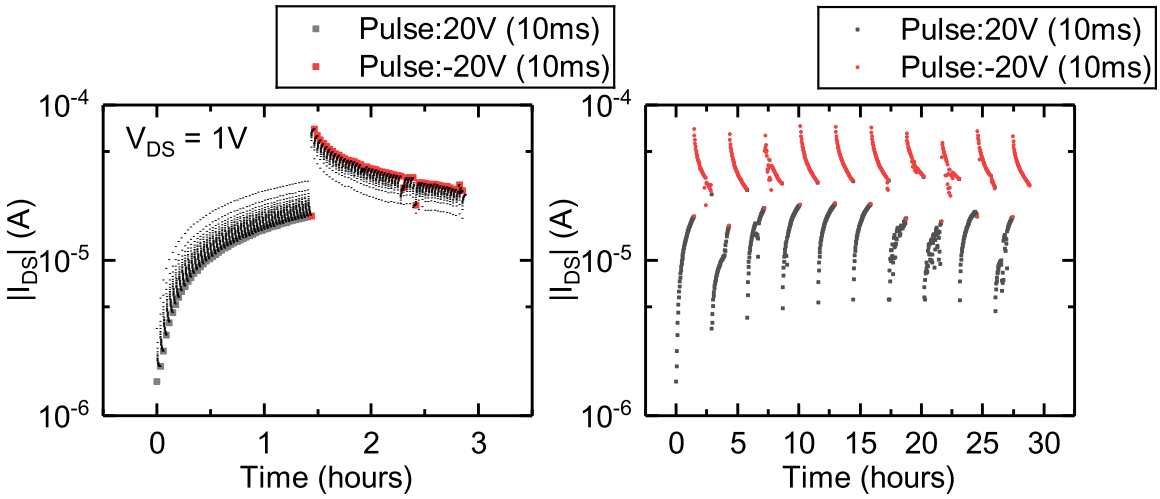


FIGURE 4.6: A) Consecutive switching of the P(VDF-TrFE) layer by applying 50ms pulses of ±20V. Every measurement point is a measurement of the conductance of the channel at a 1V source-drain bias right before the pulse. Between all pulses there is a delay of 20seconds. B) Long term memory behavior is observed, with retention time over 1 hour C) Reading the conductance with an applied gate voltage of 5V shows a very large On/Off ratio of 10^4. As becomes clear from figure 4.4, the largest difference in current between the forward and the backward scan in the transfer curve is at approximately $V_G = 5V$

the transfer characteristics is in a previous section partially attributed to the ferroelectric switching of the P(VDF-TrFE), however we also observed some other hysteresis effects which could be caused by charge traps. A measurement that sheds light on these charge traps is shown in figure 4.7a. It should be noted that the measurement here is done at a different sample than the other measurements. Also at this time 10ms pulses were used instead of 50ms, since they appeared to have the same effect. Later on in the research 50ms pulses were used since they appeared to give rise to more reliable results. The figure shows that switching of the layer works



(A) (B)

FIGURE 4.7: A) A measurement showing that applying pulses of the same polarity only gives a memory switch after the first pulse. All consecutive pulses of similair polarity give rise to opposite behaviour. The black dots represent measurements of the conductance at $V_{DS} = 1V$, whereas the grey and red dots represent a measurement of the conductance after the specified pulse is applied. B) Is a continued measurement of Figure A, here only the red and grey dots are represented. It shows that the behaviour is repeatable.

after the first pulse, however a second pulse which is fired after the first pulse has the opposite result.

As can be seen in figure 4.7a the memory is initially in the Off-state. A pulse is fired which would normally be used to set the memory in the Off-state. At this moment we see the conductance increasing instead of decreasing. After the pulse the conductance decreases over time when no pulse is being applied. This effect happens with every sequential pulse. It appears that after each of the pulses some charges are trapped/detrapped and gradually released/trapped. When a pulse is applied with opposite polarity, i.e. a negative voltage, we expect that the memory will be shifted on. This is indeed the case, however after this pulse more pulses with the same polarity cause again the same effect. Figure 4.7a is part of a larger measurement shown in figure 4.7b, where it becomes clear that charge trapping effect is very repeatable.

This trapping effects makes it difficult to create multiple non-volatile memory states, because we are dealing with more than one memory effects (this effect however appears to be volatile over the course of minutes to hours). One of the possible solutions that could be investigated is to use a thin $PMMA/Al_xO_x$ layer, since using this as a gate dielectric causes no hysteresis as can be seen in figure 4.8. The PMMA is deposited here by using a spincoating technique, whereas the Al_xO_x layer is deposited using atomic layer deposition (ALD)]

In the literature there is to our knowledge only one report on using the ferroelectric properties of P(VDF-TrFE) as artificial synapse[59]. In this paper the semiconductor IGZO is used with a 9nm-thick Al_2O_3 protection layer and a P(VDF-TrFE)-PMMA blend. Some efforts have been made to repeat these results by using s-SWCNT as active channel, however these trials did not result in noteworthy results.

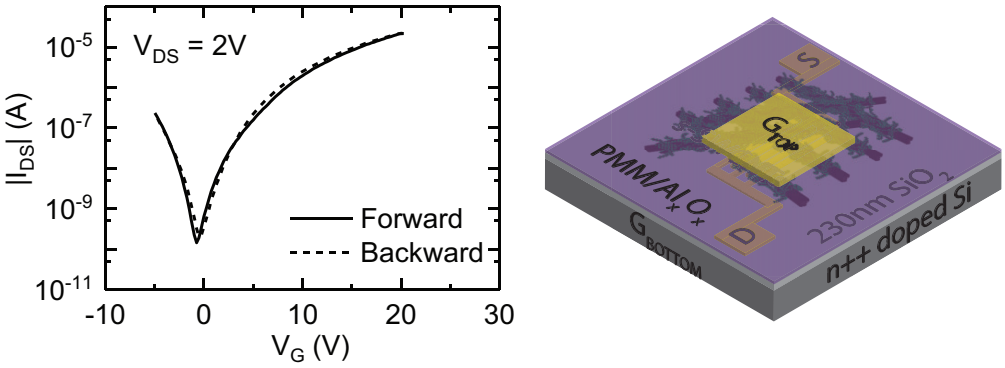


FIGURE 4.8: Transfer curve of s-SWCNT transistor with a thin layer of PMMA and ALD grown Al_2O_3 showing no hysteresis.

The lack of literature support on this topic make us conclude that the ferroelectric properties of P(VDF-TrFE) in a MFS-FeFET structure do not appear promising for the fabrication of artificial synapse in combination with any semiconducting material. The use of P(VDF-TrFE) or any of its derivatives are however successfully demonstrated as host matrix for ion gels, that can be deposited as gate dielectric on a transistor structure, which in turn can be used as artificial synapse [50, 71, 72].

4.6 Conclusion and perspectives

To conclude we were able to create non-volatile one-transistor type memory using polymer-wrapped s-SWCNT and P(VDF-TrFE) with a high On/Off ratio of 10^4 a low read voltage of 1V, data retention of $> 10^4 s$ and a write/read endurance >200cycles. These findings show that the use of s-SWCNT in combination with P(VDF-TrFE) have potential to be used as memory elements in future cheap, flexible and disposable electronics. The low read-out voltage could enable low power consumption, while the use of solution processable materials makes possible devices easy to fabricate and cheap.

To prove that these configurations can indeed be made flexible, the same configuration should be fabricated on a flexible substrate. At this time the maximum temperature in the fabrication process that is reached is 160°C, which could be reduced to 140°C. This temperature should not be any problem for fabricating the devices on flexible substrates. It could even be thought of transferring the structure to paper substrates which has been shown in the past with carbon nanotubes[73].

In future works the gate read voltage of 5V could be omitted by doping the channel with a molecular dopant. In previous work, we showed that by using molecular doping it is possible to shift the threshold of the s-SWCNT transistor towards more n-type behavior. Effectively we could tune the threshold so that there is no need of applying a gate read voltage.

Lastly, the observed charge trapping behavior mentioned in section 4.5 could be omitted by using a small PMMA layer between the s-SWCNT and the P(VDF-TrFE). However if the charge traps between the SiO_2 and the s-SWCNT turn out to cause the observed hysteresis, even while this interface is not actively gated during

read/write operations.

Chapter 5

Utilizing hysteresis effects in s-SWCNT transistors for artificial synaptic transistors

5.1 Introduction

The human brain can be described as a complex biological computer, capable of computing in massive parallelism with a very low power consumption of only 20W[1]. Neurons play a special role in the brain and communicate with each other through synapses. The brain consists out of approximately 10^{12} neurons and 10^{15} synapses and has a computational power that goes beyond the limit of anything artificially created by humans[74, 75]. Hardware implementations that could emulate the functions of synapses are necessary to realize computers capable of competing with the brain in specific tasks like pattern recognition and (unsupervised)learning tasks.

One of the most important properties that an artificial synapse should posses is the ability to be switched in different conductance states. Preferably the artificial synapse can continuously be tuned in different non-volatile conductance states, effectively creating analog memory. An often mentioned two-terminal circuit element that could emulate the working of a synapse is called a memristor[76]. Reports on creating these two-terminal memristors that could work as artificial synapse include the use of phase-change materials[47, 77], conductive bridge type memories[78], resistive random access devices[79] and electrochemical reactions[80–82]. Besides two-terminal devices there are other three-terminal devices proposed that could mimic the functioning of a synapse. These devices, often referred to as memistor[76] or synaptic transistors and could omit the additional circuits necessary to realize learning and functionality in two-terminal devices[76]. Three terminal devices that have been reported to have synaptic properties utilize electrochemical gating and/or ion diffusion[72, 74, 83, 84], charge trapping memory[85] and floating gate structures[73, 86] among others. Other attempts to mimic brain-like behavior has been demonstrated by using conventional CMOS technology[35, 87]. CMOS technology has also been used to design spiking synapses using silicon transistors, however these approaches often require a large number of transistor[88, 89]. Different types of synaptic behavior has been demonstrated in these works such as spike-time-dependent-plasticity (STDP), Paired Pulse Facilitation (PPF) and spike-duration-dependent-plasticity (SDDP).

In the field of neuromorphic computing carbon nanotubes have been used in several synaptic devices as well. It has been reported that the combination of carbon nanotubes with light-active polymers can result in synaptic behavior[90–92]. Also investigations where carbon nanotubes are gated by electrolytes have shown short and long-term plasticity[84, 93, 94]. Furthermore charge trapping[85] and floating gate structures[73] have been shown to already perform well in simulated neuromorphic circuits.

In this work we demonstrate synaptic behavior by utilizing the hysteresis effects often reported in single-walled carbon nanotube (s-SWCNT) transistors on SiO_2 substrates[56, 95, 96]. The main goal was to show that we can achieve different conductance states within the CNTFET. We compare hysteresis mechanisms in ambient air and in an inert environment to see how the hysteresis in both environments affect the synaptic properties. This study should be considered as a proof of concept study. In the next chapter, chapter 6, suggestions are given to fully characterize this device and implement learning rules to show the full potential of it.

5.2 Experimental section

Preperation of SWCNT Ink

The HiPCO nanotubes used in this research were purchased from Unidyn Inc. The wrapping polymer P3DDT was synthesized via a GRIM method by our collaborator prof U. Scherf. The polymer is solubilized in toluene and stirred for one hour at 80°C. Sequentially the solution is stirred overnight at 50°C to guarantee full solubilization. The nanotubes are added at a weight ratio of 1:2 with respect to the polymer and are sonicated for 2 hours at 78W to promote proper dispersion and wrapping in the solution. During sonication the temperature is decreased from 25°C to 16°C. After the ultrasonication the dispersion is centrifuged at 30 000rpm for 1 hour(Beckman Coulter Optima XE-90) to remove all bundles of metallic nanotubes and other heavy weight impurities. To purify the solution from excess polymer, the supernatant, obtained as described above, is centrifuged again at 55 000rpm for 5h. The semiconducting nanotubes which were initially individualized are now bundled in a pellet in the bottom of the centrifugation tube, whereas the excess polymer is still solubilized in the supernatant. The enriched pellet is now re-dispersed in o-xylene.

Fabrication and Characterization of Synaptic Transistors

Field effect transistors are made on pre-patterned silicon substrates (Fraunhofer Institute for Photonic Microsystems) with thermally grown SiO_2 of 230nm. The pre-patterned source/drain electrodes consist out of 10nm ITO/30nm Au electrodes made in interdigitated channels of 2mm width and 20μ m to 2.5μ m length. In this research all results make use of the 20μ m length channels, unless specified otherwise. The s-SWCNT ink is deposited by using a blade coating technique (Zehtner ZAA 2300 Automatic film applicator coater), the blade speed is 3mm/s and the surface is heated to 70°C. Afterwards the film is annealed at 160°for 1 hour.

5.3 Hysteresis in CNTFETs

The origin of hysteresis in the transfer characteristics of CNTFETs has been attributed to a variety of reasons. Among them have been mentioned, a surface-bound water

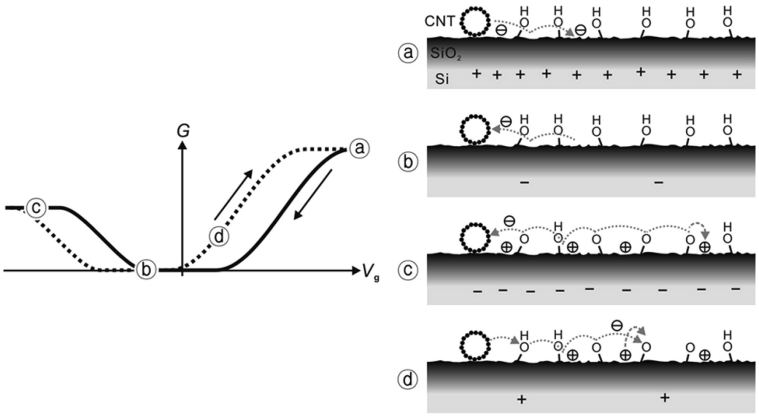


FIGURE 5.1: Schematic of proposed model of charge trapping by silanol groups on the dielectric surface: (a) A positive gate is applied, electrons are induced in the channel. (b)Trapped electrons screen the gate reducing the drain current (c) Protons are released from the OH-groups, suppressing the hole current in the backward sweep (d) Net trapped positive charges increase the electron current and caused a negative shift of the threshold (i.e. to the left). The circled plus marks represent protons released from surface silanol groups. Image adapted from:[67].

layer[65, 66] on top of the nanotubes and it has been shown in several experiments that traps caused by water molecules can be divided in two types of traps. Traps of type-1 are caused by weakly adsorbed water molecules that are easily removed by a vacuum treatment, whereas, type-2 traps are formed by water forming hydrogen bonds with dangling silanol groups and are therefore more difficult to remove[85]. Secondly also the injection of screening charges into traps on the oxide surface[56, 67, 97] has been mentioned as a possible hysteresis source by several researchers. These trapped charges effectively screen the gate, giving rise to increased or decreased charge inversion with respect to the expected charge inversion for an applied gate bias. The mentioned traps can be split in two sources: interface traps and surface traps. Where the former arise on the interface of the SWCNT and the dielectric and the later on the dielectrics surface. These traps are especially formed due to the silanol groups on the surface of the silicon oxide[67]. A proposed model by Lee et al[67] on the trapping of net charges due to silanol groups is schematically explained in figure 5.1. A remark should be made that it is very difficult to distinguish between the traps on the interface between dielectric and the nanotube and on the surface of the dielectric where no nanotube is present. All traps show the same counterclockwise hysteresis effect, where electrons are trapped at positive gate voltages and released at negative voltages. Research by Park et al[56] shows that a proposed physics-based model, which assumes that the surface traps have slower de-trapping kinetics than interface traps, shows similarities with measured data.

The observed hysteresis in the transfer characteristics of CNTFETs has been noted to be a major obstacle for implementing carbon nanotubes in digital logic systems[66]. A variety of methods has been investigated to reduce or completely remove this hysteresis, examples include the use of PMMA and other polymers[57, 68, 96], surrounding the nanotubes with oxides to have gate-all-around-geometries[95] and suspending the nanotubes above the substrate[98] . Despite the observation of a low controllability in this hysteresis, due to the fact that it depends on a variety of

environmental parameters, the hysteresis characteristics have been exploited by several researchers to create memory elements [55, 99–101]. Some researchers show that non-volatile memories using SWCNT can have retention time up to 7 days in ambient conditions without any extra control measures[85]. Furthermore it was shown that the non-volatility of the memory can be improved by depositing on the nanotubes a PMMA layer containing a low concentration of water[102]. Using such a layer allowed to obtain multi-state memory retention times up to 10^4s.

5.4 Results

5.4.1 Hysteresis in transfer characteristics

In figure 5.2 the transfer characteristics of a HiPCO:P3DDT CNTFET in an inert environment are shown. As reported often in literature, the transfer-characteristics show a dominant p-type transport. Secondly a large clockwise hysteresis loop is observed. The exact root of this hysteresis is difficult to find, since all mentioned mechanisms contribute to this effect. It could however be stated that the hysteresis caused by oxygen and water is minimized in the curves shown in figure 5.2, with respect to the transfer curve shown in 5.3, which are measured in ambient conditions. The hysteresis here is also very pronounced and counterclockwise, however there is a clear difference with respect to the measurements performed in inert conditions. The main difference between these measurements is in the electron current. In ambient conditions the electron transport is fully suppressed even at gate voltages of up to 80V. This behavior has been shown by other authors as well[103], and it has been postulated by Aguirre et al that electrons in this case are initially transfered from the nanotube channel to an aqueous oxygen electrochemical redox-couple, which is present on the sample when put in ambient conditions. The reaction that takes place in this hypothesis is,

$$O_2 + 4H^+ + 4e^- \rightleftharpoons 2H_2O. \tag{5.1}$$

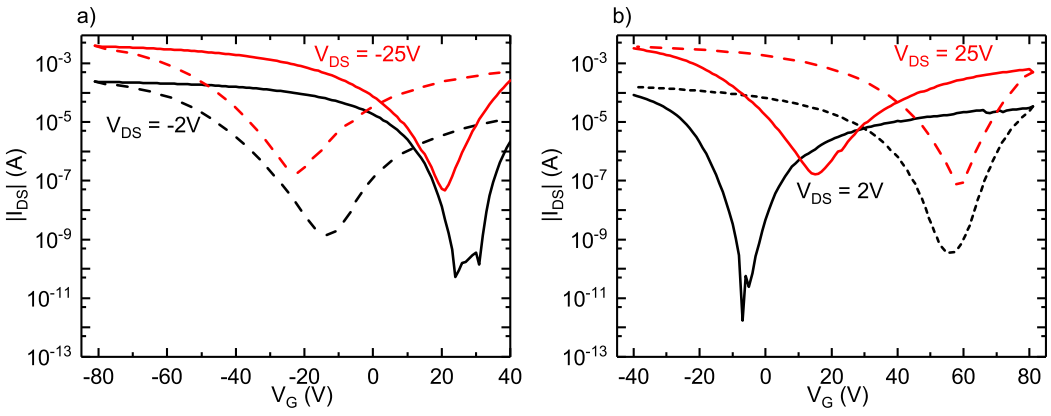


FIGURE 5.2: Transfer characteristics of HiPCO:P3DDT CNTFET in inert environment a) Gate votlages from 40V to -80V to characterize hole transport, the solid line is the forward scan, while the dotted line is the backward scan. b) Sweep from -40V to 80V to characterize electron transport,the black line is forward scan, while the dotted line is the backward scan.

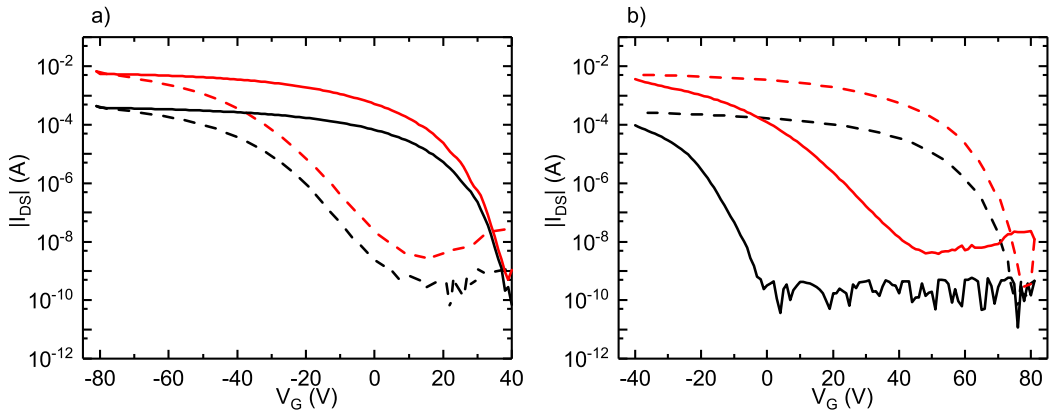


FIGURE 5.3: Transfer characteristics of HiPCO:P3DDT CNTFET. in ambient conditions a) Gate votlages from 40V to -80V to characterize hole transport, the black line is the forward scan, while the dotted line is the backward scan. b) Sweep from -40V to 80V to characterize electron transport,the black line is forward scan, while the dotted line is the backward scan.

When a positive gate is applied to the CNTFET in ambient conditions. The chemical potential of the nanotube increases with respect to its intrinsic chemical potential. This increase in chemical potential will shift the redox reaction 5.1 towards the right-hand side and thus promotes the transfer of electrons towards the water adsorbates, effectively suppressing electron transport through the channel.

5.4.2 Synaptic behavior

Inert characterization

The main goal of this investigation was to see whether multiple conductance states could be achieved by applying pulses to the gate electrode of a CNTFET. First the device in inert environment is characterized. First the transient response during the pulsing of the gate electrode is measured, more information regarding these transient measurements can be found in appendix A. In figure 5.4a a pulse of 25V and duration of 50ms is applied to the gate electrode while keeping a fixed bias of $V_{DS} = 1V$. Due to the p-type characteristics of the device the main charge carriers at this bias are holes. However during every positive gate pulse electrons are induced in the channel. As mentioned in the previous section, these electrons are gradually trapped due to the various trapping mechanisms and therefore we observe a small decrease in the current during the pulse, shown clearly in the inset of figure 5.4. When the pulse ends we observe an increased current with respect to the the current before the pulse, this increased hole current is caused by trapped electrons screening the gate. The (hole-)current here drops fast implying that a lot of the electrons are quickly de-trapped. However as it can be seen in figure 5.4 the conductance is still modulated after 30 seconds implying a long term effect. To show that at this gate voltage this effect is time dependent (implying that longer and/or multiple pulses can access new trap states) a 2 second pulse is applied and the transient response is measured. In figure 5.7b it is observed that a 2 second pulses does not show any saturation in the electron trapping during the pulse, i.e. trapping occurs

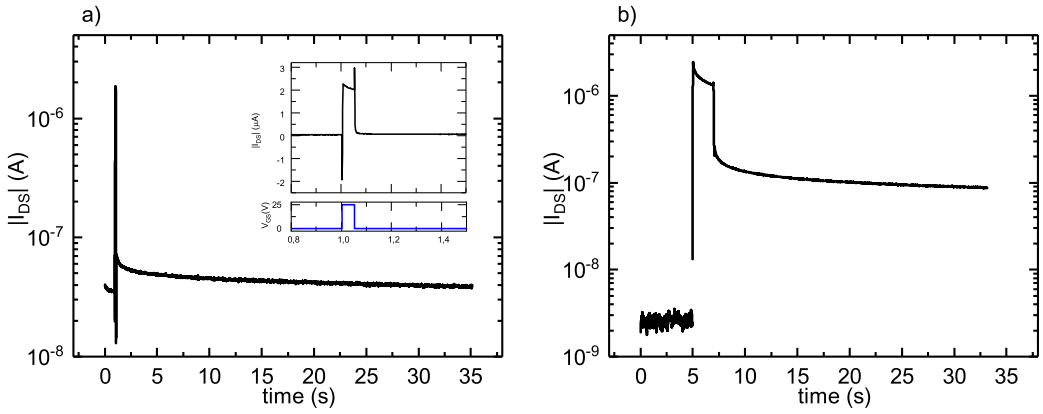


FIGURE 5.4: a)Transient behavior of the source-drain current when a 25V pulse of 50ms is applied to the gate. $V_{DS} = 1V$ during the entire measurement. The inset shows a close up indicating electron trapping during the pulse. b) The same pulse is applied only for 2 seconds showing even clearer the electron trapping during the pulse. This measurement is performed on a HiPCO:P3DDT transistor in inert environment

during the full 2 seconds. This is contrasting with measurements performed by Park et al[56], where the trapping appears to saturate after 100ms. Our observation implies that longer pulses cause more trapping and therefore a stronger potentiation of the synaptic device. This effect could be used when implementing Spike-duration-dependent-plasticity (SDDP).

To further show the ability of our device to be switched in different conductance states we apply a pulse train of 2000 positive pulses, while measuring the conductance a second after the pulse is applied. More information regarding these measurements can be found in appendix A. After 2000 consecutive potentiation pulses the synaptic transistor is depressed by applying 2000 negative pulses. The results show the plasticity of the device and its ability to cycle through different conductance states and shows the behavior of an analog memory spanning several orders of magnitude.

To investigate how non-volatile our device is, we performed a measurement where we set our device in a high conductance state by applying 2000 consecutive pulses, analogously to the measurement performed in figure 5.5. After these pulses we stop pulsing and measure the conductance overtime for 1000s. The results, summarized in figure 5.6, show that the memory slowly falls back if it is set to a very high conductance state. The reached states can therefore not be considered as fully non-volatile, but do show a memory effect.

Ambient characterization

By Kim et al it was shown that measurements in ambient conditions could provide non-volatile behavior[85]. Therefore the same measurements are also performed in ambient conditions. Figure 5.7a shows the same transient measurements as in figure 5.4. As can be observed in the graph the device operates in a resistivity regime which is over an order of magnitude lower, meaning that the drain current is higher. This behaviour could be determined by pre-measurement conditions, it could also

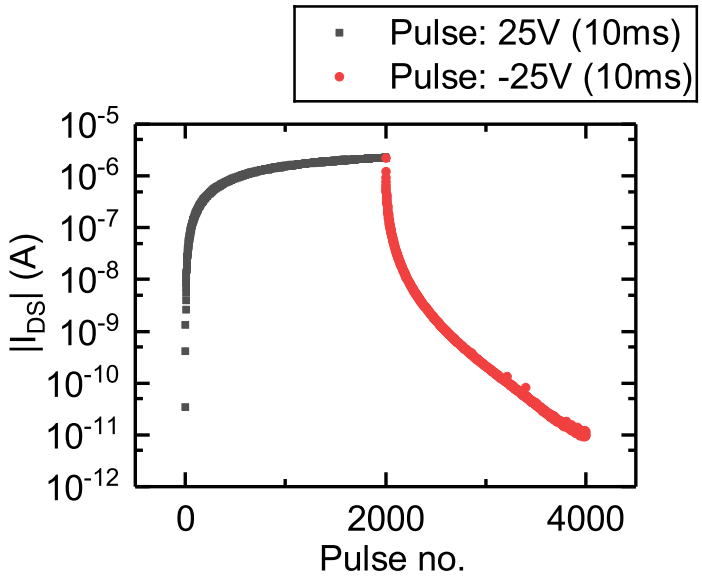


FIGURE 5.5: Measurement of the conductance after a pulse train of 2000 consecutive pulses (25V) of 10ms duration are applied, these are followed by 2000 negative pulses (-25V). One dot represents a current measurement at V_{DS} = 1V directly followed by a pulse and a 1.5 second delay before the next current measurement takes place. This measurement is performed on a HiPCO:P3DDT Transistor in inert environment

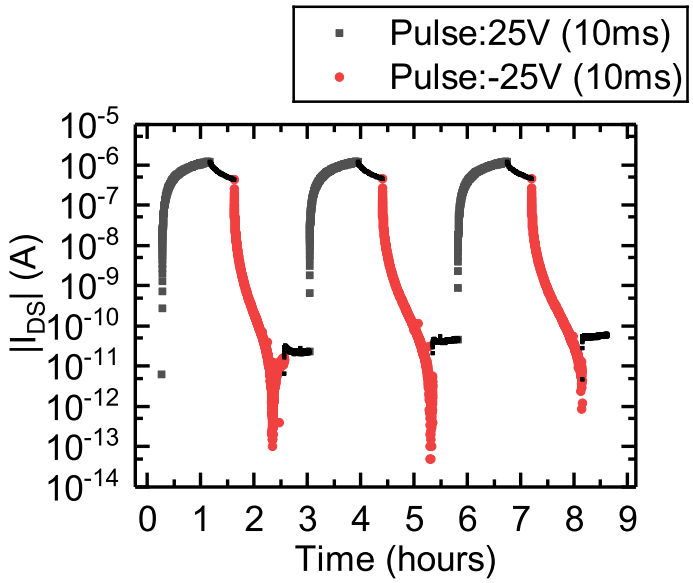


FIGURE 5.6: Measurement of conductance after a pulse train of 2000 consecutive pulses (25V) with a duration of 10ms are applied, these are followed by 1500 seconds of delay before 2000 negative pulses (-25V) are applied. The red and grey dots represents a current measurement at V_{DS} = 1V directly followed by a pulse and a 1.5 second delay before the next current measurement takes place. The black dots are current measurements at $V_{DS} = 1V$ without any pulse applied. This measurement is performed on a HiPCO:P3DDT transistor in inert environment

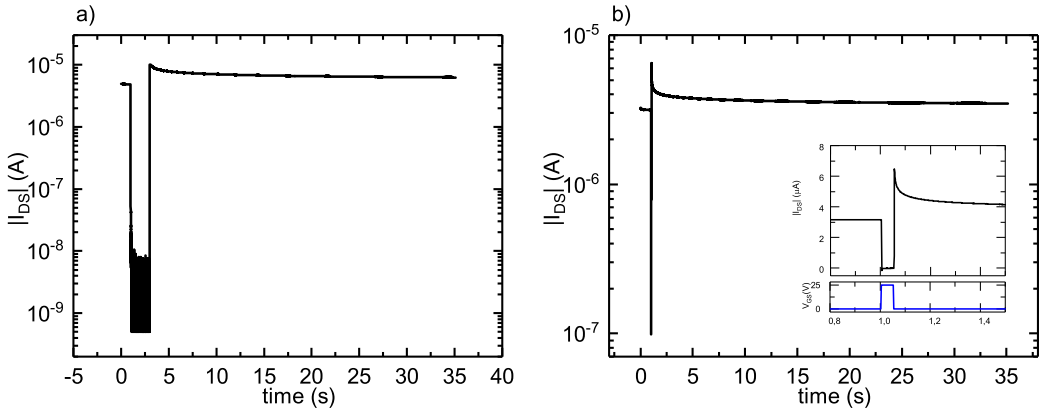


FIGURE 5.7: a)Transient behavior on the source-drain current when a 25V pulse of 50ms duration is applied to the gate. $V_{DS} = 1V$ during the entire measurement. The inset shows a close up indicating almost no electron current during the pulse. b) a 2 seconds pulse shows even clearer that there is no current at all during the pulse. The noise indicates that we are measuring near the machine precision. The current during the pulse is negative. The measurement was done on a HiPCO:P3DDT transistor in ambient environment

be caused by the difference in threshold. The threshold voltage is higher for devices in ambient condition than for devices in ambient condition. This can also be clearly observed in the transfer characteristics in figure 5.2 and 5.3. This implies that at $V_G = 0V$ the hole current in devices measured in ambient condition is higher than for devices in inert conditions.

From the measurement of figure 5.7 it is clear that during the pulse there is almost no current. This is in line with observations in figure 5.3, where it was observed that the electron current is fully suppressed. Furthermore also here we see that the device is potentiated after a 50ms pulse of 25V, similarly the conductance modulation is observable for a longer time.

Figure 5.8 shows the earlier described pulse train measurement performed on the device in ambient conditions. It becomes clear that the lowest conductance state that is reached is significantly higher than with the inert device. Therefore the modulation ratio is only slightly over an order of magnitude during this measurement, whereas the inert sample in inert conditions showed a modulation over several orders of magnitude. This does not mean that the number of traps is necessary lower nor higher, since the device is switched in a lower resistivity regime the dynamic range is lower. Measurements with a fixed positive gate read voltage could shine light on the total achievable dynamic range within the devices in ambient conditions. Since this would switch the device to a higher resistivity regime. However in this research we chose not to use any gate reading voltage since the reading itself could influence the conductance state and therefore modify the measurement making the comparison not correct.

The stability measurement that was performed on a sample in inert atmosphere is performed on the sample in ambient condition as well. This results show a very similar behavior. In 1000seconds the current drops over several states. Which shows

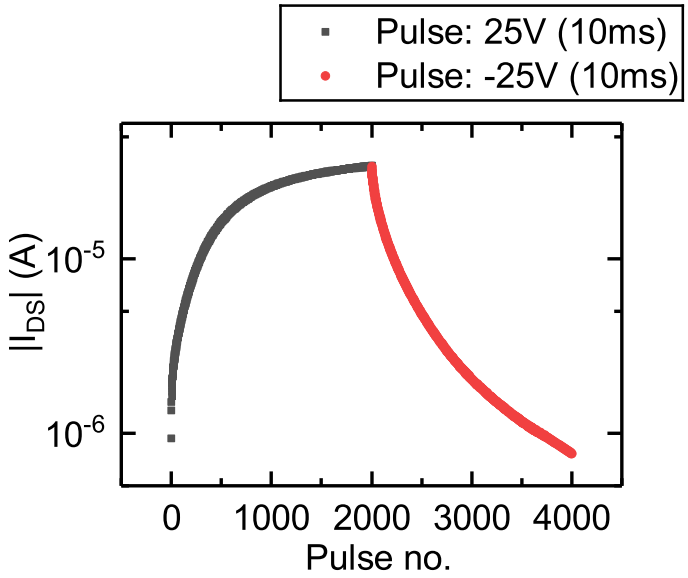


FIGURE 5.8: Measurement of conductance after a pulse train of 2000 consecutive pulses (25V) of 10ms duraiton are applied, followed by 2000 negative pulses (-25V). One dot represents a current measurement at V_{DS} = 1V directly followed by a pulse and a 1.5 second delay before the next current measurement takes place. This measurement is performed on a HiPCO:P3DDT transistor in ambient conditions.

that the highest conducting state in this measurement is also not fully non-volatile.

5.5 Discussion

Stability and non-volatility

It is difficult to determine exactly how stable the different states should be in order to call them non-volatile. In mammals it was attempted to measure how long long-term potentiation lasts[104]. Here three different types of long-term memory are defined: LTP1, LTP2 and LTP3 which have a very broad range of lifetimes ranging from minutes to weeks to years. In this research we used a 1 second waiting time in between 10ms pulses, which is already two orders of magnitude difference. While this could indicate a long term effect, the most important parameter here would be the average modulation frequency of the synapse, which should be larger than 1Hz to conclude that this system has a viable retention time. Also it is important to notice that future neuromorphic chips could perform the learning tasks very efficiently, so that after learning the whole device can be mapped to a different type of long-term memory and the weights can be used in neural networks in conventional computers.

The results of figure 5.4 and figure 5.7 show conductance modulation over a time period longer than 30s, implying that states could be non-volatile up to half a minute. Here it should be noted that all states have a stability of more than 30 seconds.It is very likely that very high conductance states, with a lot electrons trapped, have a lower stability than this state. Eventually the discussion whether the retention times are long enough should be held with the designer of the artificial neural network. Depending on a specific application it could be that retention times should be longer or are already long enough.

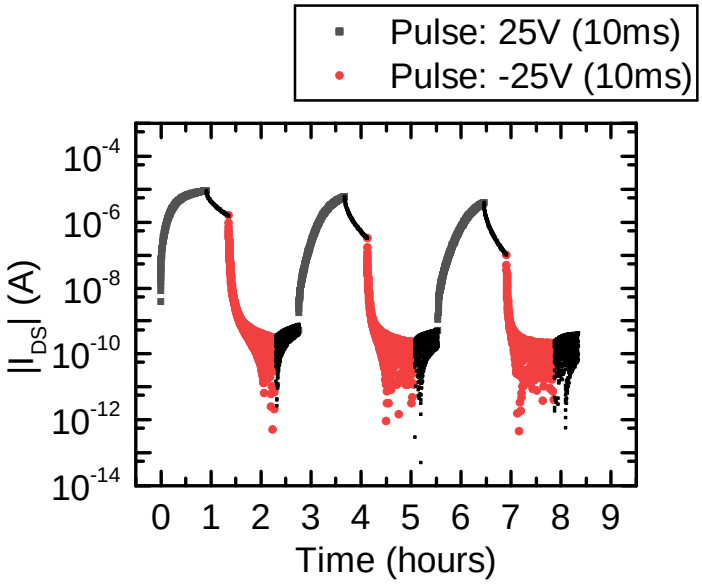


FIGURE 5.9: Measurement of conductance after a pulse train of 2000 consecutive pulses (25V) of 10ms duration are applied, followed by 2000 seconds of delay before 2000 negative pulses (-25V) are applied. The red and grey dots represents a current measurement at V_{DS} = 1V directly followed by a pulse and a 1.5 second delay before the next current measurement takes place. The black dots are current measurements at $V_{DS} = 1V$ without any pulse applied. This measurement is performed on a HiPCO:P3DDT transistor in ambient conditions

The research where it was indicated that ambient behavior gave full non-volatile results up to 7 days[85], only shows this for a single potentiation and modulation pulse. In this research we investigate the stability of the states after applying 2000 pulses which could be at the boundary of our dynamic reach. This in turn could make theses states less stable. In real life devices the boundary states will probably be the most unstable.

Ambient or Inert conditions

The comparison between the device in ambient and inert conditions still lacks a lot of data to draw strong conclusions. Due to the variety of mechanism at play it is difficult to determine which trapping mechanism is the best to exploit in a synaptic device. It should be mentioned that both devices do not show full non-volatile behavior. Furthermore better studies on the energy-levels of the traps could indicate whether we are exploiting all trapping mechanisms efficiently. With the new made software it could be tried to replicate measurements that map the energy levels and density of all traps[56]. Suggestions for further research on this are given in the next chapter.

Non-linearity

It is not directly clear from the measurements how strong the non-linearity in updating the weights is in both devices. When figures 5.8 and 5.5 are plotted in a linear scale in figure 5.10a and 5.10b, it becomes clear that the inert device has a stronger

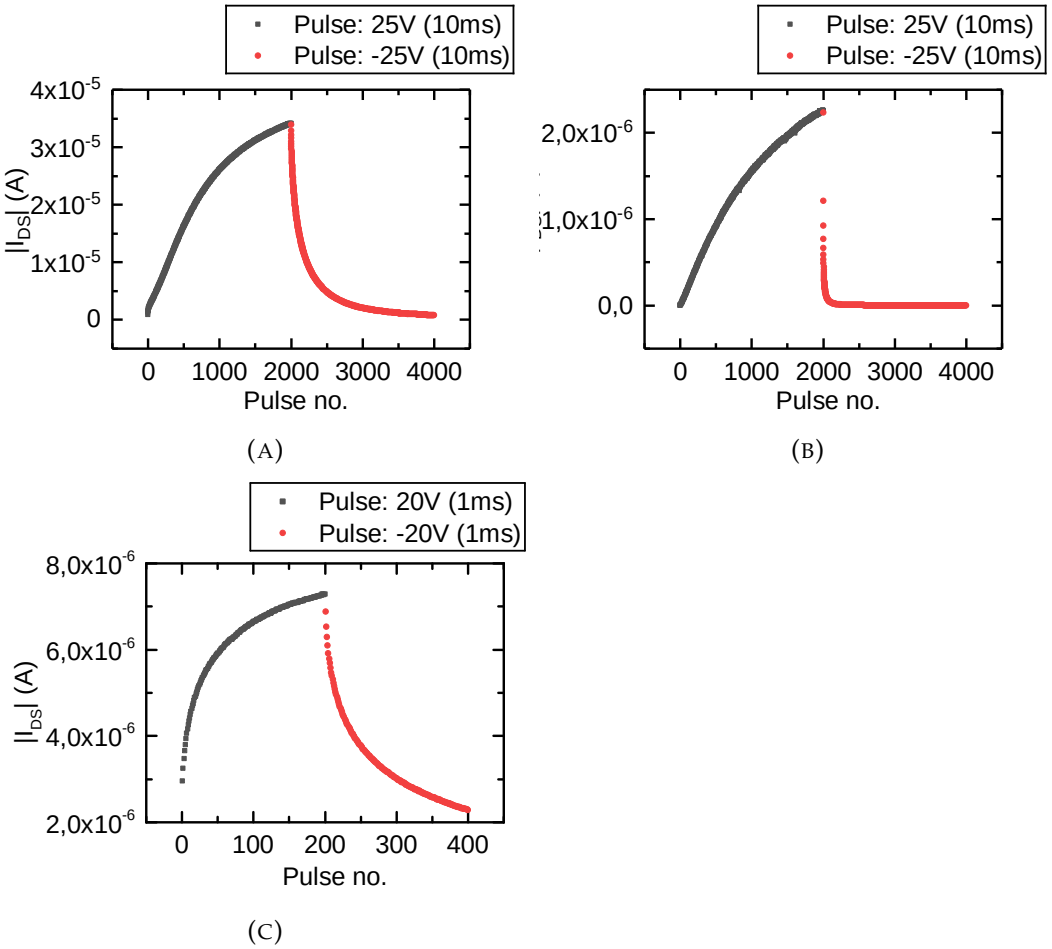


FIGURE 5.10: Linear response to pulse trains on HiPCO:P3DDT transistor. a) Ambient environment, same as figure 5.8. b) inert environment, same as figure 5.5. c) A measurement on a HiPCO:P3DDT Transistor in an inert environment, channel length is here $10\mu m$, whereas a) and b) are $20\mu m$, furthermore the pulse voltage is 20V and the width is 1ms. Also the number of pulses is lower, which could influence the linearity.

non-linearity than the device measured in ambient conditions. It should be investigated whether this is solvable by applying asymmetric pulses(i.e. a difference in absolute voltage between the potentiation and depression pulse)

The choice for 25volt pulses was based on literature reports[85], where we scaled the pulse voltage to our dielectric thickness. Since this is still ongoing research, the pulse scheme should be optimized to investigate whether we can increase the linearity.

In figure 5.10c a measurement is plotted which is performed on a different sample in an inert environment, this sample is made with the same HiPCO:P3DDT solution. Here two-hundred 20V pulses of only 1ms are applied. Here we see a stronger linearity due to the lower amount of pulses. This measurement is performed on a $10\mu m$ channel and therefore the current is significantly larger than the measurements reported on figure 5.10b. This measurement shows an increased linearity, lower pulse voltage and faster switching time showing the potential that this device has. The dynamic range however is lower and is approximately 2.5. The linearity increase is mainly caused by the lower amount of pulses used.

Transient measurements

It was difficult to measure the transient during negative pulses. This is due to the fact that at a gate voltage of $-25V$ the measurement equipment has to switch from range which causes a large disturbance in the measurement. In future research it could be possible to measure the transient response during a negative pulse by manually setting the range to higher settings. Depending on the magnitude of the current when no pulse is applied it could be possible to measure this transient properly. More on this problem can be found in appendix A

Pre-measurement conditions

Since we are working with memistive devices not every consecutive measurement will give a similar results, since current conductance states are dependent on previous measurements. Therefore it could be thought of to implement a resetting sequence for setting the device in a certain state right before every measurement. Especially when exact values should be extracted from voltage or spike width dependent measurements this has to be taken into account. Suggestions for this are given in chapter 6.

5.6 Conclusion and perspective

We were able to utilize the hysteresis in s-SWCNT to create a device ,which to some degree, mimics desired synaptic behavior. Devices in an ambient environment and in an inert environment both give rise to synaptic behavior exploiting different hysteresis mechanisms. Both devices show non-volatile LTP and LTD, with retention times over 30s. Using some extra device architecture, explained in the next chapter, we could measure STDP-behavior, showing that the device could also learn by implementing learning rules. The device shows potential due to the high dynamic range that is achieved. However a lot of investigations have to be done to fully characterize its potential.

At this point in time it is not possible to draw strong conclusions regarding the difference between the devices measured in inert and ambient conditions. Further research could indicate which trapping mechanisms are dominant and give rise to non-volatile behavior. Secondly modulating the pulse width and voltage could shine more light on the possibilities with these devices. By modulating the pulse voltage we could address traps which have different energy levels that could result in more stable trapping. In the future it can also be considered to create more traps by adding a layer which improves trapping or by using floating gate structures, which are also used by other researchers[73]. In the last chapter of this thesis suggestions are given for further investigations.

Chapter 6

Conclusion and Future investigations

In this work we showed that polymer-wrapped s-SWCNT show great potential in memory and neuromorphic applications. In chapter 4 we demonstrate that combining polymer-wrapped s-SWCNT with other solution processable materials can result in the fabrication of high-end memory devices with High On/Off ratio. The use of the ferroelectric polymer P(VDF-TrFE), which is already commercially available, makes the devices interesting for commercial applications. The device is promising for the fabrication of low-cost, flexible and disposable memory elements.

In chapter 5 t he main goal was to demonstrate how exploiting hysteresis effects in s-SWCNT can make the nanotubes suitable for neuromorphic applications. While already being showed before by other groups[85], in this work we demonstrate the enormous potential that these devices have. The dynamic range that is achieved is tremendous and gives a large freedom in using different pulse schemes. Where we still need to fully understand all mechanisms at play, it is clear that there is limited non-volatility.

6.1 Future research - Binary memory

To fully show the potential of our binary memory device of chapter 4 it is necessary to perform some other experiments. First to get rid of the charge trapping effects it is possible to try to incorporate a thin PMMA layer between the s-SWCNT and the P(VDF-TrFE). A proper solvent to spincoat the P(VDF-TrFE) could be cyclohexanone, which will be less aggressive on the PMMA, since using MEK will dissolve the thin PMMA layer.

Implementing our structure on flexible and disposable substrates could make our device competitive with other state-of-the-art ferroelectric memories. Therefore in further research work should be performed on flexible substrate, also bending radius experiments should investigate whether the P(VDF-TrFE) layer will be able to cope with severe bending. Transferring to paper substrates could also be interesting for RFID purposes.

6.2 Future research - Synaptic transistors

Here we give an overview on how this investigation can be continued and how we can improve and optimize the devices and the characterization of them.

Dielectric

The current dielectric, 230nm SiO_2, is too thick to work with, since it requires high gate voltages to induce charges that can get trapped. As mentioned the dielectric plays a significant role in the charge trapping, therefore other dielectric could be investigated like Al_xO_x or HfO_x, which we are able to grow with ALD. Besides these dielectric have a higher dielectric constant and therefore require a lower operating voltage. Furthermore when we are designing the dielectric ourselves, this also opens up the possibility of patterned gating. This patterned gating will reduce the gate leakage and makes it possible to address specific transistors instead of modulating the conductance of the full substrate.

Characterization

One of the first suggestions in terms of future characterization is the choice of proper pre-measurement conditions. One of the suggestions we have here is to use a resetting pulse train. The resetting pulse train would entail the application of alternating potentiation and depression pulses fired continuously. After a while the devices reaches a state where each potentiation pulse has the same effect as the depression pulse, which could be a proper symmetric state to start our measurements. Other suggestions would be sweeping the gate to a relatively high voltage and back, which could detrap/trap all possible trap sites and give a repeatable start point for all measurements.

The current device is characterized by mainly using pulses of 25V. The dependence on pulse voltage and width should be checked by sweeping both parameters using proper pre-measurement conditions. Also with different pulse voltages combined with the newly setup measurement equipment it is possible to make transient measurement to quantify the number of charge traps. A technique called Pulse-Time-Domain Measurement, developed by Park et al[56] could shine light on the trap density and the energy levels of the traps.

To spatially determine where charges are trapped, EFM (Electrostatic force microscopy) could be performed. In the past other researchers used this technique to detect charges on single nanotubes[105], or charges withing carbon nanotube rings[106]. Whether these trapped charges will be visible in CNT Networks has not been investigated.

Spike-Time-Dependent-Plasticity (STDP)

Implementing learning rules is crucial for artificial synapses. One of the suggestions we make here is to fabricate a small external circuit which enables the device to learn. In figure 6.1 we suggest that by using two normal transistors we can control the voltage applied to the source and gate in a way that could be suitable for neuromorphic applications using an Integrate-and-fire neuron. The blue transistor labeled

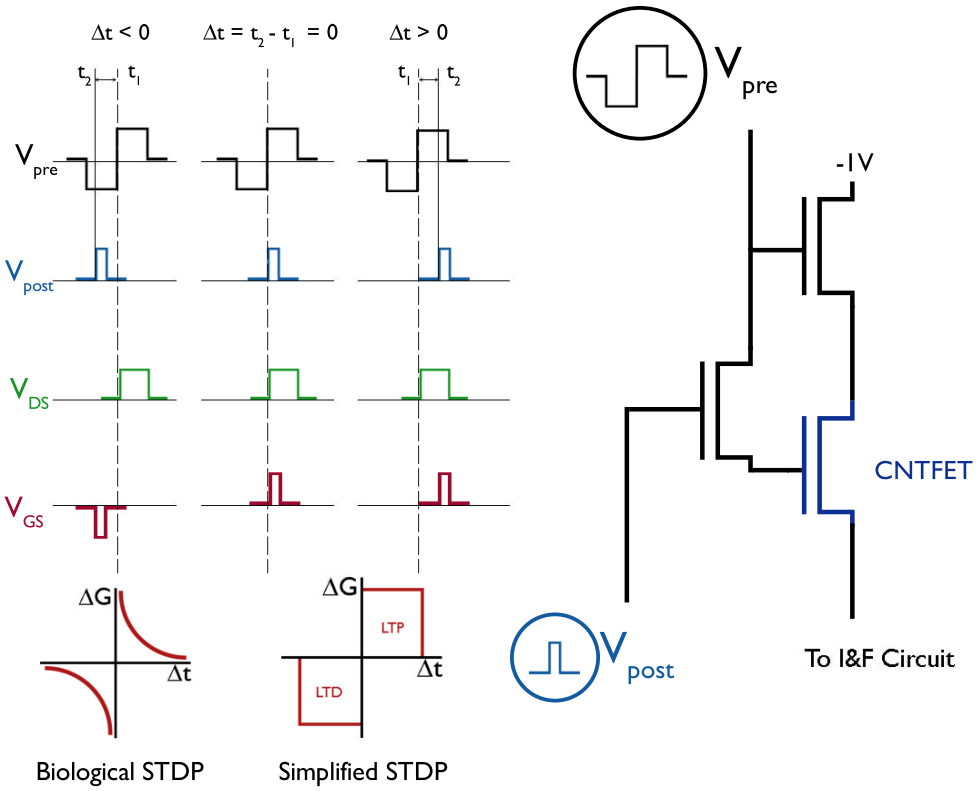


FIGURE 6.1: Potential setup for the implementation of simplified STDP. On the left side three situations are shown. First a situation where the post-spike is fired before the pre-spike is fired. Secondly a situation where both are fired simultaneously and lastly a situation where the post-spike is fired after the pre-spike is fired. The time difference between post- and pre-spike is given by $\Delta t = t_2 - t_1$, as can be seen in the figure.

CNTFET represents our synaptic transistor where the source is connected to the Integrate and Fire circuit. The two other transistors that are shown, are plain unipolar enhancement mode transistors. The transistor connected to the drain of the CNTFET gated by the pre-synaptic spike controls the current flow through our artificial synapse, whereas the other transistors controls the voltage applied to the gate of our CNTFET. The pre-synaptic spike consists of a square wave, where the negative part will be the depression pulse and the positive part the potentiation pulse. The post synaptic spike consists out of a single positive pulse.

In the left part of the figure, three situations are shown. Δt represents the time between the pre-synaptic pulse and the post-synaptic pulse. To be precise the time is taken from the center of the pre-synaptic pulse to the start of the post-synaptic pulse. In the first situation the post-synaptic spike precedes the pre-synaptic spike, implying that our CNTFET should be depressed according to the rules of STDP. The post-synaptic spike controls when the pre-synaptic spike is applied to the gate of the CNTFET, i.e. during the post-spike the pre-synaptic spike is applied to the gate of the CNTFET. So if $\Delta t < 0$ the negative part of the pre-synaptic pulse is applied to the gate of the CNTFET, causing a depression of the synaptic weight. On the other hand if $\Delta t > 0$, the positive part of the pre-synaptic pulse is applied to the gate of

the CNTFET and the channel is potentiated. Furthermore, due to the transistor connected to the source of the CNTFET, only current runs through the device during the positive part of the pre-synaptic spike. This current is integrated by the I&F neuron circuit, which handles the generation of the Post-synaptic spike when the I&F circuit is supposed to fire.

This suggestion could show simplified STDP-behavior, as can be seen in the bottom left of figure 6.1. To mimic the biological STDP even more, the pre-synaptic pulse could be shaped as a sawtooth pulse. This would reduce $|V_{GS}|$ when Δt becomes larger, which could show a stronger potentiation/depression depending on the absolute value of V_{GS}.

Appendix A

Measurement software

In this work a lot of time has been dedicated towards setting up measurement software and investigating what we could measure using our current setups and whether we needed additional hardware and/or software. In this process a lot of different measurement programs were made and continuously improved. In this section an overview is given on how we decided to measure certain parameters and how the measurement software was made. Furthermore it gives some insights in for future users.

Since we are working with devices that can be cycled through conductance states by applying different pulses, it is necessary to have a pulse generator. For this we used the output channels of the Agilent E5270B. The machine does not posses an official wavefunction generator, however, gives the user the possibility to do pulsed measurements, meaning that a single pulse can be applied during which a single current or voltage measurement can be performed. The pulse widths of this generator go from $500\mu s$ up to $2s$ and voltages up to $40V$. To control this function generator we used the PyVisa library[107] on a standard Windows pc running Python. The current program makes separate threads of which one controls the instrument and the other the plotting which is done by using MatPlotlib. The timing of measurements is done in Python, which makes implementation and live plotting easier, however does incorporate some timing inaccuracy. In the transient measurements the internal clocks of the Agilent machines are used, since these would be more reliable than the Windows timing.

Main software

The main software that we designed is made for measuring three terminal devices where the conductance over two terminals is measured (e.g. source and drain terminals), whereas pulses are applied on the third terminal (e.g. gate terminal). All measurements perform two different pulses, in the software referred to as up-pulses and down-pulses. First a sequence of up-pulses is applied, of which the user can choose the width, height, delay and number of pulses, and then the down-pulses are applied which have the same control. The number of times this is performed can be chosen by the user.

Since we want to measure the conductance before and after every pulse, every measurement cycle performs one current read (which has its own read delay of $0.5s$),

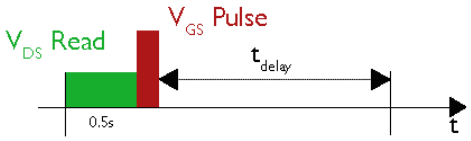


FIGURE A.1: Schematic overview of one measurement cycle.

then the pulse is applied, after which another delay can be implemented. Schematically this is shown in figure A.1. In earlier versions of the software the source drain voltage is applied during the full measurement, now it is possible to choose to either do this or to implement a read voltage after which the voltage is set to 0V. The read time of 0.5s as indicated in the figure, can be adjusted, however we never fully investigated what would happen if we do not implement any read delay. At first it seemed reasonable to wait for some time, since we could not measure the transient behavior yet. However it could be the case that applying such low voltages (1V in our measurements), would already stabilize the current output very fast, which makes the implementation of this read delay unnecessary.

Furthermore with some small adjustments in the software it is possible to turn off terminals when there is no voltage applied., This is not yet a full feature, but can be implemented relatively easy. This makes the device floating as if there would be a relay connected which disconnects the terminal when no pulse or read voltage is applied. Especially in the case of ionic systems, where synaptic behavior is mimicked by ion migration this could reduce the diffusion of ions when no measurements are performed.

Besides implementing a read delay and a wait delay between each measurements, of which the later is the indicated by t_{delay} in the figure. It is also possible to do "stability-measurements". These measurements happen between every sequence of up-pulses and down-pulses but can also be implemented during the sequences. These stability measurements perform conductance measurement over a specified time while no pulses are being fired. This gives the ability to check the volatility of certain states in our synaptic devices.

Transient software

One of the large struggles in this research was not being able to perform high speed, high accuracy and low current measurements. Being able to this could shine more light on the transient switching behavior of our devices, indicating which mechanisms are at play.

In a first stage we investigated the possibility to design a setup where we use an oscilloscope with high sampling frequency together with a function generator and a transimpedance amplifier to measure both low currents and have a high sampling rate. We did not pursue this due to the cost in terms of time involved. Other options for these type of measurements include the purchase of high end Pulsed-Measurement-units (PMU's) which specialize in transient pulse measurements.

In a later stage of the research we did implemented a way of performing transient measurements, where we reached a reasonable sampling rate while measuring low currents with high accuracy. This means that we can measure the conductance of the transistor during the application of a pulse on the gate. The method used both an Agilent E5270B as well as an Agilent E5260A as schematically shown in figure A.2.

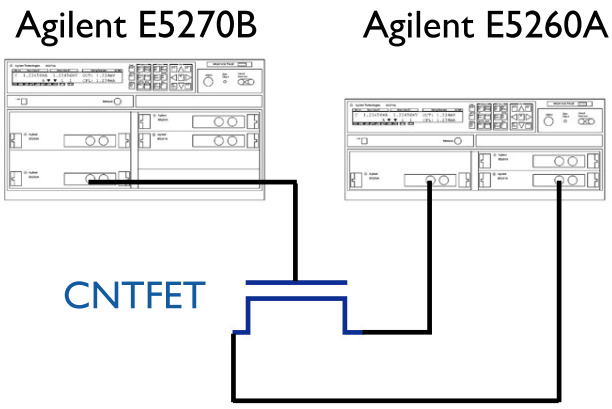


FIGURE A.2

We were able to reach a sampling frequency of around 1kHz. It should be noted that there were also measurements where we saw that the sampling frequency went up to approximately 1.65kHZ. This seemed to have to do with resetting the machine right before each measurement in combination with taking a shorter total measurement. We did not fully confirm the reason of this increased sampling rate and are also not able to reliable reach this sampling rate.

It appears that the following measures we took strongly improved this sampling frequency:

- Using the build-in programming memory, instead of sending commands via PyVISA continuously.
- Turning off the display of the Agilent
- Turning off all channels besides the measured channel
- Fixing the measurement range to the compliance value.
- Storing all measurement data in the machine buffer instead of requesting it after each measurement

By using the build in program memory of the Agilent E5260A we drastically increased the sampling rate, since no time is lost in communicating between computer and machine. Furthermore, using a programming memory on the Agilent E5270B gives the ability to precisely time a specific pulse train for example for measuring Paired Pulse Facilitation (PPF), since precise delays can be implemented in the programming memory as well.

Fixing the measurement range to the compliance value is somewhat non trivial. During each high-speed spot measurement the machine expects a measurement range, if no range is specified the range is set to auto-ranging. Auto-ranging obviously reduces the measurement speed and especially kills the speed when a range switch has to be performed. We observed that range switches can take up to 15ms, making large gaps in transient pulse measurements. Furthermore forcing a specific range also kills the speed to some extent. If however a range is specified which is equal or higher to the compliance, the compliance value will act as measurement range. This increased the speed, while sacrificing a bit of range. By omitting auto ranging the maximum current expected determines the current resolution of the

measurements. A table can be found in the manual that determines the maximum accuracy you can reach with a specific range. In general there is a factor of $2 \cdot 10^4$ between the lowest value and the highest value you can measure, implying that the transient measurement range is slightly over 4 orders of magnitude.

Bibliography

(1) Fischetti, M. *Scientific American* **2011**, *305*, 104.

(2) Ho1, V. M.; Lee, J.-A.; Martin, K. C. *Science* **2011**, *334*, 623–628.

(3) Dresselhaus, M.; Dresselhaus, G; Jorio, A *Annual Review of Materials Research* **2004**, *34*, 247–278.

(4) Gomulya, W.; Costanzo, G. D.; De Carvalho, E. J.; Bisri, S. Z.; Derenskyi, V.; Fritsch, M.; Fröhlich, N.; Allard, S.; Gordiichuk, P.; Herrmann, A.; Marrink, S. J.; Dos Santos, M. C.; Scherf, U.; Loi, M. A. *Advanced Materials* **2013**, *25*, 2948–2956.

(5) Cao, Q.; Rogers, J. A. *Advanced Materials* **2009**, *21*, 29–53.

(6) Shulaker, M. M.; Hills, G.; Patil, N.; Wei, H.; Chen, H.-Y.; Wong, H.-S. P.; Mitra, S. *Nature* **2013**, *501*, DOI: 10.1038/nature12502.

(7) Derenskyi, V.; Gomulya, W.; Talsma, W.; Salazar-Rios, J. M.; Fritsch, M.; Nirmalraj, P.; Riel, H.; Allard, S.; Scherf, U.; Loi, M. A. *Advanced Materials* **2017**, *29*, DOI: 10.1002/adma.201606757.

(8) Arora, N.; Sharma, N. N. *Diamond and Related Materials* **2014**, *50*, 135–150.

(9) Kumar, M.; Ando, Y. *Journal of Nanoscience and Nanotechnology* **2010**, *10*, 3739–3758.

(10) Guo, T.; Nikolaev, P.; Thess, A.; Colbert, D. T.; Smalley, R. E. *Chemical Physics Letters* **1995**, *243*, 49–54.

(11) Arnold, M. S.; Stupp, S. I.; Hersam, M. C. *Nano Letters* **2005**, *5*, 713–718.

(12) Ghosh, S.; Bachilo, S. M.; Weisman, R. B. **2010**, DOI: 10.1038/NNANO.2010.68.

(13) Liu, H.; Nishide, D.; Tanaka, T.; Kataura, H. *Nature Communications* **2011**, *2*, 308–309.

(14) Salazar-Rios, J. M.; Talsma, W.; Derenskyi, V.; Gomulya, W.; Keller, T.; Fritsch, M.; Kowalski, S.; Preis, E.; Wang, M.; Allard, S.; Bazan, G. C.; Scherf, U.; dos Santos, M. C.; Loi, M. A. *Small Methods* **2018**, *1700335*, 1700335.

(15) Joselevich, E.; Lieber, C. M. *Nano Letters* **2002**, *2*, 1137–1141.

(16) Nish, A.; Hwang, J.-Y.; Doig, J.; Nicholas, R. J. *Nature Nanotechnology* **2007**, *2*, 640–646.

(17) Derenskyi, V. Y., *Polymer-wrapped carbon nanotubes for high performance field effect transistors*, 2017, p 128.

(18) Gomulya, W., *Selecting Semiconducting Single- Walled Carbon Nanotubes by Polymer Wrapping Mechanism and Performances Widianta Gomulya*, 2015.

(19) Tans, S.; Verschueren, A.; Dekker, C. *Nature* **1998**, *672*, 669–672.

(20) White, C. T.; Todorov, T. N. *Nature* **1998**, *393*, 240–241.

(21) Snow, E. S.; Novak, J. P.; Campbell, P. M.; Park, D. *Applied Physics Letters* **2003**, *82*, 2145–2147.

(22) Li, J.; Liu, Y.; Zhang, Y.; Cai, H. L.; Xiong, R. G. *Physical Chemistry Chemical Physics* **2013**, *15*, 20786–20796.

(23) Wang, J.; Wei, N.; Wang, F.; Wu, C.; Li, S. *Polymer Bulletin* **2012**, *68*, 2285–2297.

(24) Zheng, Y.; Ni, G. X.; Toh, C. T.; Tan, C. Y.; Yao, K.; ??zyilmaz, B. *Physical Review Letters* **2010**, *105*, 5–8.

(25) Jung, S. W.; Lee, J. K.; Kim, Y. S.; Yoon, S. M.; You, I. K.; Yu, B. G.; Noh, Y. Y. *Current Applied Physics* **2010**, *10*, e58–e61.

(26) Kawai, H. *Japan Jurnal Applied Physics* **1969**, 975.

(27) Glass, A. M.; McFee, J. H.; Bergman, J. G. *Journal of Applied Physics* **1971**, *42*, 5219–5222.

(28) Hu, W. J.; Juo, D.-M.; You, L.; Wang, J.; Chen, Y.-C.; Chu, Y.-H.; Wu, T. *Scientific Reports* **2015**, *4*, 4772.

(29) Fukada, E.; Furukawa, T. *Ultrasonics* **1981**, *19*, 31–39.

(30) Duo Mao, B. E. G.; Quevedo-Lopez, M. A. *Herbicides, Physiology of Action, and Safety* **2015**, 253–274.

(31) Xu, H.; Shanthi, G.; Bharti, V.; Zhang, Q. M.; Ramotowski, T. *Macromolecules* **2000**, *33*, 4125–4131.

(32) Schuman, C. D.; Potok, T. E.; Patton, R. M.; Birdwell, J. D.; Dean, M. E.; Rose, G. S.; Plank, J. S. **2017**, 1–88.

(33) Schuller, I. K.; Stevens, R. *Neuromorphic Computing : From Materials to Systems Architecture Report of a Roundtable Convened to Consider Neuromorphic Computing*; tech. rep.; 2015, p 40.

(34) Backus, J. *Communications of the ACM* **1978**, *21*, 613–641.

(35) Merolla, P. A. et al. *Sciencemag.Org* **2014**, *345*, 668–673.

(36) Bliss, T. V.; Collingridge, G. L. *Nature* **1993**, *361*, 31–39.

(37) Whitlock Heynen, A. J., Shuler, M. G., Bear, M. F., J. R. *Science* **2006**, *313*, 1093–1097.

(38) Attwell, D; Laughlin, S. B. *Journal of Cerebral Blood Flow & Metabolism* **2001**, *21*, 1133–1145.

(39) Kandel ER; Schwartz, J. J.; Jessell, T. T. M.; Eric Kandel, James Schwartz, T. J.; Kandel, E. R.; Schwartz, J. J.; Jessell, T. T. M. *Neurology* **2000**, 1414.

(40) Burr, G. W. et al. *Advances in Physics: X* **2017**, *2*, 89–124.

(41) Drachman, D. A. *Neurology* **2005**, *64*, 2004–2005.

(42) Su, F.; Yuan, P.; Wang, Y.; Zhang, C. *Protein and Cell* **2016**, *7*, 735–748.

(43) Hebb, D. O., *The Organization of Behavior: A Neurophysiological Theory*, 1949, p 335.

(44) Buonomato, D. V.; Merzenich, M. M., *Chapter 7 Temporal information processing: A computational role for paired-pulse facilitation and slow inhibition*; C; Elsevier Masson SAS: 1997; Vol. 121, pp 129–139.

(45) Kong, L.-a.; Sun, J.; Qian, C.; Fu, Y.; Wang, J.; Yang, J.; Gao, Y. *Organic Electronics* **2017**, *47*, 126–132.

(46) Schulz, P. E.; Cook, E. P.; Johnston, D *The Journal of neuroscience : the official journal of the Society for Neuroscience* **1994**, *14*, 5325–5337.

(47) Eryilmaz, S. B.; Kuzum, D.; Jeyasingh, R.; Kim, S. B.; BrightSky, M.; Lam, C.; Philip Wong, H. S. *Frontiers in Neuroscience* **2014**, *8*, 1–11.

(48) Bi, G. Q.; Poo, M. M. *The Journal of neuroscience : the official journal of the Society for Neuroscience* **1998**, *18*, 10464–10472.

(49) Dan, Y. *Physiological Reviews* **2006**, *86*, 1033–1048.

(50) Hwang, S. K.; Park, T. J.; Kim, K. L.; Cho, S. M.; Jeong, B. J.; Park, C. *ACS Applied Materials and Interfaces* **2014**, *6*, 20179–20187.

(51) Zhou, L.; Mao, J.; Ren, Y.; Han, S.-T.; Roy, V. A. L.; Zhou, Y. *Small* **2018**, *1703126*, 1703126.

(52) Derenskyi, V.; Gomulya, W.; Rios, J. M. S.; Fritsch, M.; Fröhlich, N.; Jung, S.; Allard, S.; Bisri, S. Z.; Gordiichuk, P.; Herrmann, A.; Scherf, U.; Loi, M. A. Carbon Nanotube Network Ambipolar Field-Effect Transistors with 108 On/Off Ratio., 2014.

(53) Bisri, S. Z.; Gao, J.; Derenskyi, V.; Gomulya, W.; Iezhokin, I.; Gordiichuk, P.; Herrmann, A.; Loi, M. A. *Advanced Materials* **2012**, *24*, 6147–6152.

(54) Ageev, O. A.; Blinov, Y. F.; Il'in, O. I.; Kolomiitsev, A. S.; Konoplev, B. G.; Rubashkina, M. V.; Smirnov, V. A.; Fedotov, A. A. *Technical Physics* **2013**, *58*, 1831–1836.

(55) Rinkiö, M.; Johansson, A.; Zavodchikova, M. Y.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törma, P. *New Journal of Physics* **2008**, *10*, DOI: 10.1088/1367-2630/10/10/103019.

(56) Park, R. S.; Shulaker, M. M.; Hills, G.; Suriyasena Liyanage, L.; Lee, S.; Tang, A.; Mitra, S.; Wong, H. S. *ACS Nano* **2016**, *10*, 4599–4608.

(57) Choi, Y. S.; Sung, J.; Kang, S. J.; Cho, S. H.; Hwang, I.; Hwang, S. K.; Huh, J.; Kim, H. C.; Bauer, S.; Park, C. *Advanced Functional Materials* **2013**, *23*, 1120–1128.

(58) Yachi, Y.; Yoshimura, T.; Fujimura, N. **2013**, *62*, 1065–1068.

(59) Kim, E. J.; Kim, K. A.; Yoon, S. M. *Journal of Physics D: Applied Physics* **2016**, *49*, 075105.

(60) Martins, P.; Lopes, A. C.; Lanceros-Mendez, S. *Progress in Polymer Science* **2014**, *39*, 683–706.

(61) Zhao, D.; Katsouras, I.; Asadi, K.; Blom, P. W.; De Leeuw, D. M. *Physical Review B - Condensed Matter and Materials Physics* **2015**, *92*, 1–8.

(62) Sun, Y.; Xie, D.; Dai, R.; Sun, M.; Li, W.; Ren, T. *Current Applied Physics* **2018**, *18*, 324–328.

(63) Chen, Z.; Appenzeller, J.; Knoch, J.; Lin, Y.-m.; Avouris, P. *Nano Letters* **2005**, *5*, 1497–1502.

(64) Kahmann, S.; Salazar Rios, J. M.; Zink, M.; Allard, S.; Scherf, U.; Dos Santos, M. C.; Brabec, C. J.; Loi, M. A. *Journal of Physical Chemistry Letters* **2017**, *8*, 5666–5672.

(65) Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. *Nano Letters* **2003**, *3*, 193–198.

(66) Park, R. S.; Hills, G.; Sohn, J.; Mitra, S.; Shulaker, M. M.; Wong, H. S. *ACS Nano* **2017**, *11*, 4785–4791.

(67) Lee, J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, J. *Journal of Physical Chemistry C* **2007**, *111*, 12504–12507.

(68) Sun, Y.-L.; Xie, D.; Xu, J.-L.; Zhang, C.; Dai, R.-X.; Li, X.; Meng, X.-J.; Zhu, H.-W. *Sci. Rep.* **2016**, 1–7.

(69) Vizdrik, G.; Ducharme, S.; Fridkin, V. M.; Yudin, S. G. *Physical Review B* **2003**, *68*, 094113.

(70) Ducharme, S.; Reece, T. J.; Othon, C. M.; Rannow, R. K. *IEEE Transactions on Device and Materials Reliability* **2005**, *5*, 720–735.

(71) Qian, C.; Sun, J.; Kong, L. A.; Gou, G.; Yang, J.; He, J.; Gao, Y.; Wan, Q. *ACS Applied Materials and Interfaces* **2016**, *8*, 26169–26175.

(72) An Kong, L.; Sun, J.; Qian, C.; Gou, G.; He, Y.; Yang, J.; Gao, Y. *Organic Electronics: physics, materials, applications* **2016**, *39*, 64–70.

(73) Kim, S.; Choi, B.; Lim, M.; Yoon, J.; Lee, J.; Kim, H. D.; Choi, S. J. *ACS Nano* **2017**, *11*, 2814–2822.

(74) John, R. A.; Ko, J.; Kulkarni, M. R.; Tiwari, N.; Chien, N. A.; Ing, N. G.; Leong, W. L.; Mathews, N. *Small* **2017**, *13*, 15–23.

(75) Cole, M. W.; Bassett, D. S.; Power, J. D.; Braver, T. S.; Petersen, S. E. *Neuron* **2014**, *83*, 238–251.

(76) Adhikari, S. P.; Kim, H. *IEEE Transactions on Circuits and Systems I: Regular Papers* **2012**, *59*, 2611–2618.

(77) Secco, J.; Corinto, F.; Sebastian, A. *IEEE Transactions on Circuits and Systems II: Express Briefs* **2017**, *65*, 1–1.

(78) Wang, Z. et al. *Nature Materials* **2017**, *16*, 101–108.

(79) Prezioso, M.; Merrikh-Bayat, F.; Hoskins, B. D.; Adam, G. C.; Likharev, K. K.; Strukov, D. B. *Nature* **2015**, *521*, 61–64.

(80) Strukov, D. B.; Borghetti, J. L.; Stanley Williams, R. *Small* **2009**, *5*, 1058–1063.

(81) Valov, I.; Linn, E.; Tappertzhofen, S.; Schmelzer, S.; Van Den Hurk, J.; Lentz, F.; Waser, R. *Nature Communications* **2013**, *4*, 1771–1779.

(82) Waser, R; Aono, M *Nature Materials* **2007**, *6*, 833.

(83) Van de Burgt, Y.; Lubberman, E.; Fuller, E. J.; Keene, S. T.; Faria, G. C.; Agarwal, S.; Marinella, M. J.; Alec Talin, A.; Salleo, A. *Nature Materials* **2017**, *16*, 414–418.

(84) Shen, A. M.; Chen, C. L.; Kim, K.; Cho, B.; Tudor, A.; Chen, Y. *ACS Nano* **2013**, *7*, 6117–6122.

(85) Kim, S.; Yoon, J.; Kim, H. D.; Choi, S. J. *ACS Applied Materials and Interfaces* **2015**, *7*, 25479–25486.

(86) Vu, Q. A.; Kim, H.; Nguyen, V. L.; Won, U. Y.; Adhikari, S.; Kim, K.; Lee, Y. H.; Yu, W. J. *Advanced Materials* **2017**, *29*, 1–7.

(87) Meador, J. L.; Cole, C. S. **1989**, 678–686.

(88) Indiveri, G.; Chicca, E.; Douglas, R. *IEEE Transactions on Neural Networks* **2006**, *17*, 211–221.

(89) Arthur, J.; Boahen, K. *Advances in neural information processing systems 17* **2006**, *23*, 281.

(90) Agnus, G.; Filoramo, A.; Bourgoin, J. P.; Derycke, V.; Zhao, W. *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems* **2010**, 1667–1670.

(91) Liao, S. Y.; Retrouvey, J. M.; Agnus, G.; Zhao, W.; Maneux, C.; Frégonése, S.; Zimmer, T.; Chabi, D.; Filoramo, A.; Derycke, V.; Gamrat, C.; Klein, J. O. *IEEE Transactions on Circuits and Systems I: Regular Papers* **2011**, *58*, 2172–2181.

(92) Zhao, W. S.; Agnus, G; Derycke, V; Filoramo, A; Bourgoin, J.-P.; Gamrat, C *Nanotechnology* **2010**, *21*, 175202.

(93) Chen, C.-L.; Kim, K; Truong, Q; Shen, A; Li, Z; Chen, Y *Nanotechnology* **2012**, *23*, 275202.

(94) Kim, K.; Chen, C. L.; Truong, Q.; Shen, A. M.; Chen, Y. *Advanced Materials* **2013**, *25*, 1693–1698.

(95) Park, R. S.; Hills, G.; Sohn, J.; Mitra, S.; Shulaker, M. M.; Wong, H. S. *ACS Nano* **2017**, *11*, 4785–4791.

(96) Ha, T. J.; Kiriya, D.; Chen, K.; Javey, A. *ACS Applied Materials and Interfaces* **2014**, *6*, 8441–8446.

(97) Robert-Peillard, A.; Rotkin, S. V. *IEEE Transactions on Nanotechnology* **2005**, *4*, 284–288.

(98) Cao, J.; Nyffeler, C.; Lister, K.; Ionescu, A. M. *Carbon* **2012**, *50*, 1720–1726.

(99) Fuhrer, M. S.; Kim, B. M.; D??rkop, T.; Brintlinger, T. *Nano Letters* **2002**, *2*, 755–759.

(100) Cui, J. B.; Sordan, R.; Burghard, M.; Kern, K. *Applied Physics Letters* **2002**, *81*, 3260–3262.

(101) Rinkio, M.; Johansson, A.; Paraoanu, G. S. **2009**, *197*.

(102) Hwang, I.; Wang, W.; Hwang, S. K.; Cho, S. H.; Kim, K. L.; Jeong, B.; Huh, J.; Park, C. *Nanoscale* **2016**, *8*, 10273–10281.

(103) Aguirre, C. M.; Levesque, P. L.; Paillet, M.; Lapointe, F.; St-Antoine, B. C.; Desjardins, P.; Martel, R. *Advanced Materials* **2009**, *21*, 3087–3091.

(104) Abraham, W. C. *Philosophical Transactions of the Royal Society B: Biological Sciences* **2003**, *358*, 735–744.

(105) Heo, J.; Bockrath, M. *Nano Letters* **2005**, *5*, 853–857.

(106) Jespersen, T. S.; Nygård, J. *Nano Letters* **2005**, *5*, 1838–1841.

(107) Authors, P. PyVISA: Control your instruments with Python PyVISA 1.9.0 documentation., 2018.