PbS nanocrystal based field-effect transistors

Bachelor thesis July 2012

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Abstract

Colloidal nanocrystals are interesting materials because of their size-dependt optical and electronic properties. Due to their semi-conducting features they can be used in electronic devices, like transistors. However, some issues need to be solved for their integration in devices. Nanocrystals are unstable and have the tendency to aggregate, becoming bulk semi-conducting material again. Therefore, during the synthesis, long insulating molecules, called 'surface ligands', are attached to the surface of the nanocrystals to keep them separated from each other. These molecules need to be replaced by shorter molecules that allow the transport of charges from one particle to the other. In this thesis, we fabricated field effect transistors based on PbS nanocrystals treated with 3-mercaptopropionicacid (3-MPA) in a top contact configuration. Two different batches of PbS Lead(II)Sulfide nanocrystals were used, PbS-A clean and PbS-C super-clean, having a different degree of purity. The objective of the work was to test the influence of the cleaning procedure on the device performance. Both the devices based on PbS-A and PbS-C showed ambipolar behavior. The hole carrier mobility measured was unaffected by the different cleaning, instead the higher purity of the PbS-C superclean resulted in an increased electron mobility.

Contents

Introduction

In modern electronics a transistor is a key element used in computers, radios, mobile phones, etc. to amplify and switch current. The most common material used to fabricate a transistor is silicon. To use silicon for device application, the purity has to be high. Moreover, the fabrication process is time consuming and rather expensive because it requires very high temperature and low pressure. Therefore, alternative materials have been explored. In particular material that can be solution processed at room temperature.

A recent field of research is exploring the possibility to use nanocrystals for electroni and optoelectronic device application. Nanocrystals are very small semi-conducting crystalline materials, with a size ranging from 1 to 10 nm. Such nanocrystals can be made of different semiconductors including many II-IV and IV-VI semiconductors. Because of their small size, they are subject to the quantum confinement effect, which causes a size dependency of their energy band gap. In other words, modifying the size and shape of the particle changes the electronic and optical features of the nanocrystal. This feature makes nanocrystals very attractive for several applications such as light emitting diodes, solar cells, photo detectors and transistors. The nanocrystals, due to their very small size, are instable in solution and have the tendency to aggregate. Therefore, during the synthesis long molecules, called *surface ligands,* cover the surface of the nanoparticles to avoid the aggregation. These long ligands are however insulating molecules. To make use of the semi-conducting properties of the nanocrystals, charges should be able to travel between particles. This is realized by replacing the surface ligands molecules with shorter molecules. These molecules are able to "crosslink" the nanocrystals, allowing a current to flow between the NC layer.

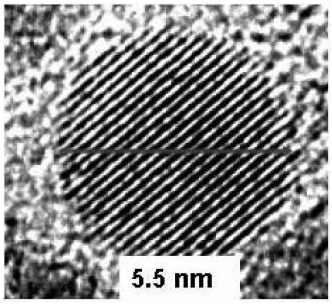


Figure 1, transmission electron microscopy image (TEM) of a single gold nanocrystal

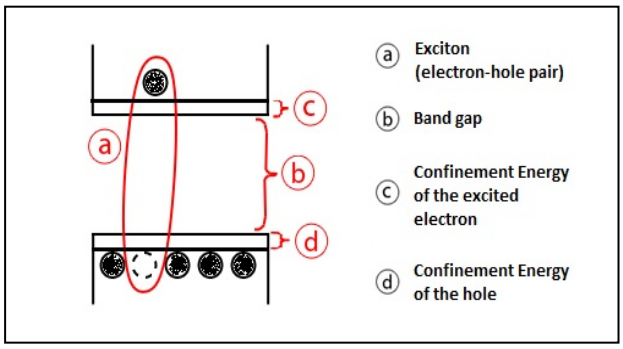
In this thesis, field effect transistor based on PbS Lead(II)Sulfide nanocrystals have been fabricated. The substitution of the surface ligands is done using a 3-mercaptopropionicacid (3-MPA) solution. We tested two different batches of PbS

Lead(II)Sulfide nanocrystals PbS-A and PbS-C, having a different degree of purity clean and super-clean, respectively. The difference is due to the cleaning procedure, performed after the synthesis of the PbS nanocrystals, so is not the quality of the NCs that is changing but the content of impurities in the solution where the NCs are dissolved. In PbS-C more left overs of the synthetic process are removed thanks to repetitive washing processes. A higher purity should result in a higher mobility. A comparison between the two batches is made to test the effect of the nanocrystal purity on the device performance.

II. Theory

II.I *Nanocrystals*

Nanocrystals are small particles of semi-conducting crystalline material containing from a 100 to 1000 atoms. When the dimensions of the particles are such, the quantum confinement effect starts playing a role.



A bulk semi conducting material has a certain band gap (the energy gap between valence and conduction band), which is fixed for every semi-conductor. Electrons can jump from valence band to conduction band leaving behind a hole: because of the columbic interaction the electron-hole pair can form the so called exciton. The distance between the electron and the hole in the exciton is called the 'exciton bohr radius'. If the nanocrystal is smaller than this typical length, the electronic and optical properties of the nanocrystal become size- dependent due to the quantum confinement effect. This effect splits up the continuous energy bands of the bulk semi-conducting material into discrete energy levels (see figure below).

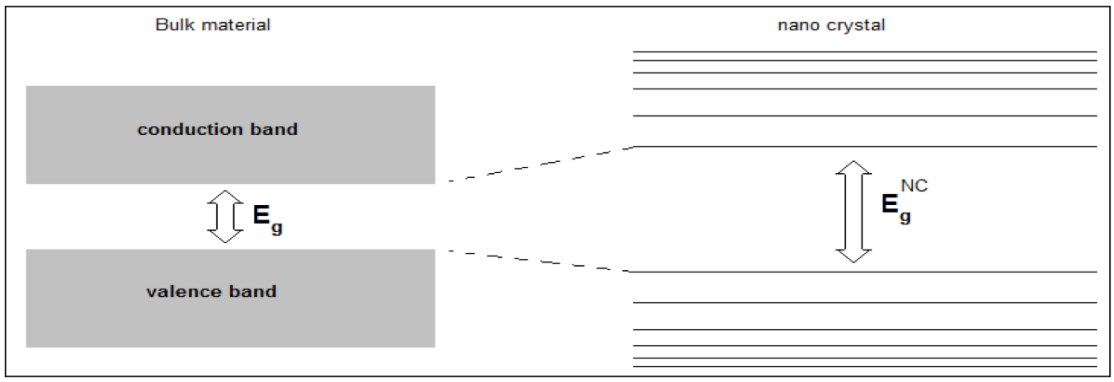


Figure 3, the quantum confinement effect.

The size dependency of the energy band gap of a nanocrystal is shown by the formula below, which was introduced by L. Brus. The original band gap of the bulk semi-

[1] http://upload.wikimedia.org/wikipedia/commons/b/ba/Exicton_energy_levels.jpg

conducting material is given by E_g. One can see that the band gap of a nanocrystal is size-dependt from the presence of Radius term (R), m_e and m_h are the effective masses of the electron and the hole. The reduced Planck constant is represented by $\hbar$, and ε is the dielectric constant of the semiconductor.

$$E_g^{NC} = E_g + \frac{\hbar^2 \pi^2}{2R^2}\left(\frac{1}{m_e} - \frac{1}{m_h}\right) - \frac{1.8e^2}{\varepsilon\varepsilon_0 R}$$

Equation 1, Energy band gap of a nanocrystal.

The optical and electronic properties can be therefore changed by varying the size of the nanocrystals. When the band gap is changed, the absorption and emission spectra can be modified. In the picture below a shift in absorption spectrum of Lead(II)Sulfide (PbS) nanocrystal having different sizes is shown.

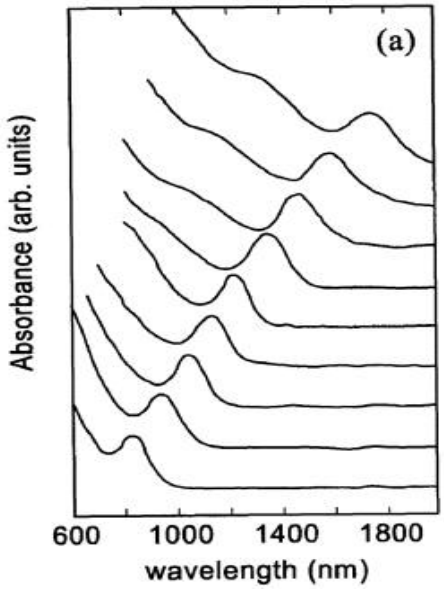


Figure 4 The shift in the absorption peak of PbS nanocrystals of different sizes. .

II.II *Crosslinking of surface ligands*

Synthesis of the nanocrystals

The synthesis of nanocrystals starts by heating the Pb precursor together with a solvent, which contains the surface ligands. The temperature is first raised to 145 C., then the precursor of Sulfur is injected and the temperature is cooled to room temperature. At this point, the nanocrystals start growing. The type and size control of the nanocrystals is a very delicate process. A fine-tuning of the temperature is necessary to obtain the growth of the desired nanocrystals.

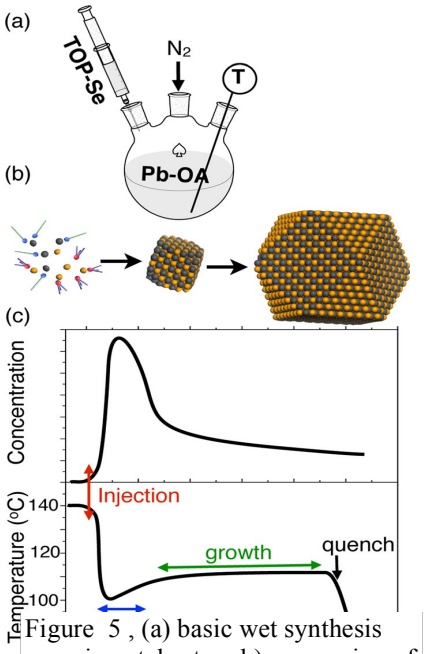


Figure 5 , (a) basic wet synthesis experimental setup, b) conversion of precursor molecules to nanocrystals (c) concentration and temperature profiles.[1]

At the end of the synthetic process the nanocrystals are surrounded by the surface ligands. These long carbon chain molecules will avoid the aggregation of the nanocrystals, ensuring the stability in solution of the nanoparticles. However, since the surface ligands are insulating, in order to use the nanocrystals in devices it is necessary to replace these molecules with shorter ones.

For the ligand exchange procedure short molecules with two head groups (thiols, carboxylic acid etc.) that can bind with the nanocrystals are used (see Fig.7). The substitution takes place because of the higher affinity of these molecules with the nanocrystal surface. Also, as a result of this process, the nanocrystals are crosslinked together.

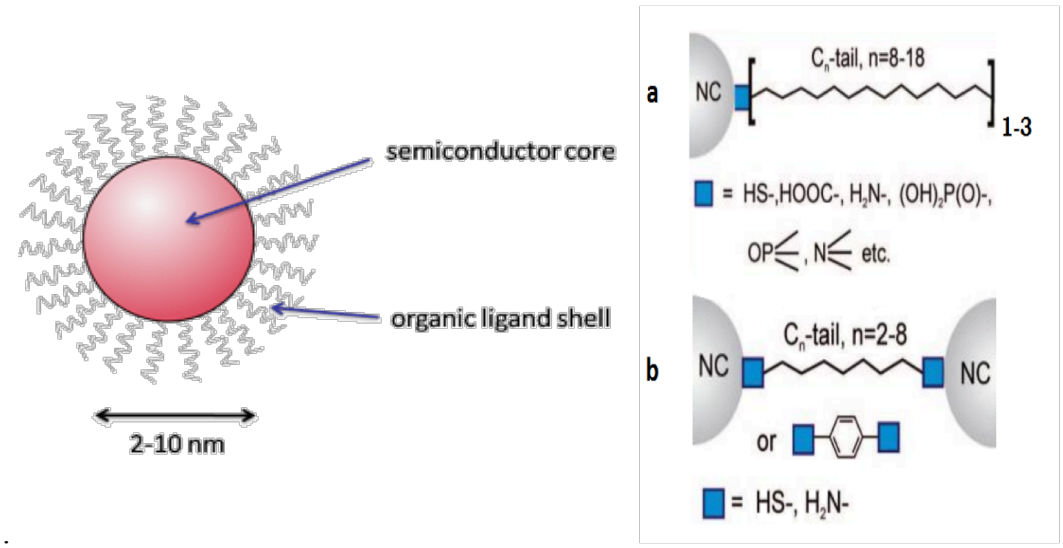


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Figure 6, Schematic of substitution of the surface ligands by crosslink molecules.[2]

[2] http://www-mtl.mit.edu/wpmu/tisdale/research/

III Field-effect transistor

In this thesis Field-effect transistors (FET) based on nanocrystals are realized.
The transistor is a device with three electrodes: the gate, the source and the drain. The gate electrode is separated from the active layer by a dielectric layer.

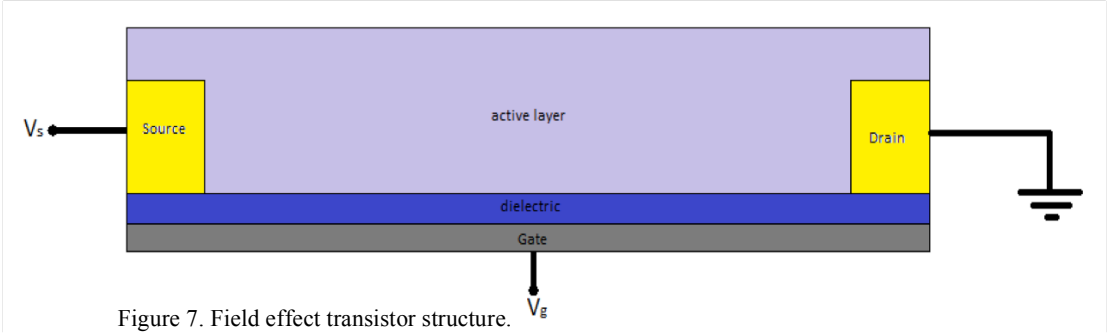

Figure 7. Field effect transistor structure.

By applying a voltage to the gate electrode, it is possible to control the current flowing between the source and the drain in the channel. Depending on the characteristics of the material and the voltage applied electrons, holes, or both can flow in the channel. For example when a positive gate voltage is applied, negative charge carriers are accumulated forming a n-type conducting channel in the active layer. Obviously not all charge carriers are mobile because of traps that need to be filled. Therefore the gate voltage should overcome a certain value that is called the *threshold voltage* to induce enough charge carriers and fill the deep traps.

When a relatively small source drain current is applied which is much lower than the gate voltage, ($V_{ds} << V_g$) the transistor is in the linear regime. The source-drain current is directly proportional to the source-drain voltage and transistor works as a resistor.
When applying an even higher source/drain voltage more charge carriers will be drawn to the source or drain (depending on a positive or negative value of the gate voltage). The conductive channel will become pinched off when the source/drain voltage reaches a certain limit, $V_{ds} = V_g - V_{th}$. The FET is starting to work in the so-called “saturation regime”. When raising the source/drain voltage even more the pinched off point is starting to move away from the electrode (see figure 2d), causing a gap between conductive channel and drain electrode. Charge carriers are still free to move out of the channel to the electrode, but they need to cross the depletion region

between pinched off point and electrode. A higher V_{ds} would not result in an higher I_{ds} due to the increase of the gap between pinched off point and drain electrode. This results into a constant value for the source-drain current.

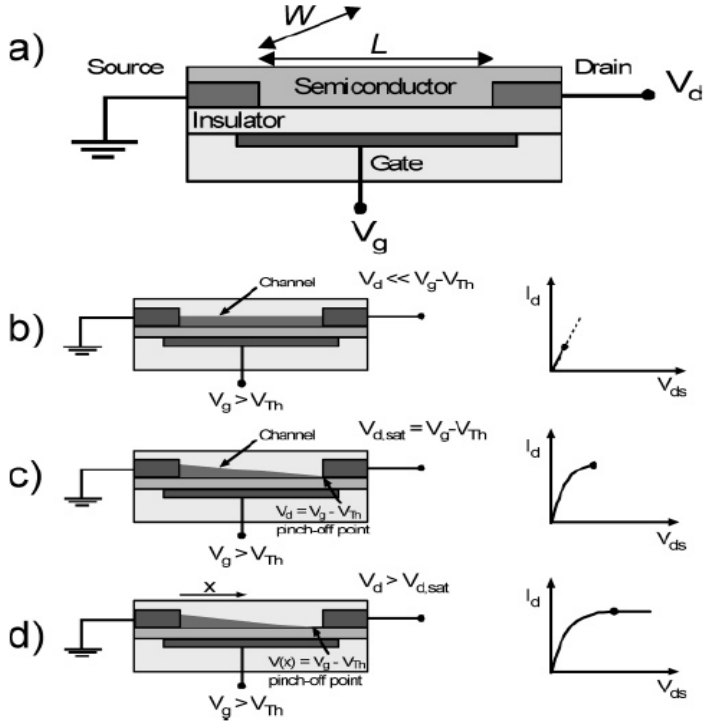

Figure 8, a) Field-effect transistor, b) linear regime,
c) pinch off point, d) saturation regime

III. II *Parameter extraction*

The dielectric layer can be seen as a capacitor with capacitance C, and then the additional charge per unit surface is equal to:

$$Q = CV$$

With Vx the voltage at a point x due to the voltage between source and drain and Vt the threshold voltage needed for charge carrier accumulation, the voltage at a point x over the dielectric is equal to:

$$V(x) = V_g - V_t - V_x(x) \tag{3.2}$$

$$V_x(x) = V_s - \frac{V_s}{L}x \tag{3.3}$$

If the channel has a width W, then this means that charge over an infinitesimal surface Wdx is equal to:

$$dQ = C\big(V_c - V_t - V_x(x)\big)Wdx \tag{3.4}$$

The current that flows from source to drain is:

$$I_{ds} = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt} \tag{3.5}$$

The charge mobility μ is defined as the ratio of the mean velocity of the charge and de electric field:

$$\mu = \frac{v}{E} = \frac{\frac{dx}{dt}}{\frac{-dV}{dx}} \quad \rightarrow \quad -\mu = \frac{dV}{dx} \tag{3.6}$$

Now equation 3.5 and 3.6 can be combined to acquire:

$$I_{ds}dx = -\frac{dq}{dx}\mu\frac{dV}{dx}dx \tag{3.7}$$

which with equation 3.4 becomes:

$$I_{ds}dx = -\mu C\big(V_c - V_t - V_x(x)\big)WdV \tag{3.8}$$

Now we assume that the carrier mobility is constant over the channel length. This is only valid in the linear regime were the density of charge carriers is uniform over the channel length. In the saturation regime instead this assumption does not hold because the carrier density varies over the channel. Because in the linear regime μ is assumed to be a constant 3.8 can be integrated over x and V respectively:

$$\int_0^L I_{ds}dx = \int_0^{V_s} -\mu CW\left(V_g - V_t - V_x(x)\right)dV = I_{ds}L = -\mu CW\left(V_gV_s - V_cV_s - \frac{{V_s}^2}{2}\right) \tag{3.9}$$

$$I_{ds} = -\frac{\mu CW}{L}\left(V_gV_s - V_cV_s - \frac{{V_s}^2}{2}\right) \tag{3.10}$$

Now equation 3.10 is differentiated over V_g to obtain:

$$\frac{\partial I_{ds}}{\partial V_g} = \frac{\mu CW}{L}V_s \tag{3.11}$$

$$\rightarrow \quad \mu = \frac{\partial I_{ds}}{\partial V_g}\frac{L}{CWV_s} \tag{3.12}$$

In this last equation can be seen that μ is easily extracted from the slope of I_{ds} versus V_g plot provided the device is in the linear regime, see figure 3.4.

When $V_s = V_g - V_t$ the current saturates, so with this information and equation 3.10 the current in the saturation regime can be calculated:

3.13

$$I_{ds,sat} = -\frac{\mu CW}{L}\left(V_g(V_g - V_t) - V_t(V_g - V_t) - \frac{(V_g - V_t)^2}{2}\right)$$

$$= -\frac{\mu CW}{L}\left(V_g - V_t - \frac{(V_g - V_t)}{2}\right)(V_g - V_t) = \frac{\mu CW}{L}\frac{(V_g - V_t)^2}{2}$$

From this equation the mobility can also be extracted by plotting $\sqrt{I_{ds,sat}}$ versus V_g:

$$\sqrt{I_{ds,sat}} = \sqrt{\frac{\mu CW}{L}\frac{(V_g - V_t)^2}{2}} = \sqrt{\frac{\mu CW}{2L}}(V_g - V_t) \qquad 3.14$$

Now equation 3.14 can be differentiated with respect to V_g againt to obtain:

$$\frac{\partial\sqrt{I_{ds,sat}}}{\partial V_g} = \sqrt{\frac{\mu CW}{2L}} \quad \rightarrow \quad \mu = \left(\frac{\partial\sqrt{I_{ds,sat}}}{\partial V_g}\right)^2 \frac{2L}{CW} \qquad 3.15$$

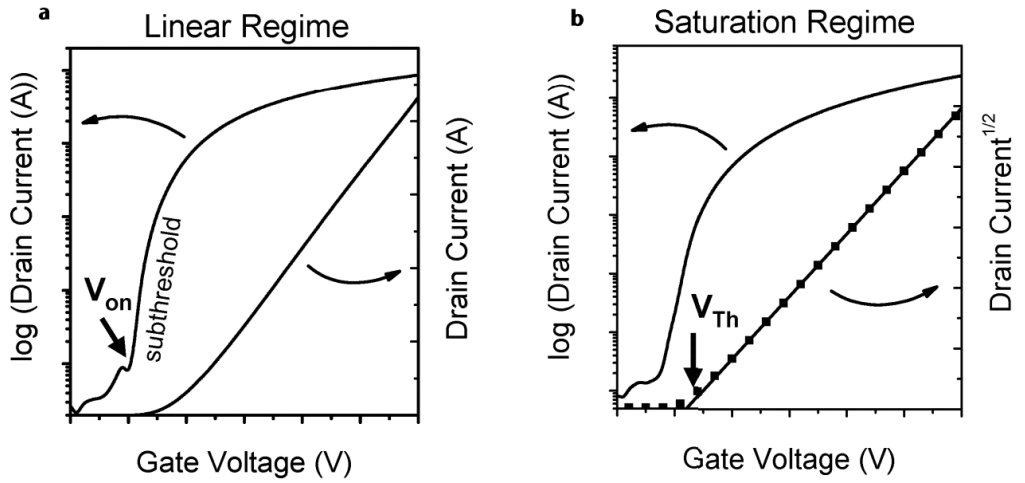

Figure 9 Typical transfer characteristics of a field effect transistor a) in the linear regime, b) in the saturation regime.

From this last equation μ can be obtained from the slope of $\sqrt{I_{ds,sat}}$ versus V_g plot (transfer) when the device is in the saturation regime, see figure 10. Inside a tiny amount of material the actual mobility varies, so the extracted value of mobility μ is only a mean value in the layer.

The on/off ratio is another key parameter. It is the ratio between the current that flows when the transistor is turned off and the current in the saturation regime. The 'on-off' ratio is an indication of the switching capability of the transistor.

III.III *Ambipolar characteristics*

As mentioned before in a field effect transistor positive charge carriers, holes, or negative charge carriers, electrons can flow in the transistor channel. A third option is that both types of carriers are present at the same time. This is called a bipolar or ambipolar FET.

To examine the working mechanism of ambipolar transistor we can consider the different voltages applied. With a given positive drain voltage $V_{d,}$ we apply a gate voltage that is the same as the given drain voltage and we hold the source potential to zero ($V_g = V_d$, $V_s = 0$). In this situation, since the gate voltage is more positive than the source voltage, electrons are injected at the source. This happens when $V_g > V_{th,e}$, ($V_{th,e}$ being the threshold voltage for the electrons.) During this regime only electrons are the active charge carriers. This regime is called the unipolar regime.
In the case of V_g being smaller then V_d, the potential difference V_g - V_d is negative. When $V_g << V_{th,e,}$ this results into an injection of holes at the drain electrode. Again the transistor will have a unipolar regime. This time only holes will accumulate in the conductive channel.
To achieve injection of both charge carriers one should have a V_g of value between V_d and V_s. Now the gate voltage is bigger than $V_{th,e}$ but also $V_g - V_d < V_{th,h}$ holds. Both charge carriers will be injected into the channel and the transistor will work in the ambipolar regime.

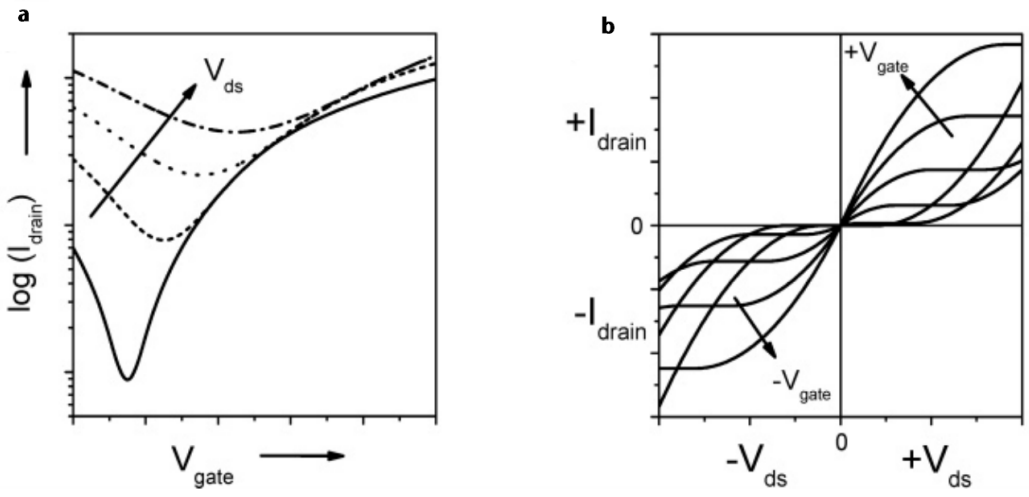

figure 10. a) Ambipolar transfer curve, b) Ambipolar output curve.

IV. Methodology & materials

IV.I *Nanocrystals*

In this thesis we used PbS nanocrystals, to fabricate transistors. In Figure 12 the absorption spectrum of the nanocrystal used is shown. The peak around 1270 nm, corresponds to a band gap around 1 eV and to a dimension of the nanocrystal of about 6nm.

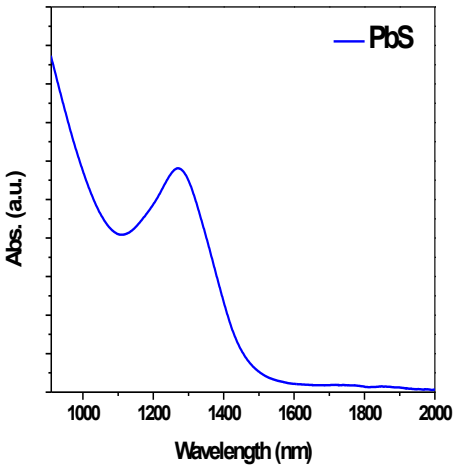

Figure 11. Absorption spectrum PbS

After the synthesis the nanocrystals undergo a cleaning process. The molecules and left over of the synthesis should be removed from the solution to ensure a certain degree of purity. In this thesis two types of PbS have been used. The cleaning procedure for the two batches is different; in particular for the batch C "superclean" two additional steps have been added.

PbSLP1111a ***clean***	Washed with Hexane/Ethanol X3, CHCl3
PbSLP1111c ***superclean***	Washed with Hexane/Ethanol X3, CHCl3, CH3OH, dried, CHCl3 anhydrous

For the device fabrication a solution of 5mg/ml of PbS nanocrystals in $CHCl_3$ has been used.

3-Mercaptopropionicacid.

For the ligand exchange procedure we used 3-mercaptopropionicacid (3-MPA), which has two different head groups (a thiol and an carboxyl group), which can react with the nanocrystals surface. The 3-MPA is dissolved in methanol with a concentration of 10%.

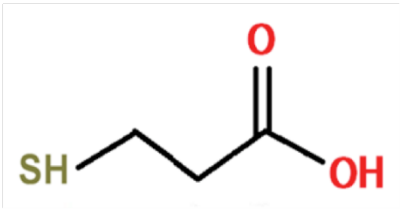

Figure 12 , 3-mercaptopropionicacid (3-MPA)

IV. *Substrates.*

The substrates used in the experiments are silicon/silicon dioxide substrates. The silicon serves as the gate and it is covered by a 230 nm layer of silicon dioxide, which serves as dielectric. The capacitance of the silicon dioxide is **15*10^$^{-9}$ F.** The type of device structure that has been used is a top-contact. The source and drain gold contacts have been evaporated using a mask on top of the active layer. The mask allows obtaining on the same substrate three devices with different channel lengths and fixed channel width:

L = 100 µm, W = 13 mm

L = 200 µm, W = 13 mm

L = 300 µm, W = 13 mm

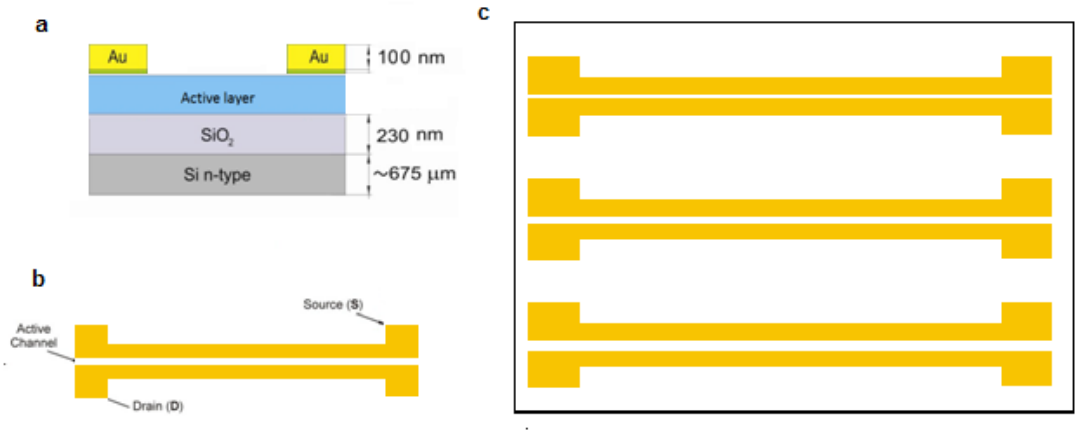

Figure 13. II The top contact transistor structure: a) Side view of the layers. b) Structure of the transistor electrodes. c) Layout of the devices on the substrate.

IV.III *Cleaning*

The substrates have being cleaned following a standard procedure for silicon substrates. The cleaning process is done in a clean room to avoid contamination of dust particles. The standard procedure is the following:

1. Acetone bath 10 min
2. Isopropanol bath 10 min
3. Hotplate 10 min. for drying
4. Plasma cleaner. 10 min

After this procedure the substrates are ready for nanocrystal deposition.

IV.IV *Deposition of the nanocrystals.*

The NCs depositions are done inside a nitrogen glove box, since the materials used are very sensitive to oxygen and water. For the deposition of the nanoparticle solution we used the spin-coating technique. A droplet of solution is deposited on top of the substrate. The substrate rotates very fast to obtain a uniform distribution of the solution and the formation of a thin layer. The parameters used for the spin-coating procedure are:

- V = 4000 rpm
- A = 4000 rpm
- T = 60 sec

For the formation of the active layer, the procedure is the following

- depositing nanocrystals
- spin coating
- depositing crosslinking solution
- waiting for 30 sec
- spin coating

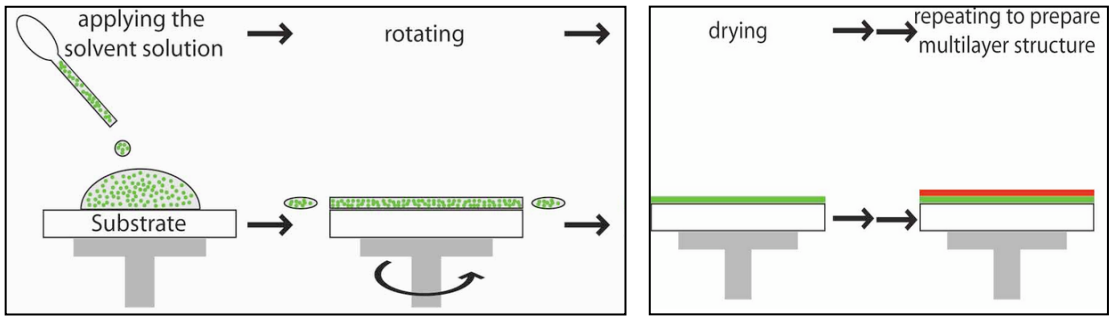

figure 14. procedure for the fabrication of the active layer. [3]

This process is repeated ten times to form layer thick enough (about 60-80nm). After the depositions the substrate is placed on a hotplate at 140ºC for the annealing treatment to get rid of all the remaining solvent.

After annealing the gold contact are being evaporated on the surface. This is done by using a thermal evaporator. After reaching a pressure of 10^{-7}mbar in the chamber, 50 nm of gold have been evaporated with a rate of 1 Å/sec.

IV.V *Measurement*

For measuring the current-voltage characteristics of the devices, three probes are connected to source, drain and gate. As stated above the silicon is used as the gate electrode and the other two probes are connected to the gold contacts, evaporated on top of the active layer. The probes are connected to an Agilent- semiconductor parameter analyzer for modulating the voltage and recording the current.

[3] http://materials.web.psi.ch/Research/Thin_Films/Methods/Spin.htm

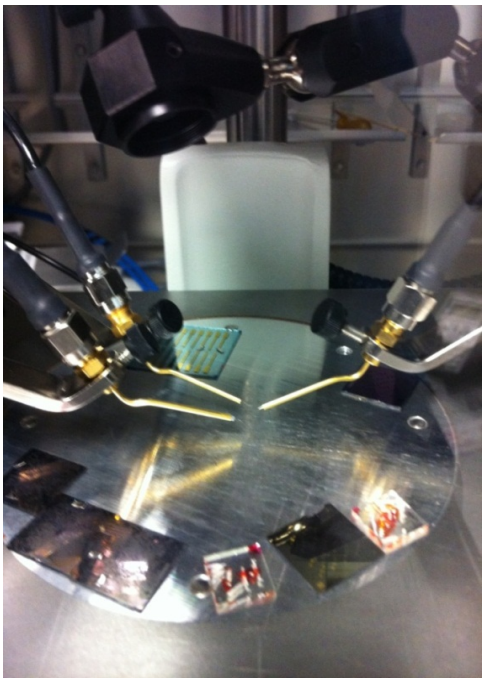

figure 15. Photo of the probe station used for the measurements.

V. Results.

Below the results of the measurements are presented. The objective of this work is to understand the influence of the cleaning procedure on the device performance; therefore a comparison is made between the two PbS batched. First the n-channel is displayed. The gate voltage is varied from 0 V up to 80 V in steps of 20 V. Then, the p-channel is presented. The gate voltage was applied from 0 V to -80 V, in steps of -20 V. The output curves are shown in figure 16 & 17.

L = 100 µm

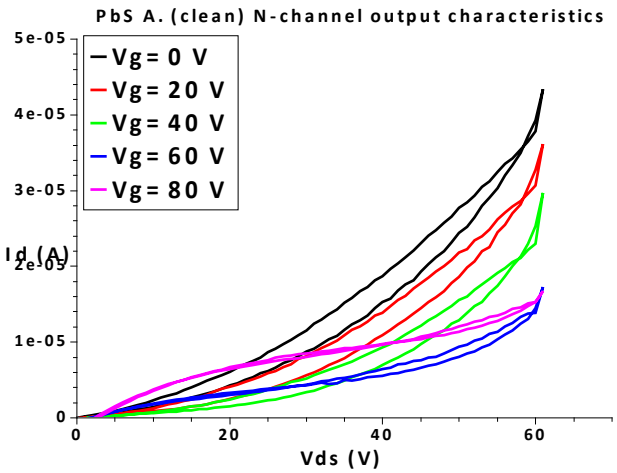

Figure 16

L = 200 µm

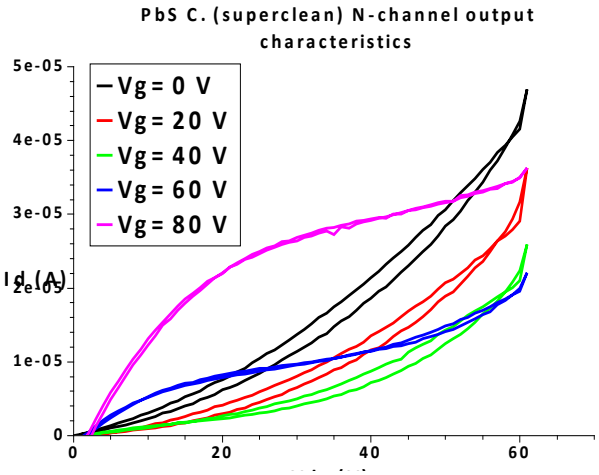

Figure 17

The graphs show ambipolar behavior. This can be explained by the relatively small band gap (≈ 1 eV) of the nanocrystals. The small band gap allows both electrons and holes to be injected from the gold electrodes. The first four values of the gate voltage result in superlinear curves, which is explained by the presence of both electron and hole charge carriers. The curves measured applying 80 V show some saturation behavior. This is an indication of an ambipolar active layer. The front and back sweeps of the curves do not overlap. This is an indication of trapping of charges during the sweeping of the voltage of the active layer. The drain current measured in the transistor fabricated using the PbS C *superclean* is much higher at Vg = 80 V. This can be a first suggestion of the influence of the cleaning procedure on the device performance.

The p-channel characteristics are shown below.

L = 100 µm

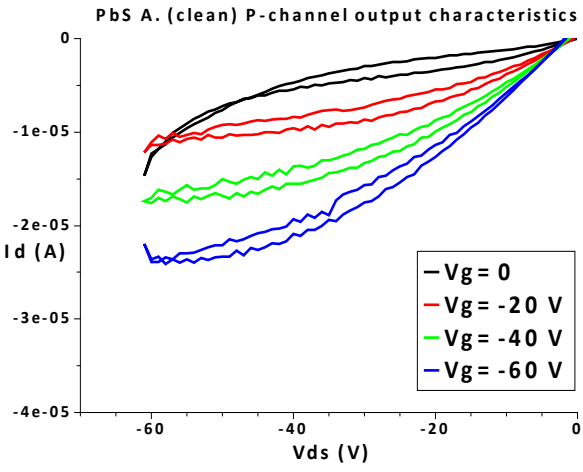

Figure 18

L = 200 µm

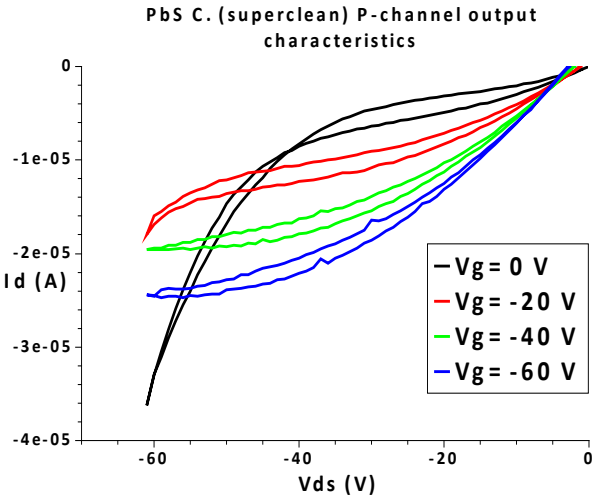

Figure 19

Also these graphs show ambipolar characteristics. The first curve measured at Vg = 20 V is a superlinear curve. All other curves show saturation. The curves in the plots above show some noise and hysteresis. This effect has been observed in all the devices tested, but especially in those fabricated using the PbS A *clean* batch. The

noise and the hysteresis are due to traps, defects and impurities in the active layer of the device.

In order to calculate the mobility the transfer curves were recorded in the saturation regime. The transfer curve has been measured by applying a drain voltage of 30 V. On the left axis the drain current is plotted against the gate voltage for the extraction of the I_{on}/I_{off} ratio. On the right axis the square root of the drain current is plotted against the gate voltage for the extrapolation of the carrier mobility.

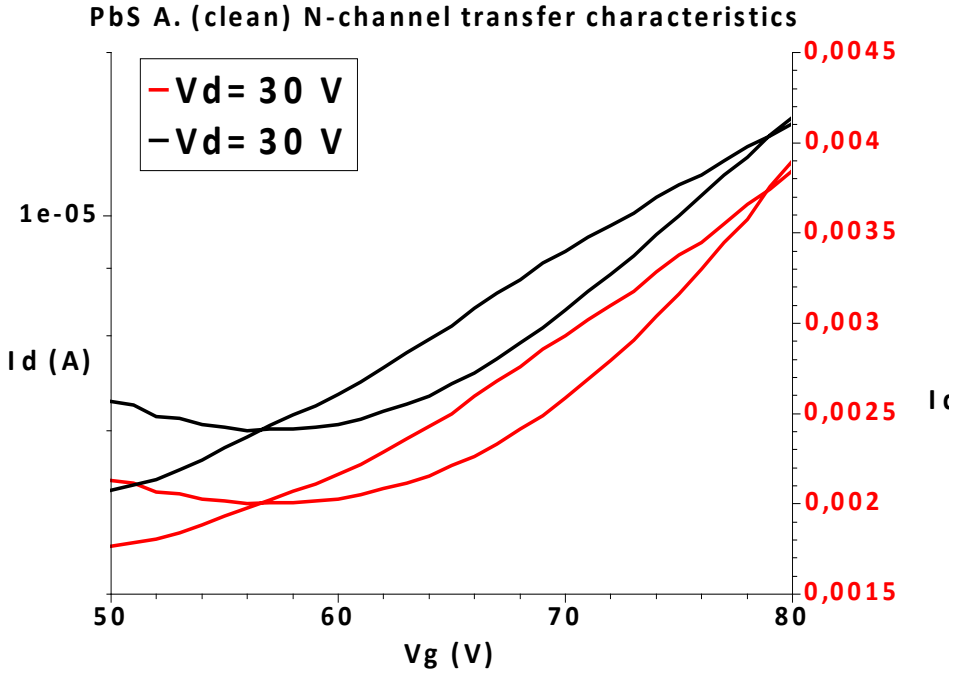

Figure 20

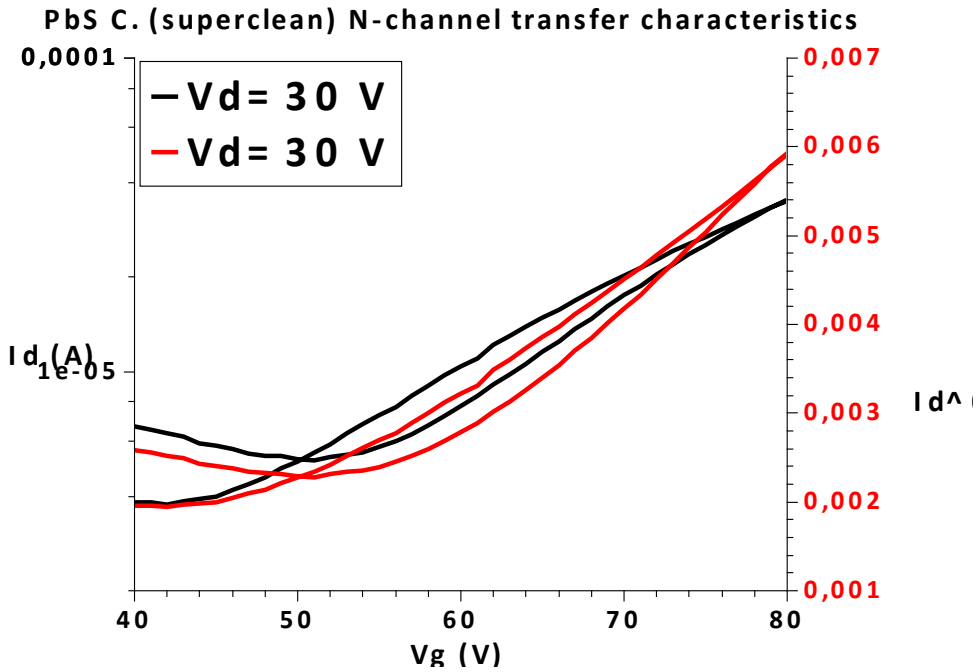

Figure 21

The charge carrier mobilities calculated from the graphs are

- PbS A *clean*: μ_e = **5,0*10**$^{-3}$ cm^2 / Vs
- PbS C *superclean*: μ_e = = **3,0*10**$^{-2}$ **cm2** / Vs

The *superclean* batch shows higher charge carrier mobility for the electrons, being the difference between the two values of one order of magnitude.

The on/off ratio is relatively low, due to the high leakage current registered in these devices:

- PbS A *clean:* $I_{on/off}$ = **3,5**
- PbS C *superclean*: $I_{on/off}$ = **4**

The saturation transfer curves of the p-channel are presented below:

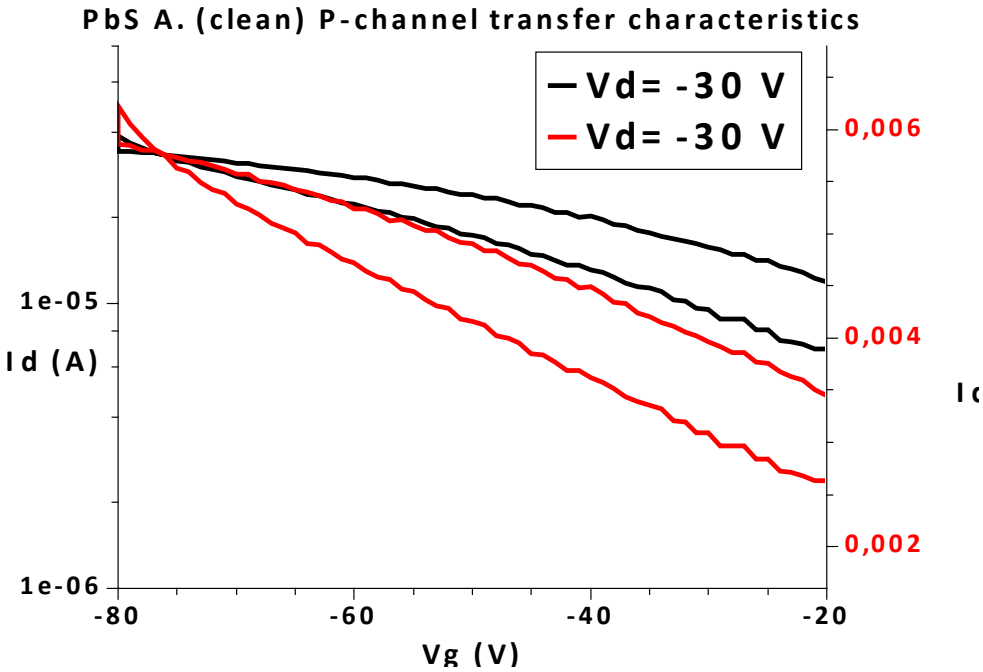

Figure 22

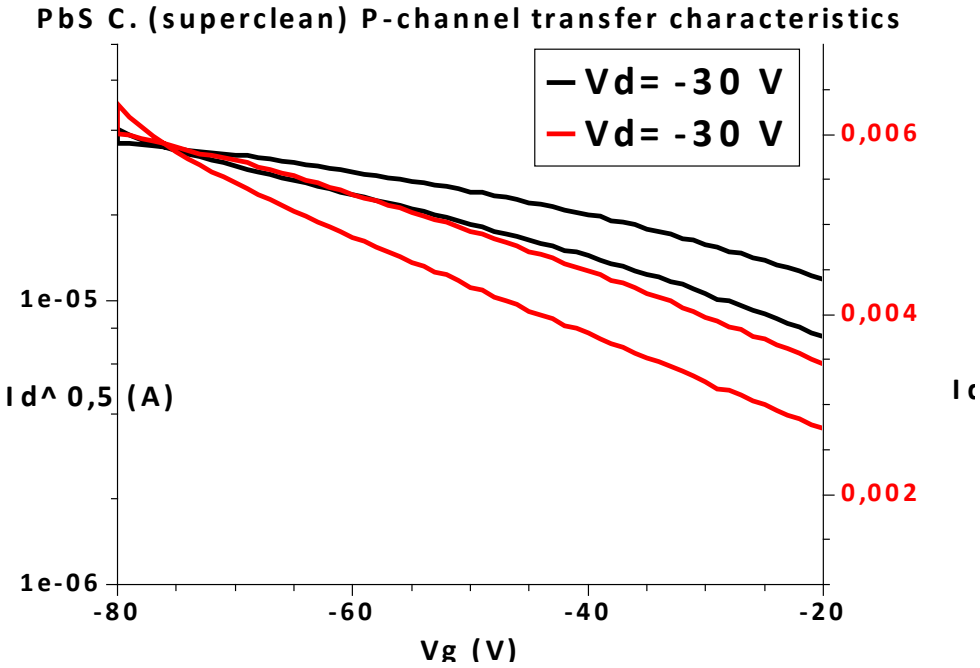

Figure 23

The charge carrier mobilities are:

- PbS A *clean:* μ_h = = **2,7*10^{-3}** cm^2 /Vs
- PbS C *superclean*: μ_h = = **2,5*10^{-3} cm^2** cm^2 /Vs

The carrier mobility is equivalent. Therefore we can conclude that the different cleaning of the PbS has no influence on the hole mobility.

The on/off ratios for the p-channel:

- PbS A *clean:* $I_{on/off}$ = **4.**
- PbS C *superclean*: $I_{on/off}$ = **5**

The leakage current registered during the experiments was quite high, preventing the observation of transistor behaviour in most of the devices tested. In optimal conditions the leakage current should be at least 3 orders of magnitudes lower than the current measured in the devices. Usually high values of leakage current are due to a not proper functioning dielectric.

VI Conclusions

Working transistors were realized using a top contact configuration in order to test two different batches of PbS, PbS A *clean* and PbS C *superclean*, treated with a 3-MPA. Both devices show ambipolar behavior. The hole carrier mobility is equal for both types of PbS nanocrystals. Regarding the electron mobility, the PbS C *superclean* batch shows an increase of mobility, which is an order of one magnitude higher than the one calculated for the PbS A *clean* batch. We conclude that the different cleaning procedure of the PbS nanocystals has a beneficial influence on the electron carrier mobility. This is in agreement with electrons being more sensitive to traps and impurities.

Acknowledgement

My acknowledgement goes to Dr. Claudia Piliego in the first place. You helped me with my problems and were pretty much all the time optimistic about the future. This helped me also keep the confidence going strong. Thank you for everything and guiding me through this research. Secondly, Dr Satria Bisri for all the help in the lab and for doing several evaporations and most of all guiding me.

I would like acknowledge Prof. M.A. Loi for giving me the opportunity for my research and showing the right perspective at certain times, the entire Loi Group for the support and interest, and the technicians for their technical assistance.

I learned a lot on an academic level and as a person. Thank you.

References

1. Meijssen, M. Bachelor Thesis Universty of Groningen (2011). *Crosslinking of nanocrystals for application in transistors*
2. D.V Talapin, J. Lee, M.V. Kovalenko, E.V Shevchenko, *Chem. Rev.,* **2010** 110, 389-458
3. W. Koh, S.R. Saudari, A.T. Fafarman, *Nanoletters* **2011,** 11, 4764–4767
4. A. Carillo-Castillo, A. S. Villasensor, I Meija, S. Aguirre-Tostado, B.E. Gnade, M.A. Quevedo-Lopez. Thin Solid Films.**2012.** 520. 3307-3310
5. K.S. Jeong, J. Tang, H. Liu, J. Kim, A.W. Schaefer, K Kemp, L Levina, X Wang, S Hoogland, R Debnath, L Brzozowski, E. H. Sargent, J. B. Asbury. *Asc Nano.* **2012.** 6. 89-99

6. C. Kittel, *Introduction to Solid State Physics*, Seventh Edition (John Wiley & Sons, New York, Chichester,**1996**).
7. L.E. Brus (2007). *Chemistry and physics of semi-conductor nanocyrstals*
8. J. Vac. *Sci. Technol. A*, **2012.** Vol. 30, No. 3
9. J. Zaumseil, H. Sirringhaus, *Chem. Rev.,* **2007**, 107, 1296-1323