EXPLORING GLASS GATING
SPACE CHARGE SEPARATION TECHNIQUE

Abstract

Ionic Liquid Gating is a known technique to study the properties of quantum phases in thin layer materials. Here we introduce another ionic media - Glass. Field effect transistor was made based on semiconducting WS_2 monolayer as a channel material and glass substrate as a gate insulator. Sample was successfully tuned from band insulating state to metallic and to reentrant insulating state. Similar results were observed based on ionic liquid gating.

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Device Physics of Complex Materials

Introduction

Field Effect Transistors (FET) are widely used in computer chips as a logic element. Moore stated that every 2 years, the number of transistors is doubled. This famous law is called Moore's[1] law and is approaching it's limit.

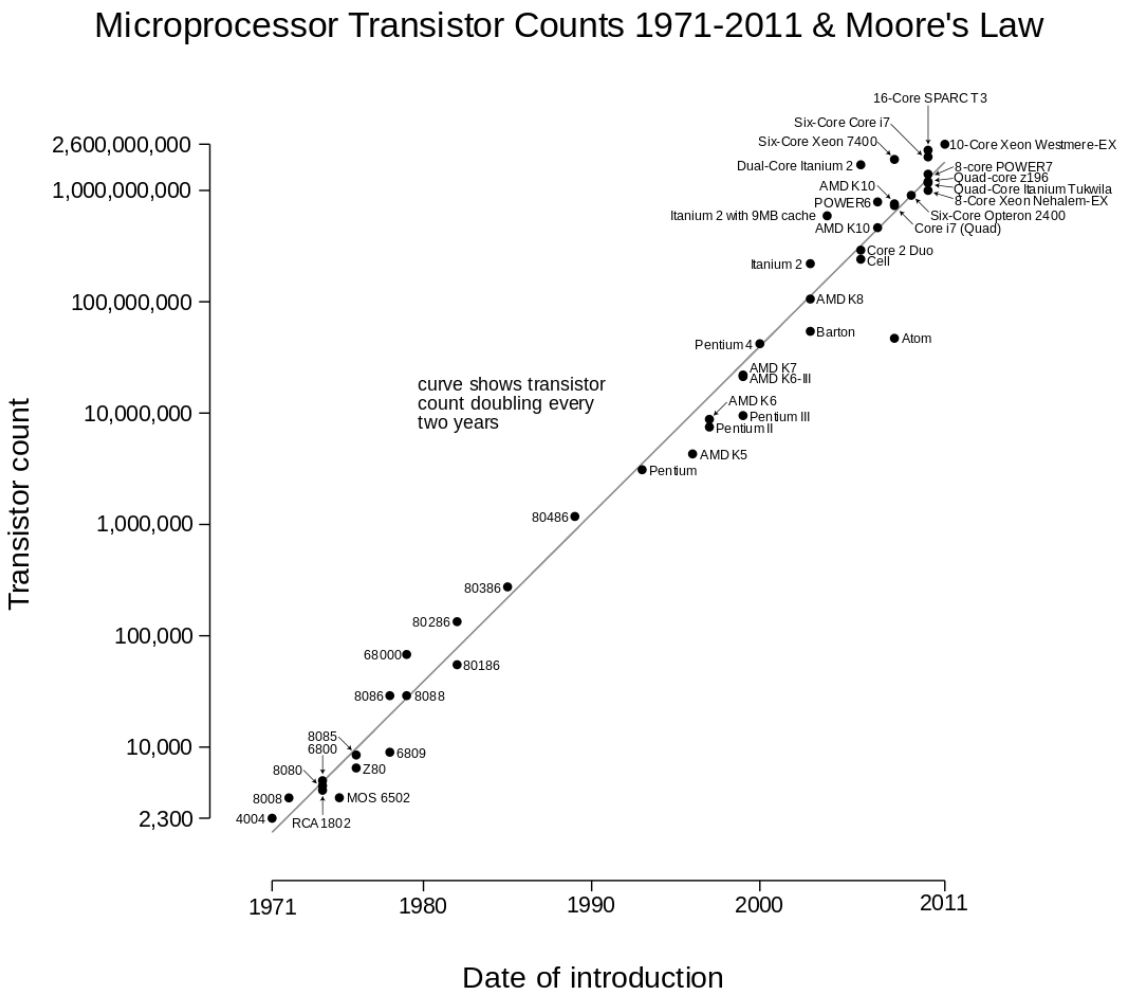

Figure 1: Moore's law. Every two years, the number of transistors in a computer double. This graph[2] shows the law holds until these days, but the limit comes closer.

The typical size of a singe transistor is about 15 nm and it's approaching atomic scales, where the quantum phenomena becomes more pronounced, thus limiting further miniaturisation of single logic elements. To improve the FET, people are intensively studying properties of new materials and exploring new techniques, that can fully explore these properties. First we remind the principle of a typical FET, than we will introduce Electric Double Layer Transistors[3] (EDLT) and later proceed to a new ionic media - Glass. Such techniques are widely used to study Ambipolar transport, electric field control of spin polarisation[4] and circularly polarised electroluminescence can be observed with the help of the EDLT.

Graphite exists of mono layer structures bound by Van-der-Waals forces and can be split into monolayers by the scotch tape method quite easily. This new monolayers, graphene, show different properties from bulk material and is therefore very interesting to study. Graphene shows a metallic state in monolayer. Transition Metal Dichalcogenides (TMD) are a special kind of material existing of a transition metal atom (for example W) and two chalcogen atoms (for example S). Similar like Graphite, TMDs are also formed of monolayers bound by Van-der-Waals forces, but this monolayer has semiconducting properties.

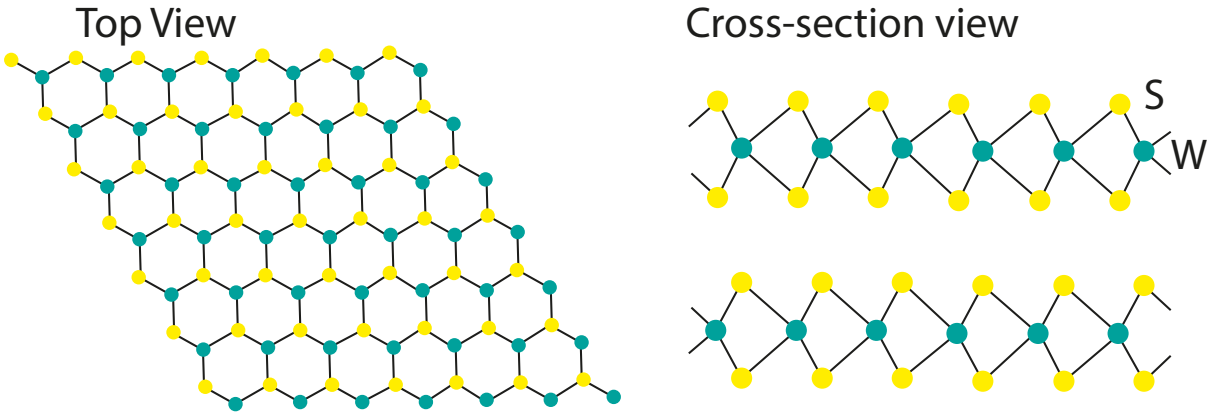

Figure 2: WS_2 structure. Left: top view, hexagonal structure. Right: monolayers on top of each other forming double layer or bulk material.

Where the bulk material has an indirect band gap, a monolayer of WS_2 has a direct band gap[5] and can therefore be used as a transistor and as detectors and emitters in optics. Since the monolayer structure has no inversion center, a new degree of freedom can be used to study valleytronics[6]. The electron spin can be controlled by tuning the excitation laser photon energy, because of the strong spin-orbit coupling in TMDs[7]. Also a superconducting state can be induced when tuned right at low temperature. Therefore WS_2 is a very interesting and promising material to study and do we use it in this device.

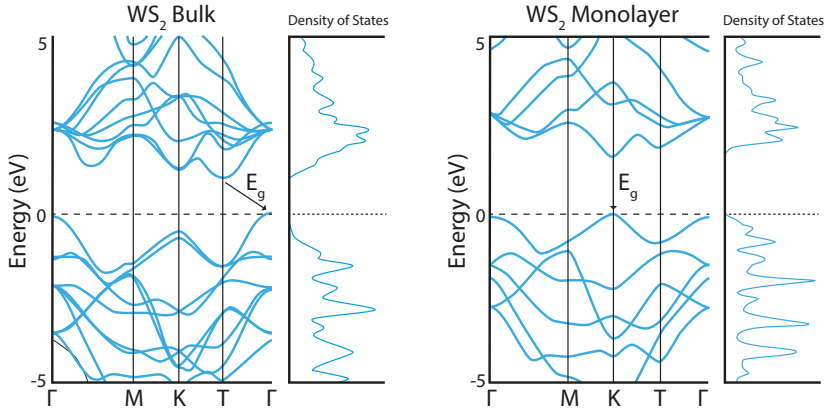

Figure 3: WS_2 electronic band structure. In bulk material there is an indirect band gap (left) and for a monolayer there is a direct band gap (right)

From Insulating State to Metallic State

Electronic properties of materials are determined by their band structure and relative position of Fermi level there. Several basic examples are shown schematically in figure 4. From left to right are metals, semi-metals, semiconductors and insulators[8].
When the Fermi level is in a band, the material is conducting. This type of materials are the metals with typical carrier density of 10^{15} cm^{-2} and a very high conductivity . On the other end we have insulators with a carrier density of 10^{9} cm^{-2} and no conductivity. Then the Fermi level is in the band gap and electrons cannot go from the valence band to the conduction band by thermal excitation.

Between these two types, there are semiconductors with a typical carrier density of 10^{10} - 10^{14} cm^{-2}. For semiconductors, the Fermi level is laying in the band gap, but the band gap is not to big or the fermi level is near one band. For our Glass Gating device we use semiconducting WS_2 monolayer flakes. First we discuss the intrinsic semiconductor. An intrinsic semiconductor has no defects or doping. Its Fermi level is in the middle of the band gap and the semiconductor can become conducting if the energy of the electrons is large enough to overcome the gap. At higher temperature or with an higher gate voltage, the semiconductor becomes more conducting.

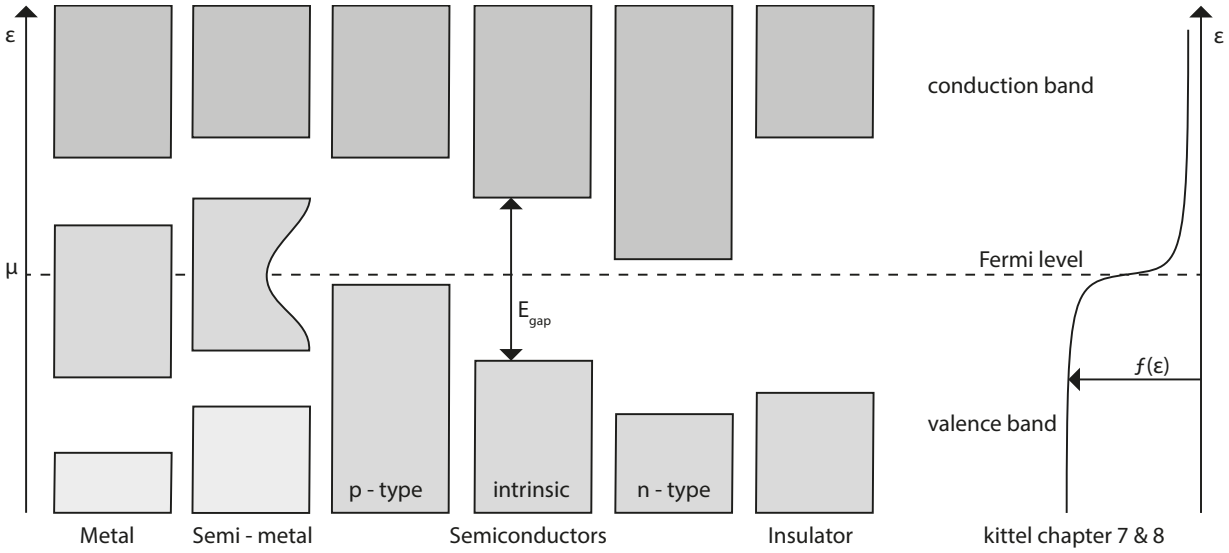

Figure 4: At the most left a metal state and at the right a band insulator. This figure shows the difference in relative position between the Fermi level and the band gap.

The p and n-type semiconductors are both doped with ions. For normal semiconductors often Arsenic for a positive charge (n-type) and Boron for a negative charge (p-type) is used. This charge creates respectively donor levels (n-type) or acceptor levels (p-type). These levels are close to the conduction band or the valence band. Because of this level, the semiconductors become more conductive depending on the doping level. When the doping level increases, the band comes closer to the band and the semiconductor becomes more conducting. This type of electric field tuning by doping, we use to create our device.

Field Effect Transistor

There are serval ways of tuning the carrier density of a semiconducting material and one basic way of tuning can be done by a Field Effect Transistor (FET). For this case we look at a simple MOSFET. This is a device, containing a metal and an insulator oxide. There are two types of MOSFETs: nMOSFET and pMOSFET, depending on if you use a n-type or p-type channel.

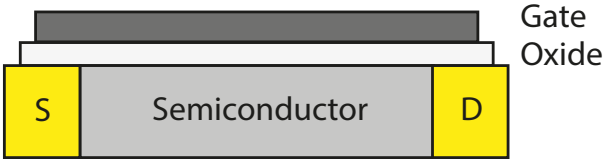

Figure 5: A simpel Field Effect Transistor with a Gate and Insulating layer on top of Semiconducting material.

We consider the pMOSFET type for now. When a positive gate voltage is applied, there is a depletion region created. The positively charged holes are pushed away from the surface and negatively charged acceptor ions are left. At the interface between the Oxide and the depletion layer, there forms a inversion layer if the gate voltage is high enough. Negatively charged carriers form the inversion layer. When the density of holes and electrons is the same, the threshold voltage has been reached.

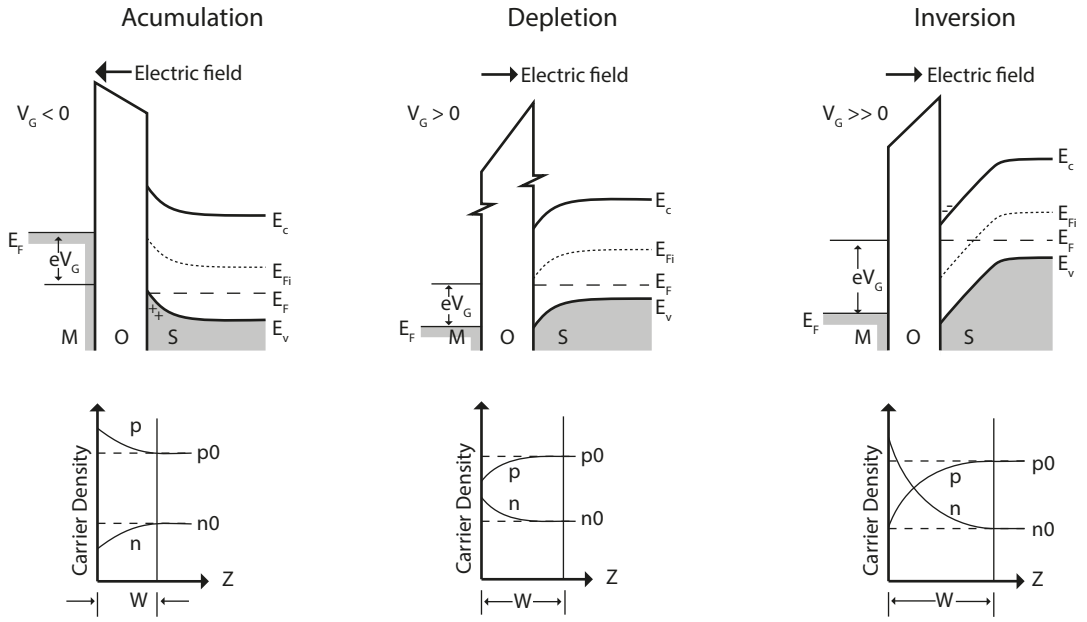

Figure 6: Three regimes of operation of a FET. Accumulation: With a negative gate voltage hole carriers get attracted to the surface and electron density decreases. Depletion: With a gate voltage high than 0 V,number of holes decreases and electron density increases. Inversion: With a high gate voltage an inversion of carriers is created at the surface, having a increase of carriers at the surface.

There are different types of regime. First there is accumulation. When a negative gate voltage is applied, the band structure bends near the interface. In the metal part there is no electric field. In the Oxide layer is a linear electric field and in the semiconductor the band structure bends towards the same angle as the electric field has in the Oxide and then becomes flat further away from the surface. The valence band is bend towards the Fermi level. This electric field pushes away the electrons, while attracting the holes. Hole accumulation occurs. The opposite happens when the Gate Voltage is positive. Now the conduction band comes closer to the Fermi level and holes get pushed away, while the electrons get attracted. But when the gate voltage is much higher, you will see Inversion. The electrons get attracted to the surface, while the holes are pushed away and inverting the original doping result. This way a high carrier density can be reached, which we will use to create high capacitance and change the state from an insulating insulator to a conducting metallic state.

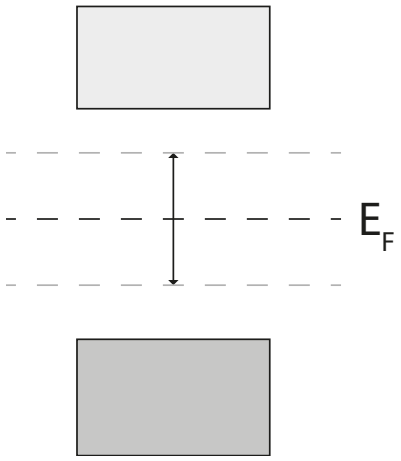

Figure 7: The Fermi level is in the band gap and can only shift a little bit up and down.

For a FET, we can only shift the fermi level for a little bit. Typical carrier density of 10^{12} cm^{-2} can be reached. There has to be found a new technique, where we can increase the shift of the Fermi level.

Ionic Liquid Gating

Another way to significantly tune Fermi level is with the help of an Electric Double Layer Transistor (EDLT) This EDLT has a thickness of 1 nm and typical carrier density can be $4x10^{13}$ cm^{-2} compared to 10^{12} cm^{-2} in SiO_2 FET. This is a very efficient way of gating, because of the high capacitance which can be reached with two EDLs. An Ionic liquid (IL) existing of small molecules with a size of 1 nm and a low Glass Transition temperature is used as doping material. The transition temperature is 190 K and ions are mobile at 210 K. A device as in figure 8 is made and the liquid is put on top. With this device, Ionic Liquid Gating[9] is possible with a capacitance up to 7 μF cm^{-2} compared to a capacitance of 0.03 μF cm^{-2} in a SiO_2 FET.

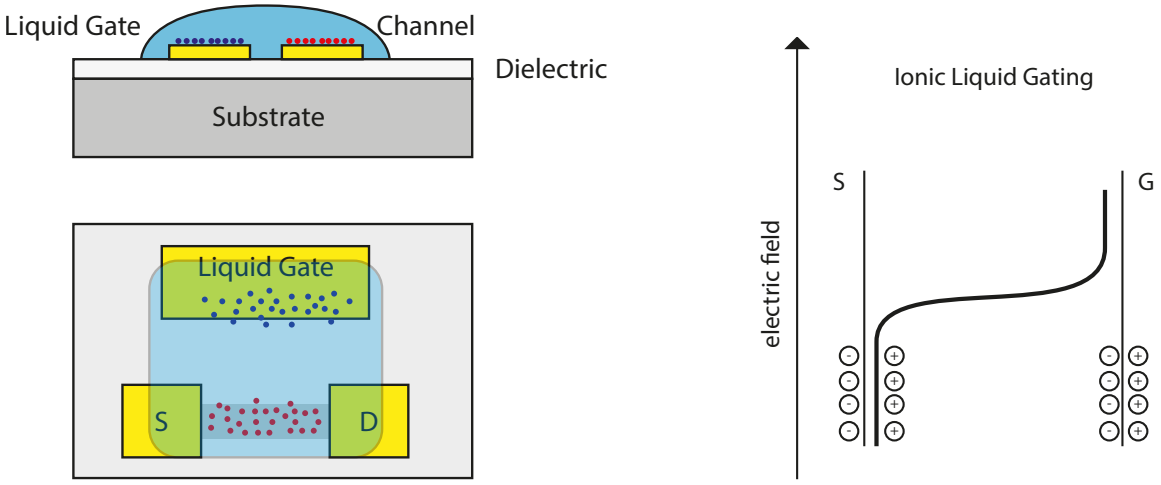

Figure 8: Glass Gating device. A back gate and a thin layer of glass with electrodes on top. Glass is the ionic medium facilitating the carriers for gating. Also a high range of carrier density is possible, comparable with ILG.

When a gate voltage is applied, all negatively charged particles accumulate at the gate. The positive ions are attracted to the channel and induce electrons. What is formed on the interface is called the Electric Double Layer (EDL) These ions create a channel, which makes it highly electron or hole conducting.

Because both anions and cations are in the IL, two EDLs are created. A high capacitance, determined by the thickness of the EDL (1 nm), of 2 orders of magnitude larger has been seen which results in a good on/off ratio. Because of this EDL the electric field is about 10 times larger than when using only SiO_2. The EDLT is very useful to study new electronic properties because of the high electric field which can be created at the surface. Ambipolar transport, electric field control of spin polarisation and circularly polarised electro-luminescence can be observed with the help of the EDLT. Also superconductor properties are found in these type of devices and can be studied.

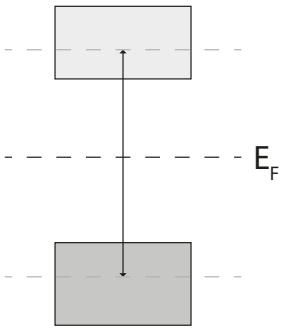

Figure 9: The Fermi level is in the band gap and can shift a lot more than in the FET.

Principle of Glass Gating

For Glass Gating[10] (GG), not an IL is used, but the liquid is replaced by the sodium ions in the soda lime glass. In this case, Sodium ions are the new ionic medium. A flake of WS_2 is used on top of the glass as channel material. This material has superconducting properties when it is monolayer and therefore very interesting to study. The optimal structure of the device would be a thin layer of glass. With a thin layer of glass and electrodes on both sides, a very strong electric field can be created. Therefore we aim for this design to have an optimal electric field at lower voltage.

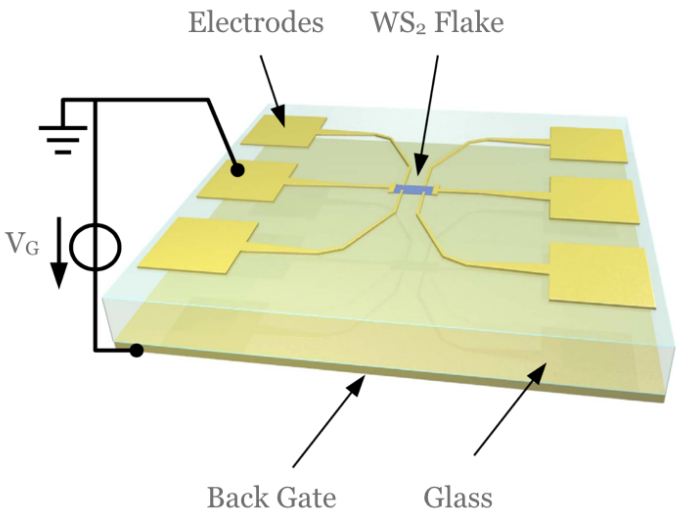

Figure 10: Glass Gating device. A back gate and a thin layer of glass with electrodes on top. Glass is the ionic medium facilitating the carriers for gating. Also a high range of carrier density is possible, comparable with ILG.

Soda Lime Glass Structure

Other than Silicon, glass is amorphous instead of crystalline. Glass is produced by mixing the basic components and heating this mix. Then the glass is cooled down quite fast to keep the un ordered structure. Soda lime glass is widely used in many applications. The name soda lime glass comes from the components of the glass which form good glass. The basic material is silica, but pure silicon forms a crystal, not useful glass. To achieve this, other materials are used. Two types of materials can be used for this: Fluxes and Stabilisers[11]. Fluxes are used to lower the melting temperature and stabilisers make the glass strong and water resistant.

Glass Composition							
constituents	SiO_2	Al_2O_3	Fe_2O_3	Na_2O	CaO	K_2O	MgO
percentage	72,3	0.5	< 0.02	13.3	8.8	0.4	4.3

Table 1: Glass composition[12] of the used microscope slides as ionic medium for our glass gating device.

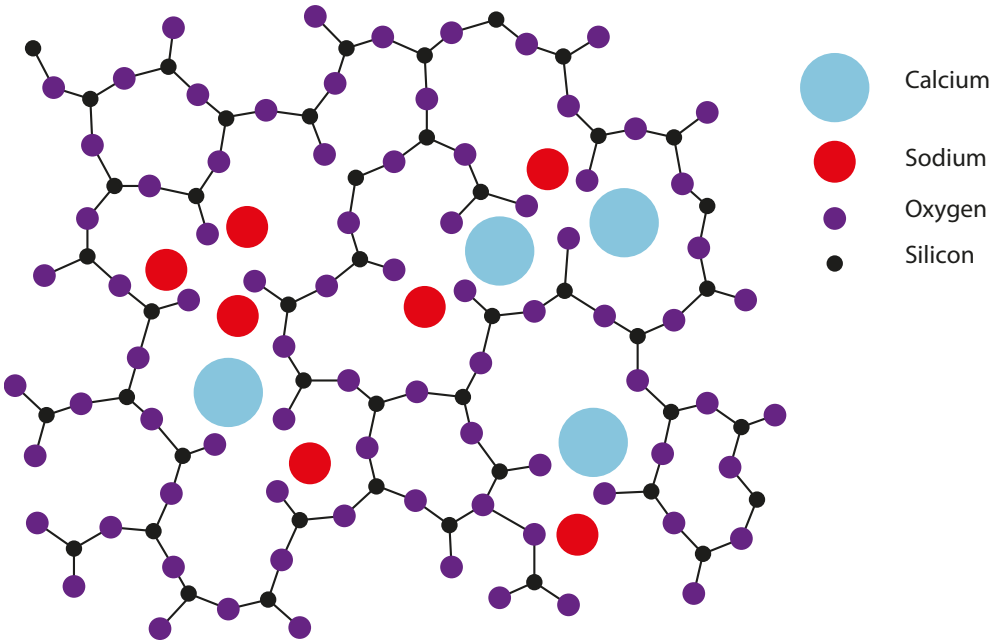

Figure 11: Soda lime glass structure. Mostly Silicon bound to Oxygen, with some Calcium and Sodium in between.

Because of the pollution from the other materials, soda lime glass is not a perfect crystal, but an amorphous material, making it easier for the ions to move at relatively low temperature. The ions are weakly bound to the Oxygen atoms which have a δ^- charge. Therefore in an electric field and at a temperature of 400 K, ions are able to move through the glass. The positive ions are attracted by the negative electrode and pushed away at the positive electrode.

Gating the Glass

When a positive gate voltage is applied, an electric field applies and the positive Sodium ions (1+) are pushed from the gate towards the surface were the sample is and accumulate at the surface. There the ions create an electric bilayer, which creates a channel on the other side of the surface from negative carriers and a current can flow.

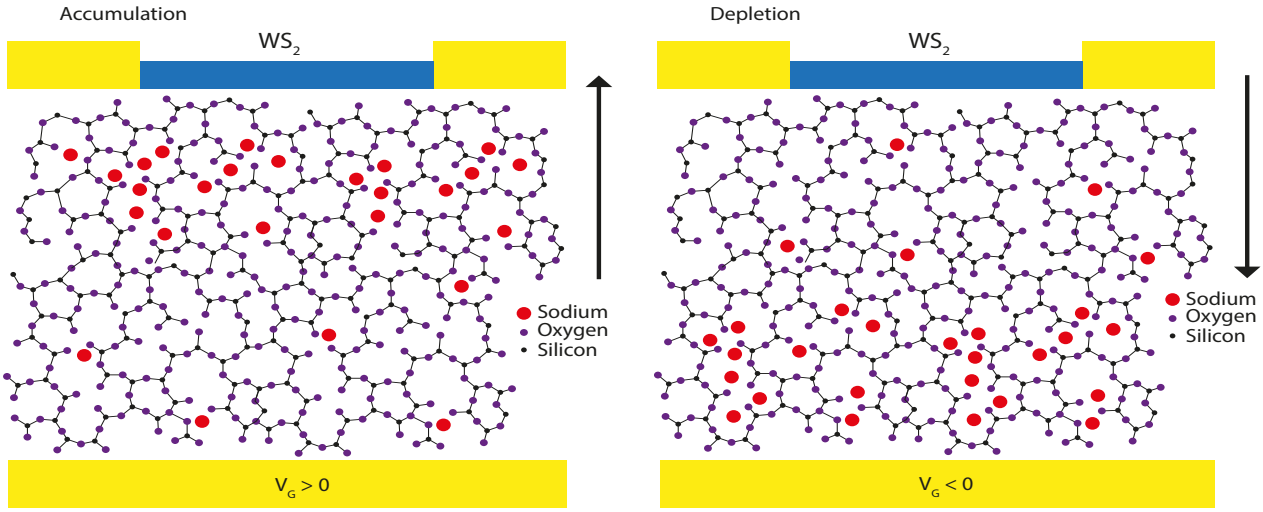

Figure 12: Accumulation (left): Sodium atoms get pushed away from the ionic gate, towards the surface of the sample, creating a positive charge at the surface. A thin layer of opposite charge will form a channel. Depletion (right): Sodium atoms are attracted by the ionic gate and removed from the surface. A positive charge at the surface is left and a negative channel will form.

When a negative gate voltage is applied, the ions move away from the surface, creating a depletion layer resulting in a positive carrier layer on the top surface. Only at high temperature (400 K) the ions can move. At lower temperature, the ions are trapped in the glass structure. This is useful, because the state can be frozen at low temperature (300 K). This way it is easy to test the resistance at different carrier densities. To make a comparison, earlier results from ILG are used and a glass gating device is fabricated.

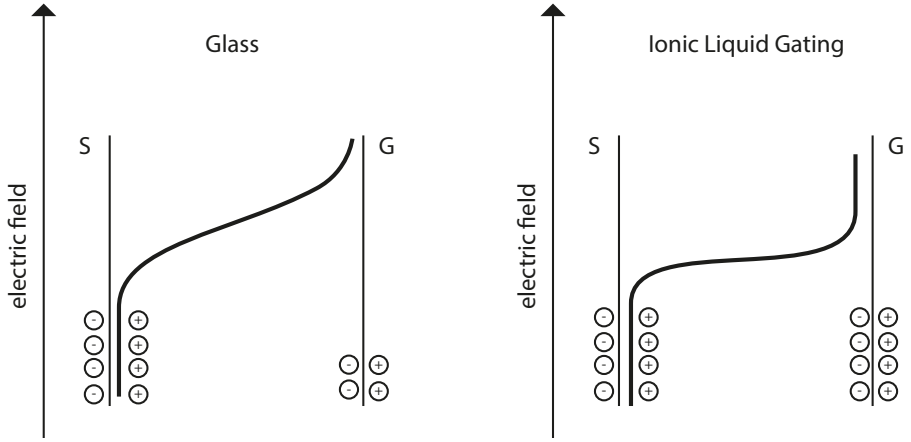

Figure 13: The electric double layers of both devices are shown here. On the left, a Glass Gating device with one strong bilayer and a weak bilayer near the gate. On the right an ILG device with two strong bilayers and therefore high capacitance.

Thin Layer of Glass

For optimal testing of this device, we would like to have a thin layer of glass. Then a back gate can be applied from the bottom surface and there is a large area on the back for the gate. This way a thin layer capacitor can be created. With a small back gate a large electric field can be achieved.

To make this thin layer, e-beam evaporator technique has been tried. Glass beads with extra sodium ions were ordered from the company and melted in a crucible to be loaded in the e-beam evaporator. Then a thin layer (30 nm) of glass has been deposited on a marked wafer. The result was a very non smooth surface, many nucleations are seen. Most likely, the stoichometry has been broken and the glass becomes highly reactive with the atmosphere. Foreign particles work as a catalyser and increases the nucleation rate[13]. The foreign particles lower the interfacial free energy and the atomic mobility is increased at the surface. Water from the air binds to the surface and the particles nucleate, which leaves a very rough and useless surface. Also the markers showed some reaction with the glass. From now on, unmarked bare wafer is used.

Next a sample of 100 nm glass was made. This sample has been annealed in the oven at 500 ºC overnight. After that the surface was still rough. The sample was submerged in water, which improved the sample a little bit, but the surface was still not smooth enough to use for a device.

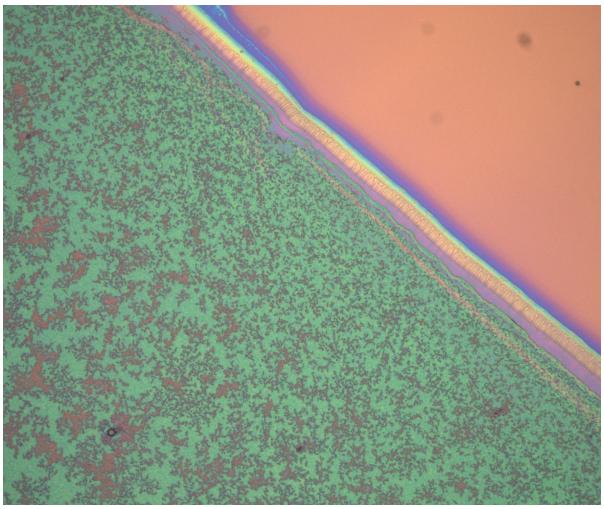

Figure 14a: First try of a thin layer of glass after E-beam evaporation. Very rough surface

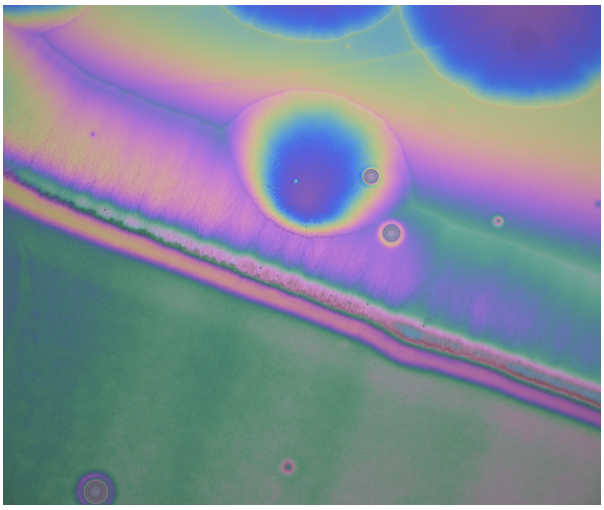

Figure 14b: Annealing changes the structure, but the surface is still not smooth.

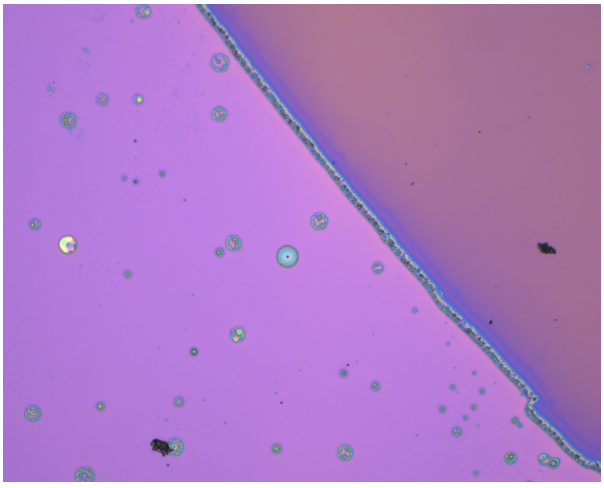

Figure 14c: Submerged in water. More smooth areas but a lot of nucleations

Annealing at 800 ºC for 1 hour and overnight has been tried. The sample for 1 hour did not look good and the sample overnight was clearly being baked at to high temperature.

Water treatment directly after deposition washes away all the glass particles and leaves us with only bare wafer.

One last option was reducing the time the sample gets exposed to air. A layer of glass (150 nm) is deposited on a wafer and transferred to the oven directly. There was no difference visible compared to the earlier experiments.

Therefore we did not make a thin layer of glass and used microscope object glass of thickness 1 mm, which also contains sodium ions. The disadvantages are a smaller gate area on top and the distance between the top gate and the sample has to be at least 1 µm. Which results in a less strong electric field because of the larger distance.

Figure 14d: Annealing for longer time, also not the solution. A lot of cracks, so far not smooth enough.

Because of this, the design of the device has to be changed. Now a gate on top of the material is used. A disadvantage is that the distance between channel and gate have to be 1 µm instead of 100 nm. This weakens the electric field, but the idea would still work. So the new design looks a lot like the ILG device, except for the part that there is no IL, but the ions are in our new Ionic medium, the glass.

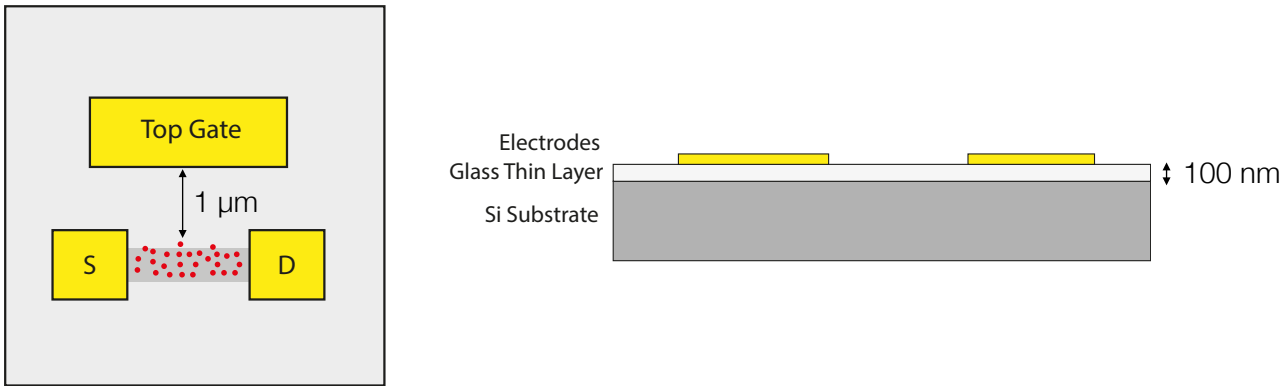

Figure 15: Left: new design for glass gating. When using a top gate on top, the distance becomes larger. Right: the old design. Use a gate at the bottom. This way a thin layer brings the electrodes very close together and a strong electric field can be induced.

WS_2 Flakes

The WS_2 flakes have been made by Chemical Vapor Deposition (CVD). In a tube, a reaction takes place, which creates the flakes. The process is thermally stimulated and takes place at high temperature. The following reaction results in the desired WS_2 flakes.

$WO_3 + S_2 \rightarrow WS_2 + SO_2$

The setup contains a furnace with a 1 meter quartz tube, which is heated to 750 ºC. Before the tube a container with Sulfur powder surrounded by a heater supplies the sulfur necessary for the reaction. In the tube, the WO_3 is placed and a wafer to deposit the WS_2 on. The setup is in vacuum.

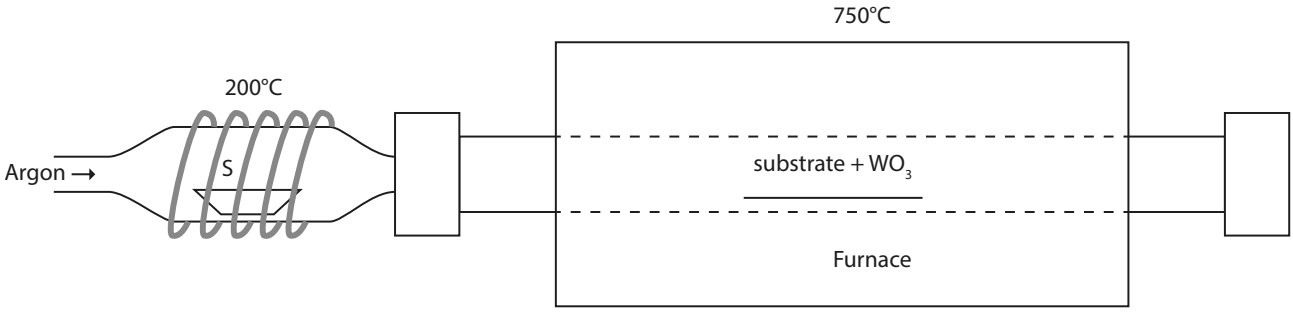

Figure 16: CVD setup. A heated container with Sulfur connected to a heated quarts tube at vacuum. Substrate and WO_3 in the chamber, purged with argon.

To prepare the CVD setup, the tube is filled with WO_3 and then the tube is purged with argon to remove any oxygen and get a steady flow. After that the tube get heated up slowly to a temperature of 750 ºC and the sulfur powder is heated to 200 ºC. Sulfur gas is in the tube now and WO_3 gets evaporated and after about 10 cm it condenses on the wafer. Once condensed it will react with the sulfur and then crystals will form. The growth time is typically about 30 minutes and the flow rate is 3 mm/s. After that the tube has to cool down slowly to room temperature by just switching of the heater. The result are large flakes with monolayer triangular WS_2 material. These can be selected for the use in samples to test the Glass Gating principle.

Fabrication Process

The device is fabricated on a object glass for microscopes, which is normal soda-lime glass. One of the components of this glass are sodium ions, which are used as gating ions instead of the ionic liquid. The glass has been cut in small pieces of 4mm by 4mm and has a thickness of 1mm, to make it fit in the chip carrier.
After the glass has been cleaned very well, by acetone and iso propanol and heating in an oven for some time, samples of WS_2 flakes are transferred on top of the glass. This has been done by the scotch tape technique, which is often used in Graphene studies.

- Previously made flakes are carefully selected under the microscope. Important is that there are many useful flakes, large areas of monolayer crystals are ideal. We used the wafers with most useful flakes, to have a large change of transferring some flakes successfully.
- First a polymer diluted in chloroform is put on our carefully selected wafer where WS_2 crystals have been grown on. Then the sample is baked at 180 ºC for 10 minutes, and cool down after that for 30 minutes.
- Then the sample gets submerged in liquid nitrogen to cool down. Now the sample can be transferred by tape to our glass substrate.
- First tape is put on top of the samples
- The tape with flakes is slowly removed from the wafer.
- Once the tape comes off completely, the tape with the flakes is put on top of the glass and leave the tape on top. After transfer, the sample still with the tape on top, has to be baked again for 10 minutes at 150 ºC and cool down to room temperature very slowly to form a good bond to the substrate.
- When the sample is at room temperature, the polymer can be diluted in chloroform and only the WS_2 crystals are left on the glass substrate.

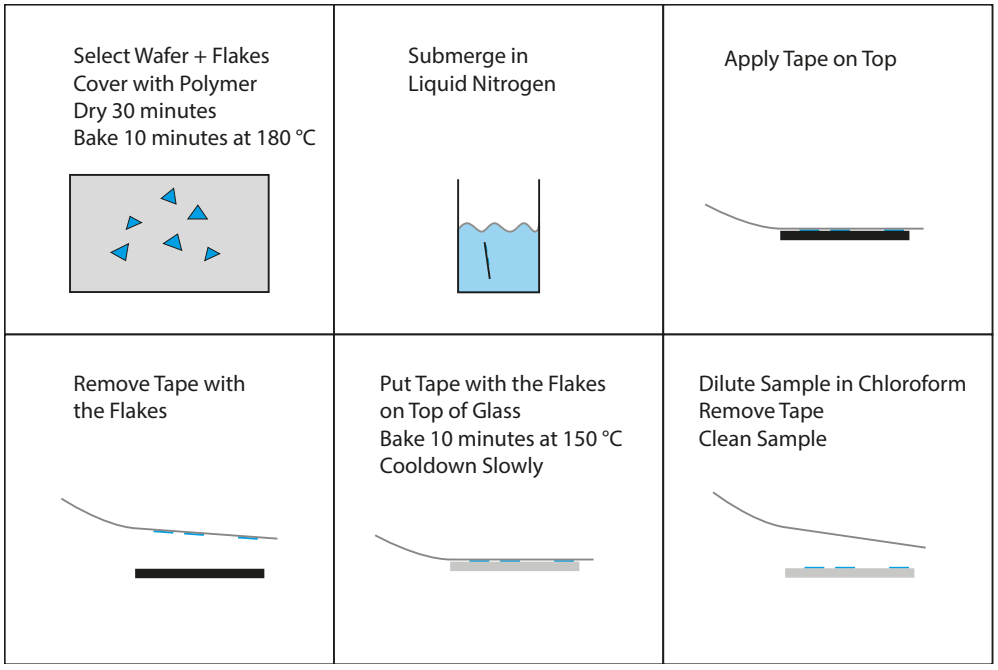

Figure 17: Steps in the flake transfer process.

- Now a good crystal with monolayer has to be found under the microscope. We recognise them by a very thin, part with low opacity especially at edges of flakes.
- Once one has been found, the position is notated and markers are printed around the useful flake. Then pictures are taken again to determine the position very accurate.
- A Hall bar can be designed around the flake with AutoCAD. One has to avoid that multiple electrodes cross the same flake, which will short both electrodes. Also excessive flakes around the one which gets used have to be etched away.
- The sample is covered with PMMA and pattern is printed with e-beam lithography on the PMMA
- The sample is developed in a mixture of MIBK and IPA (1:3) for 30 seconds. Everything which has to stay gets covered with PMMA.
- With the help of an ion beam and Oxygen, the flakes are removed by Reactive Ion Etching. After etching, the excessive PMMA gets removed and a circuit for the electrodes can be designed.

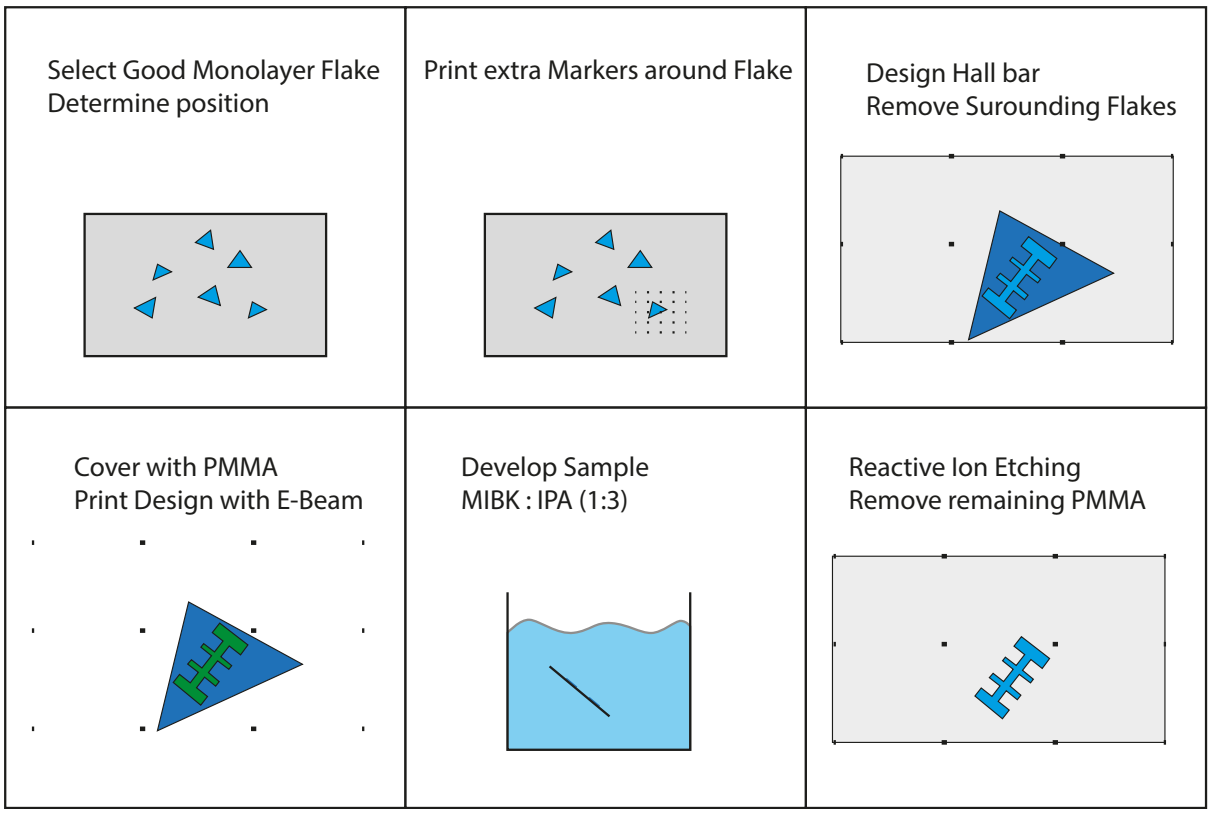

Figure 17: Steps in the etching process.

- Pictures are taken again under microscope and in AutoCad the circuit is designed.
- The sample is covered with PMMA and the designed electronic circuit can be patterned by e-beam lithography. Dose has to be lower than normal to prevent overexposure, because of the scattering in the glass is higher compared to silicon.
- The sample is developed in MIBK : IPA (1:3)
- The Ti/Au electrodes deposited on top in the E-beam Evaporator.
- After Evaporation lift off is done in Acetone for a few minutes at 60 °C.
- The device can be put in the chip carrier. After connecting the sample to the chip carrier, the device can be put in the measuring machine. To minimise the damage because of the atmosphere, the device has to be loaded immediately.

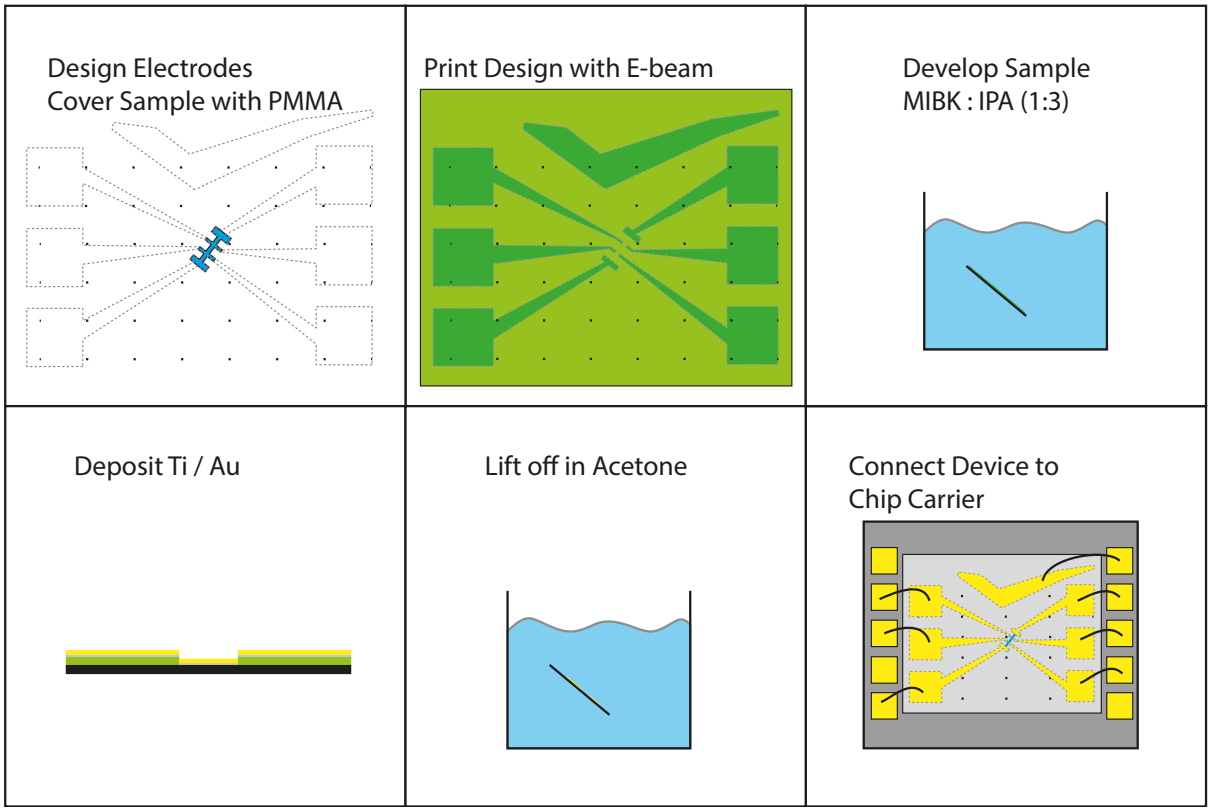

Figure 18: Steps in the deposition process.

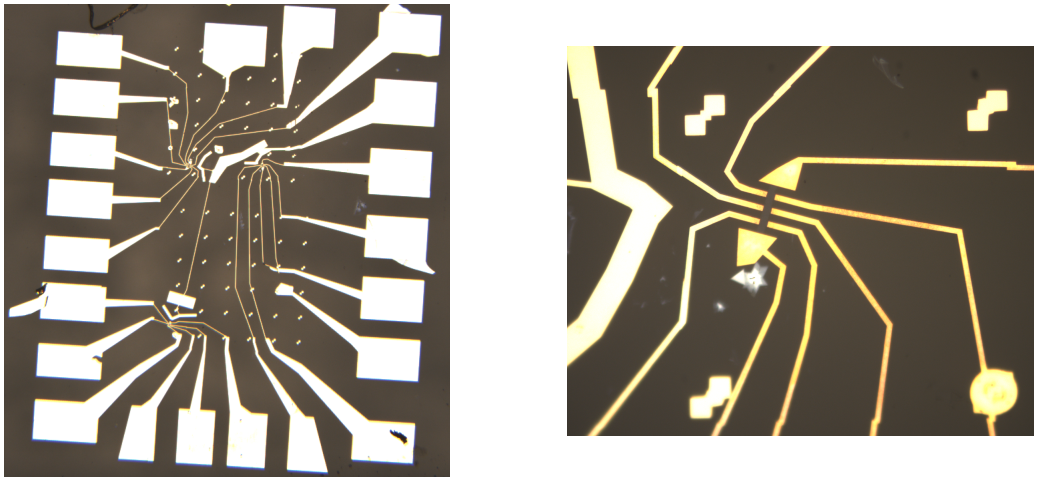

Figure 19: Final device. Flakes are connected by the electrodes.

Measurement Setup

The device has been measured in Janice. This cryostat works at a vacuum and the temperature can be controlled. Moreover it has a transparent window on top, which allows to perform an optical experiment. For this experiment, resistance, current and voltage are measured. The cryostat is a Liquid Nitrogen Cryostat which also can be heated. Temperature is controlled by Helium and a heater and the cryostat can reach a temperature range of 80 K to 400 K. The upper limit is due to the stycast in the cryostat which will damage at a higher temperature.

The machine as a multi-pin connector connected to every electrode, so a volt or current meter can be connected. The gate connection is a isolated cable, because higher voltages are used and this way less interference is created in the other signals. The gate voltage is applied with the DC Meter and Lock-in Amplifiers are used to apply current, measure voltage drop in probe configuration. A switch box makes connection multiple different terminals possible. A chip carrier has to be used to make the connection between the cryostat and the sample.

An application makes it possible to vary voltages applied and register and store the data collected. Also temperature is controllable by the computer, so experiments can be done semi-automatically.

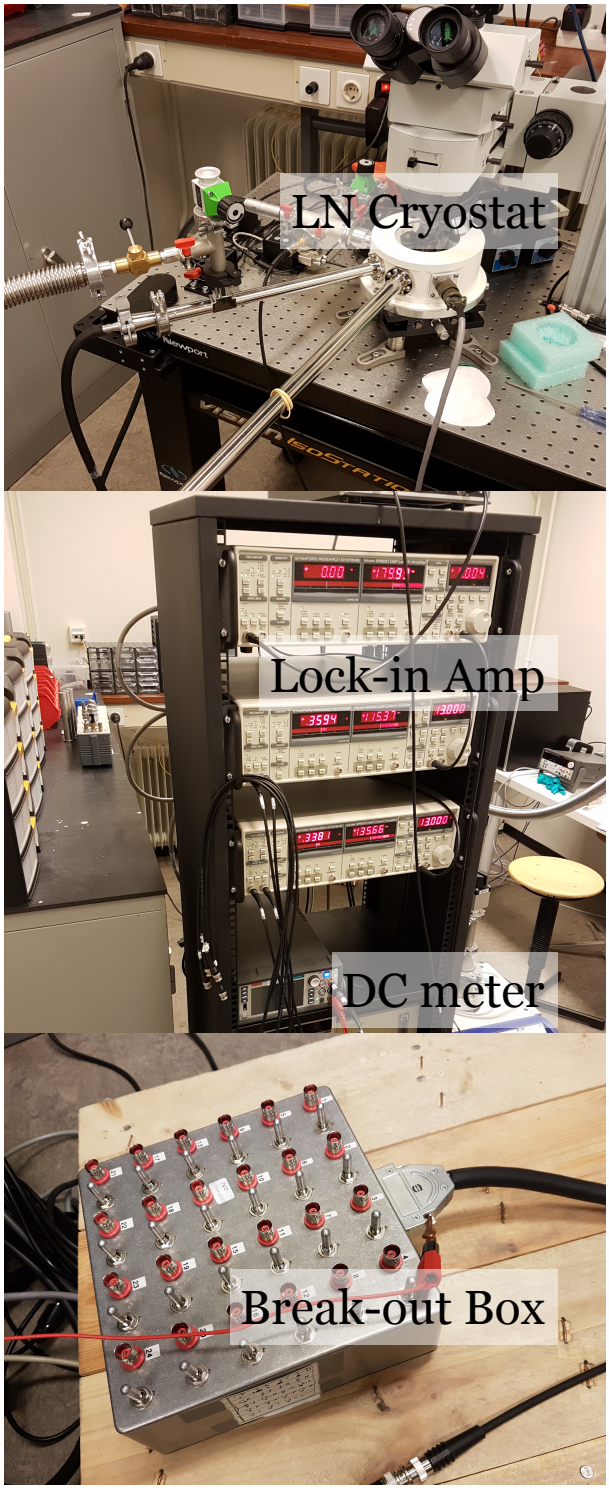

Figure 20: Measurement Instrument. Voltage applied by DC meter, connected by Break-out box to the sample. Lock-in Amplifier connected to computer to collect results.

Results and Discussion

At a temperature of 400 K the gating effect has been tested. The source drain voltage is set to 0.1 V. The gate voltage is increased by 1 V and then wait for 2 minutes. This is continued until there is a drop in the source drain current and the maximum current has been found. The gating effect becomes visible. Measurement is stopped at 18 V, to prevent destroying the sample by electrochemical reaction.

When gate voltage is kept constant, you still see a small increase of the Source Drain current. These are the ions moving through the glass, accumulating at the surface. Also you clearly see a peak around 16 V. Here the conduction is maximal because at lower gate voltage, the electrons do not have enough energy to overcome the band gap. After the peak at 16 V, the concentration of ions at the surface becomes so big, a high electric potential can be seen at the surface. This potential also contains large peaks, which can trap the electrons and is therefore limiting the current.
Also the surface is saturated with ions and ions will be removed from the surface, reducing the gating effect.

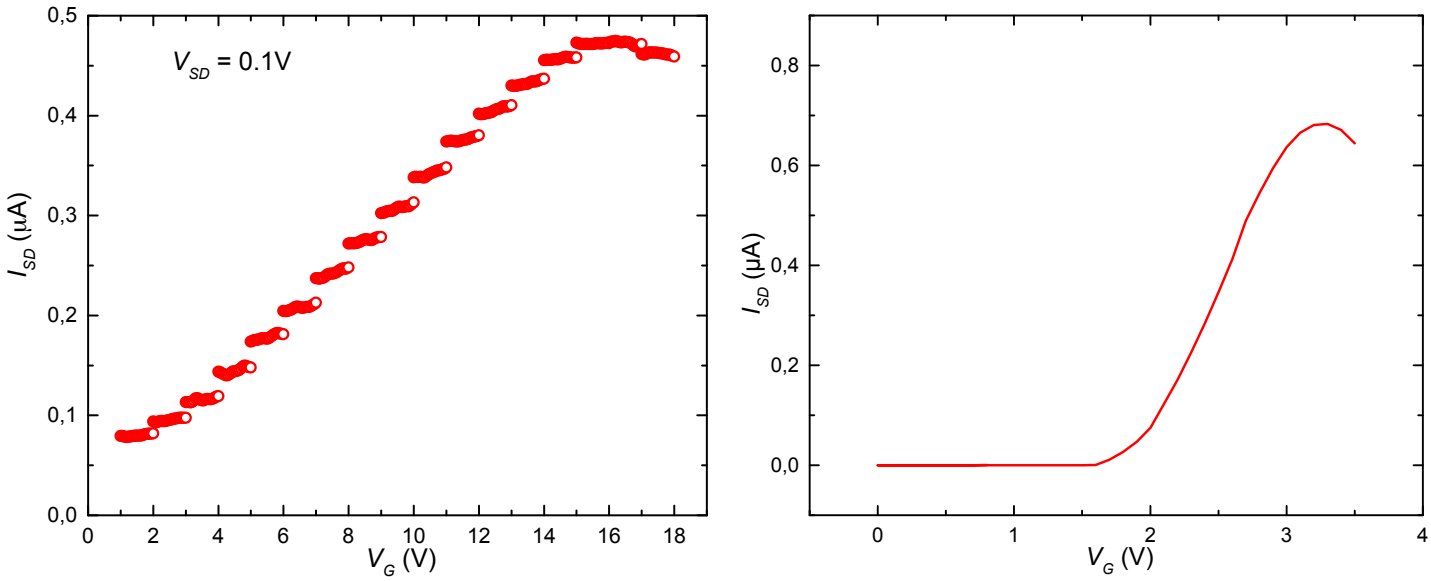

Figure 21: Left: Results from Glass Gating device. Gate voltage is applied, wait for 2 minutes and increase gate voltage. Right: Ionic Liquid Gating device. Gate voltage is slowly increased. Threshold value at 1.5 V for this device.

The same behaviour has been found in Glass Gating as in Ionic Liquid Gating. The same trend can be seen, but there are minor differences. First of all, there is a threshold value for ILG. The gating effect can be seen from 1.5 V in ILG, instead of 1 V or even lower for GG. The peak has been found at 16 V for GG and for ILG at 3 V. The current is in the same regime. If we can create a thin layer of glass and use a back gate, a stronger electric field can be created with a smaller voltage. This is because the distance gets smaller (~1 µm becomes 100 nm). Then a peak at lower gate voltage is expected. This way we can tune the device. Also change of temperature results in different speeds of diffusion.

At higher gate voltage the electrodes react, which you can tell by the change of color of the gold near the sample. The color on the negative side changes to a darker color because of this reaction. It is probably corrosion by the sodium atoms.
Therefore only at lower gate voltage (max 20V) measurements have been done to not destroy the sample.

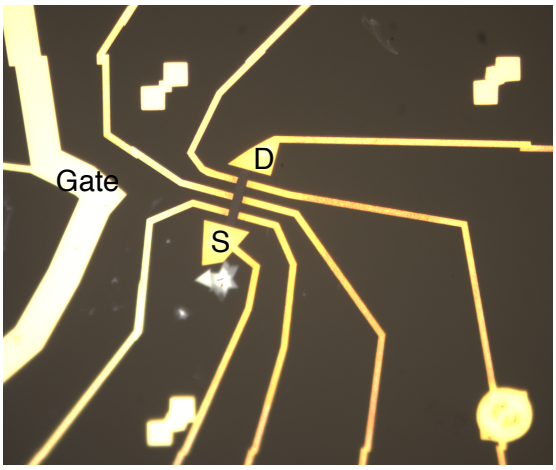

Figure 22: Electrodes on the right side change color because of a reaction with the material at higher voltage.

Now we put on a gate voltage of 18 V and measure the resistance, while changing the temperature from 400 K to 80 K. Than the gate voltage is released to 0 V. Because of the temperature, the sodium ions are frozen in the glass. When the sample is warmed up, ions slowly get removed from the surface and the sample becomes more metallic. The sample reaches a temperature of 330 K and stays at that temperature for 10 minutes. Then the sample is cooled down to 80 K and this cycle gets repeated multiple times until we find the most metallic state. These metallic states are very interesting, because they suggest superconductivity at lower temperatures. After the most metallic state, more and more ions are released and the sample becomes more insulating again. And we see more noise, because the fermi level is in the band gap again.

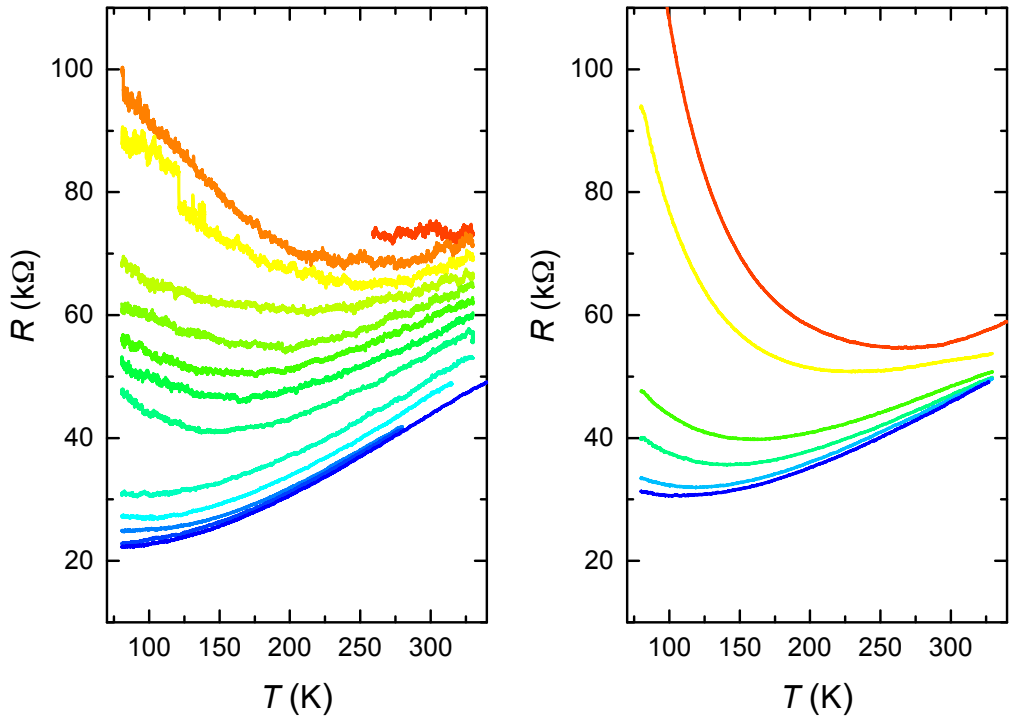

Figure 23: For Glass Gating. Left side: Start with low resistance and metallic state with average carrier density. Resistance increases when carriers diffuse into the material and carrier density reduces. Fermi level moves away from conduction band insulating state is found. Right side: Very insulating state at high carrier density. Electrons are trapped by the sodium ions at the surface. When the carrier density is reduced, the trapping effect becomes less and the resistance reduces.

First, when the carrier density is high, we see at the right side of the dome a reentrant insulating state. Here ions can trap electrons in the sample, so the ions cannot move. The electric field potential because of the ions close to the surface is very rough and can trap the electrons.

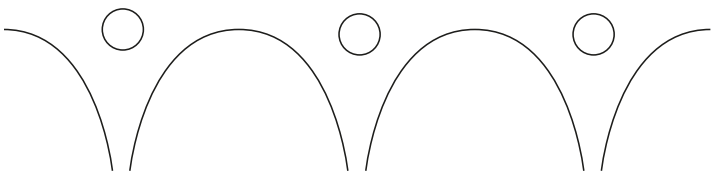

Figure 24: Visualisation of trapping potential. The sodium ions can trap electrons.

At the left side of the dome one can see normal band insulating state, because the gate voltage is not high enough for the fermi level, which is in the band gap. In between both limiting processes a metallic state has been found. This proposes a possibility of superconductivity, which can be studied further and makes this technique already very promising.

For ILG, we can see very similar behaviour. Therefore, we can use Glass Gating instead of ILG to reach the same result. The resistance is in the same range for both techniques. At the right side, we see a higher resistance. Because of the trapping potential which can better trap the electrons. A difference is that for Glass Gating you set the gate voltage to 0 V and the ions are diffused slowly through the glass depending on the temperature, reducing the sodium density at the surface. For ILG you have to apply a voltage any time, to keep the ion density constant. Therefore ILG is faster to control, but GG is more stable over time.

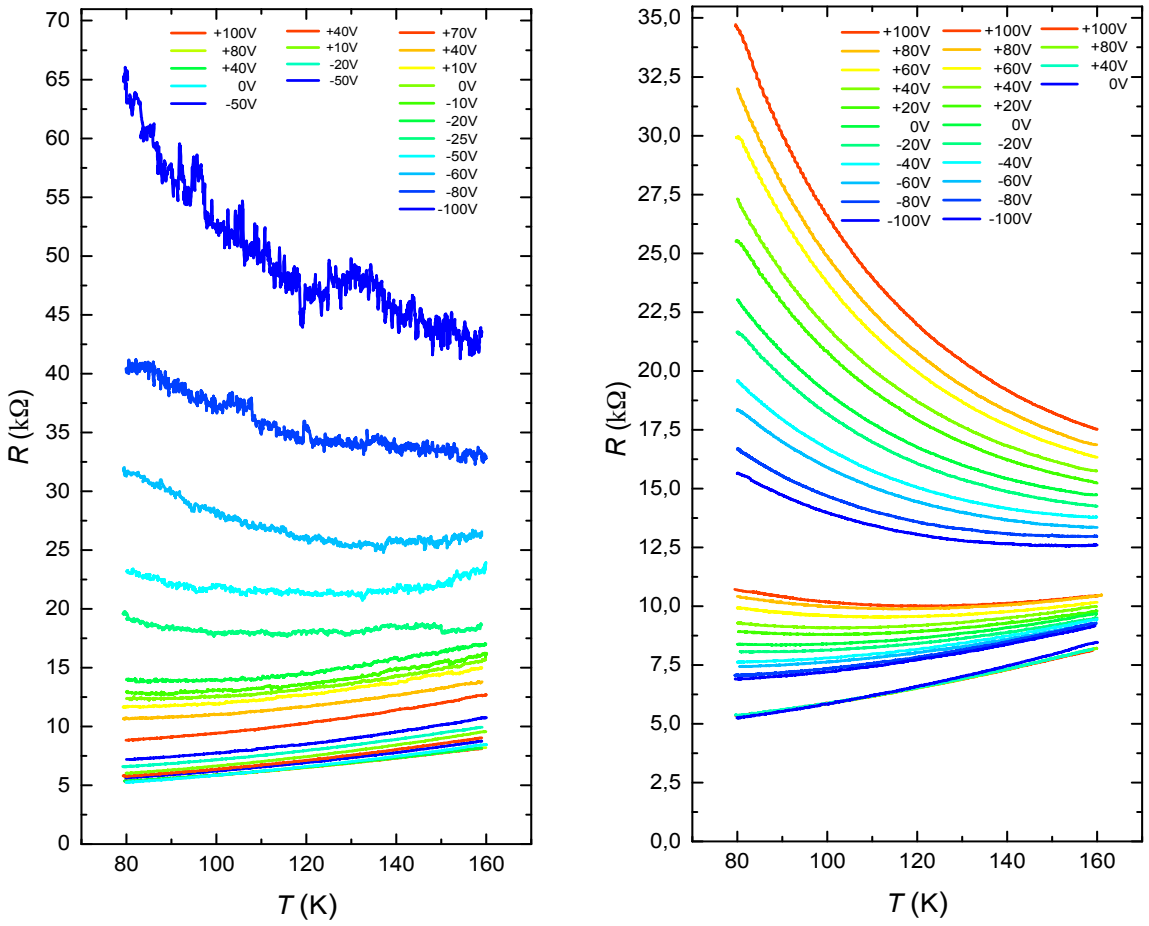

Figure 25: For Ionic Liquid Gating. Left side: Start with low resistance and metallic state with average carrier density. Resistance increases when carriers diffuse into the material and carrier density reduces. Fermi level moves away from conduction band insulating state is found. Right side: Very insulating state at high carrier density. Electrons are trapped by the sodium ions at the surface. When the carrier density is reduced, the trapping effect becomes less and the resistance reduces.

Depending on temperature and gate voltage or carrier density, a 2D colormap can be made. The color shows the resistance. Here we see at low voltage an insulating state. When the carrier density is increased, the metallic state becomes visible. But at to high votlage, the state becomes insulating again, the reentrant insulating state. Effective carrier density measured by Hall effect is decreasing when $V_G > 3$ volt, this is due to the trapping potential. This is what we saw in Figure 21 also.

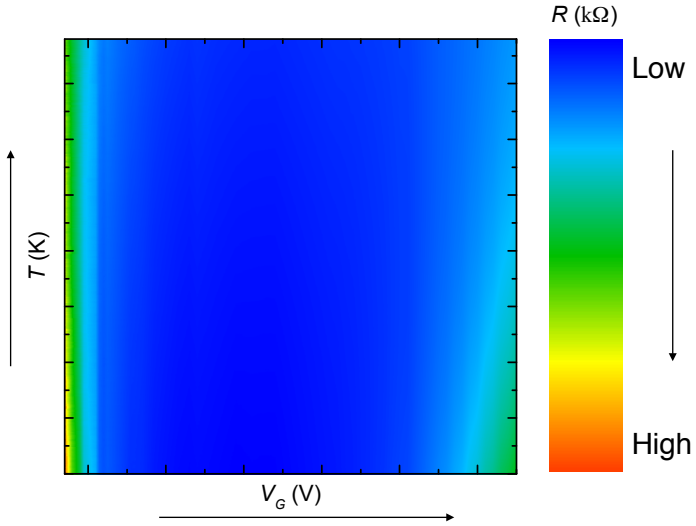

Figure 26: Temperature and Gate Voltage on axis, Color is resistance. Insulating stage on the left side at low carrier density. Metallic state at moderate carrier density and Reentrant Insulating state at high carrier density.

As you can see in table 2, Glass Gating has some advantages compared to Ionic Liquid Gating. Glass Gating technique works at higher temperature. Glass Gating technique is better controllable because of its slower response. And even more useful is that the surface is free to do other measurements like AFM or STM. Also for optical measurements, the Ionic Liquid will not interfere any more and influence the results.

Ionic Liquid Gating	Glass Gating
T = 220 K	T = 400 K
Size = 1 nm	Size = 6 Å
fast process	steady slow process, better control
Ionic Liquid on top	Free surface
Peak around 3 V	Peak around 16 V

Table 2: comparing Glass Gating and Ionic Liquid Gating.

Conclusion

We can compare both Ionic Liquid Gating and Glass Gating. Both show comparable results and therefore Glass Gating is found to be a working method. Gating effect was observed and also a metallic state has been found. Advantages of Glass Gating can be put to great use. For example to study quantum phenomena at very low temperature. The surface is free and makes it possible to study optical and geometric properties with AFM or STM. Glass Gating is very good controllable and is more stable over time. Unfortunately we were not able to create a thin layer of glass, which could improve the gating even more. But never the less, it has been shown Glass Gating is a very promising technique.

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