University of Groningen

Field Effect Tuning of Electrical and Optical Properties of Chemical Vapor Deposition Grown WS_2

Abstract:

Monolayer WS_2 is a direct bandgap semiconductor existing of one layer of WS_2 molecules. This paper presents WS_2 grown by chemical vapor deposition using two different methods and a comparison of these methods is given. The asgrown WS_2 will be used to produce a field effect transistor. It is found that photoluminescence intensity gives an indication of doping level and type of major dopands. Tuning the fermi level using a backgate can be used to determine the kind of doping. Subsequently a liquid ion gate is applied to inspect the complete PL dependancy on the gate voltage. The profiles are reasonably symmetric in accordance with theory. Different PL maxima are observed in different locations of the same flake.

Thomas Mutter S2212056

Contents

1 Introduction

Transition metal dichalcogenides (TMD) are a class of materials with the chemical formula MX_2. Where M is a transition metal from the groups IV, V and VI and X is a chalcogen (S, Se or Te) [1]. Tungsten disulfide (WS_2) is one of the TMDC's that has gained an interest over recent years. The material is classified as an indirect bandgap semiconductor. However once a WS_2 crystal is reduced to monolayer, the properties of the material change. One of the prominent changes is the change of bandgap from an indirect one to a direct one. The monolayers of WS_2 are also referred to as 2D WS_2 semiconductors. There are several ways to obtain the 2D TMDC, top down methods, but also bottom up methods. In this text a bottom up method called chemical vapor deposition (CVD) is used to grow 2D WS_2. Growing TMDC's using CVD was first reported in 2012[2]. In this report MoS_2 was grown onto a Si/SiO_2 substrate in a quartz tube oven. Two CVD growth methods will be used and compared. In the first method a quartz tube furnace with one heating element at low pressure will be used. The other method will make use of a furnace with three seperate heating elements at ambient pressure.

Two dimensional materials have started to get an increased interest since the discovery of graphene, which is monolayer graphite. Graphene has different physical properties than it's 3D counterpart graphite and these properties are what makes graphene interesting.[3] Graphene however does not have a bandgap limiting its applications in electronics. Monolayer WS_2 is classified as a semiconductor with a bandgap of approximately 2.0 eV. This makes the material ideal for the production of Field Effect Transistors (FET). [4]

This device, made from a different material (Si), is already widely used in applications world-wide. The reason why this material is of interest is because of its two dimensionality it brings preferable properties to the table such as a lack of dangling bonds, structural stability and a larger mobility than Si, which is currently used to make FETs. [1] Other properties of TMDCs are that some are superconducting under special conditions. TMDC semiconductors also introduce an extra degree of freedom, namely the valley degree of freedom. In short, TMDCs offer many interesting phenomena that can be investigated upon and perhaps used in future applications.

CVD growth produces a large variety of samples. A simple method of determining the quality of growth could aid researchers in selection of as-grown samples for the production of devices. A possible method of determining the quality of as-grown flakes might be selection based on photoluminescence (PL) intensity. In this text the response of the PL of a WS_2 FET device to a changing gate voltage will be investigated to see if the PL is only dependent on sample doping or wether there are other factors playing a role.

2 Theory

2.1 Two Dimensional WS_2

WS_2 is one of many TDMCs, in bulk it is structured of layers of two dimensional WS_2. These layers are held together by a van der Waals interaction. This structure is similar to that of graphite, which is made up of layers of graphene interconnected by a van der Waals interaction. This property makes WS_2 or TMDCs in general an interesting candidate for the production of two dimensional layers. The W & S atoms inside of a layer are bonded together via covalent bonds in the form of S-W-S. The crystal structure of the monolayer can assume two polymorphs: trigonal prismatic (AbA) and octahedral (AbC). The prismatic trigonal structure is displayed in figure 1. The terms between brackets indicate chalcogens (capital) and transition metal (lower case) stacking order. WS_2 is most often found to be in the trigonal prismatic phase, which is used in this work.[5] Three dimensional WS_2 is classified as an indirect bandgap semiconductor. However as the number of layers is reduced a shift in bandgap takes place making the material a direct bandgap semiconductor for the monolayer case.[1] This means that in monolayer WS_2 photons are easily absorbed and re-emitted, hence reasonably strong PL is present in this material. [6]

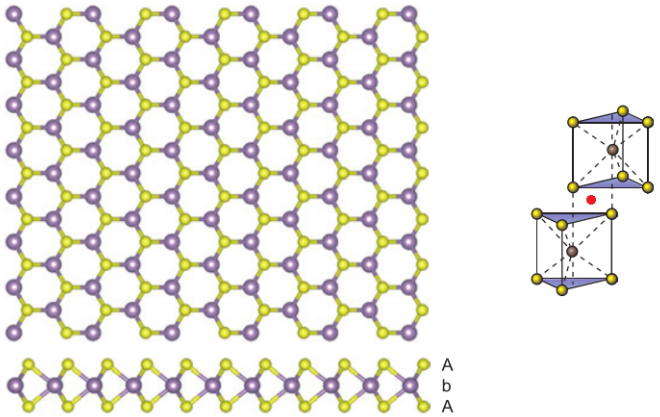

Figure 1: The crystal structure of monolayer TMDC. On the top left of the picture a topview of the monolayer crystal structure is displayed, on the bottom left the side view of monolayer WS_2 is shown and on the right the unit cell of WS_2 is shown, the red dot indicates the inversion center. Purple atoms represent W atoms and yellow atoms represent sulfur atoms. Image courtesy of Chhowalla et al and Wang et al. [5] [1]

The unit cell of WS_2, as shown in figure 1, has an inversion center. However it is seen that the unit cell is spanned over two layers of WS_2. In this text monolayer WS_2 is discussed. When the crystal is reduced from an even amount of layers to a single layer the inversion symmetry is broken. The breaking of

symmetry introduces the lifting of degeneracy of energy levels. In this case degeneracy of the valence and conduction bands are broken as will be discussed in more detail in the next section. [7]

2.2 Band structure

The band structure of bulk WS_2 is different than that of monolayer WS_2 as shown in figure 2. The band structure depends on the amount of layers of WS_2 present. [8] Bands indicate the available energies for electrons in a material. An energy band is the collection of all molecular energy levels that are formed when atoms in a solid start to form molecular bonds with one another. While more molecules bond together to form a solid there will also be regions in which no energy levels exist for the electrons to occupy. Theoretical calculations show that the bandstructure undergoes a change as the layers are decreased. The main observable change is that the conduction band minimum (CBM) at the T-point shifts in energy with respect to the valence band maximum (VBM) at the Γ-point up to the point that this energy gap is larger then the direct bandgap at the K-point.[8]

A direct bandgap indicates that in order for an electron to be promoted to the conduction band it only requires enough energy to cross the bandgap, it is a one step process where only an energy transition is required. But in an indirect bandgap the wave describing the electron must also undergo a change in momentum, this is a two step process, next to the transition in energy the electron also requires a transition in momentum which comes in the form of a phonon. A photon does supply momentum to the electron as well but this negligible.[9] Because a phonon is required to have a indirect bandgap transition of electron it becomes more unlikely that electrons are promoted to the conduction band.

Since energy bands are a representation of the energy state of a multielectron system it is reasonable to assume that once changes in the direct environment of this system will lead to a change in band structure, i.e. the occupation of levels may shift, this happens under thermal excitation or excitation with light. But also the peaks in the band structure can change. For such a phenomena to occur one needs to change the energy state of the system. When the amount of layers (z-direction) of WS_2 is decreased the band structure shifts from one with an indirect bandgap (multilayer) to one with a direct bandgap (monolayer). Because the layers are coupled together via a van der Waals interaction it means that the electrons are affected by this interaction. This means that the wavefunction will look different when the system is exposed to a van der Waals interaction with respect to when it is not exposed. Hence changing the hamiltonian that describes the energy of the system.

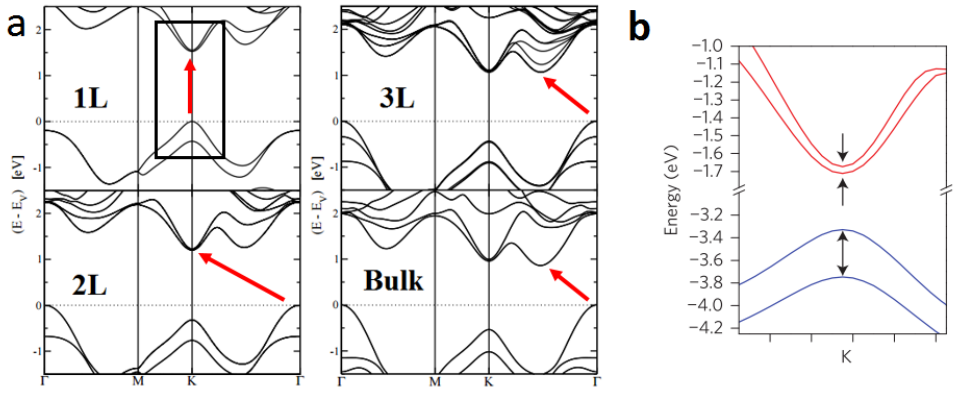

Figure 2: On the left four different band diagrams are visible. a: The red arrows indicate the bandgap of the crystals. 1L, 2L and 3L stand for mono, bi, trilayer WS_2 respectively. The black square in the 1L band diagram is zoomed in upon and displayed in b. b: The spin splitting of the valence and conduction band is visible. Arrows indicate the size of the splitting, not the spin preference of the bands. Images courtesy of [10] and [11].

Due to the breaking of inversion symmetry the effect of the strong spin orbit coupling in the material becomes visible in the band structure [7]. It is seen that the valence and conduction band have split, which is the lifting of the degeneracy of the energy levels as discussed above. Without this splitting the energy levels for spin up and spin down electrons are degenerate, in this situation however spin up and spin down electrons have different energies which is shown as splitting of the valence and conduction bands. But this is not the only new phenomena. In the image on the right in figure 2b only the bandstructure at the K-point is shown. At the -K-point, also known as K'-point, the bandstructure is exactly the same except for the energy levels for the spin-up and spin-down electrons. These energy levels are exactly opposite of the ones in the K-point. This is a result of conserved time reversal symmetry which states that the conduction band states at the (K,s=-1/2) and (-K,s=1/2) should be degenerate. [11] Another results of the breaking of the symmetry is that electron interband transitions at the K-point can only be occur under the absorption/emission of right handed circularly polarized light (σ^+) whereas at the K'-point electron interband transitions can only be occur under the absorption/emission of left handed circularly polarized light (σ^-) as shown in figure 3. [12] Hence electrons in the K-point can be distinguished from electrons in the K'-point by simply observing the polarization of light that excited electrons emit. Also, because of the combination of spin splitting and the valley dependent polarization electrons with certain spin can be excited using the right kind of light polarization which can be useful in spintronic applications.

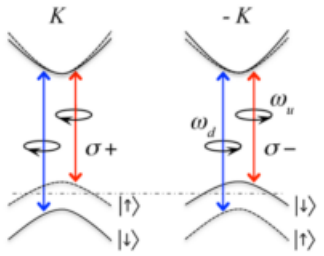

Figure 3: Valley dependent optical selection rule. At the K-point only right circularly polarized light can excite carriers whereas for the -K-point only left circularly polarized light can. ω_d and ω_u are the frequencies of the two excitons. Image courtesy of Xiao et al. [12].

2.3 Electrical Transport

In semiconductors electrons can only conduct current when they are in the conduction band. When an electron is promoted to the conduction band there is a non occupied energy state in the valence band. This non occupied energy state can be seen as a quasi particle which is called a hole. Holes can be seen as if they are electrons with positive charge (+e). Hence a semiconductor has two types of charge carriers: electrons in the conduction band and holes in the valence band. In intrinsic semiconductors there are an equal amount of conduction electrons as there are holes at a finite temperature. The rate at which electrons and holes move through a material under influence of an electric field is called mobility (μ).

$$\mu = \frac{|v|}{E} = \frac{e\tau}{m} \tag{1}$$

Where v is the drift velocity which for a charged particle equals $q\tau E/m$ where q is the charge of the particle, τ is the collision time, E is the electric field and m is the mass of the particle. The electrical conductivity (σ), which is an indication of how well your material can transport charge, is then found to be:

$$\sigma = e(n\mu_e + p\mu_h) \tag{2}$$

Where n(μ_e) and p(μ_h) are the concentrations(mobilities) of electrons and holes respectively. [9]

Conduction depends on the ability of electrons to propagate through matter. When electrons propagate through matter they meet many obstacles, also called scattering centers. The more scattering centers there are the more difficult it becomes for an electron to travel a certain time without scattering. This time is know as the collision time mentioned above (τ). τ depends on the environment of the charge carriers. There are several mechanisms for charge carrier scattering. There are four main contributions: optical and acoustical phonons scattering,

coulomb scattering at charged impurities, surface interface phonon scattering and roughness scattering. [1]

2.4 Photoluminescence

PL intensity depends on the ability of a material to absorb photons and re-emit photons. A quantative description of this ability is called the quantum yield (Φ). Quantum yield of a material is defined to be:

$$\Phi = \frac{\#\,\text{photons emitted}}{\#\,\text{photons absorbed}} \tag{3}$$

This quantity will always have a value ranging between zero and one. There are several properties that affect this value, e.g. the reflectivity of the surface of the material, the doping of the material and the bandgap of the material. A measure in which the amount of PL can be expressed is the rate of recombination (R), which is proportional to the electron and hole densities (n and p). When the Fermi level (E_F), which is the energy level above which no occupied electron states are found at zero kelvin, is in the center of the bandgap an equal amount of electrons and holes will be created under the excitation of light. If the semiconductor is doped however, the Fermi level will either be raised or lowered, depending on the doping. What this means is that extra energy states have come available for either electrons and holes (depending on the impurity doping) in the form of either elements with one more or one less valence electron then the "host" material. When these atoms give up an electron to the conduction band or accept an electron to create a hole in the valence band no electron-hole pair (exciton) that radiates light under recombination is created. This means that the PL intensity will be also dependent on the position of the Fermi level in the band diagram. Doping can also be done by applying a gate voltage to the material. The electric field imposed on the material essentialy raises or lowers the Fermi level in the conduction or valence band respectively allowing for a current flow and resulting in a reduction of PL as shown in figure 4, this is because as the charge carriers gain more energy from the electric field it means that there is a larger chance for the charge carriers to be excited thermally into the conduction or valence band and remain there for a longer period of time, effectively reducing the recombination rate. Hence this directly relates to the quantum yield in a way that the more the Fermi level deviates from the center of the band gap the lower the quantum yield becomes. Besides excitons also trions are a quasiparticle that can be found in monolayer WS_2. Trions are excitons bound with an electron or a hole, negative or positive trions respectively.

2.5 Field Effect Transistor

A field effect transistor (FET) is practically a switch. It either conducts current or it does not. This property makes FETs very useful for the making of computer chips. Moore's law predicts that the amount of transistors that will fit on a chip

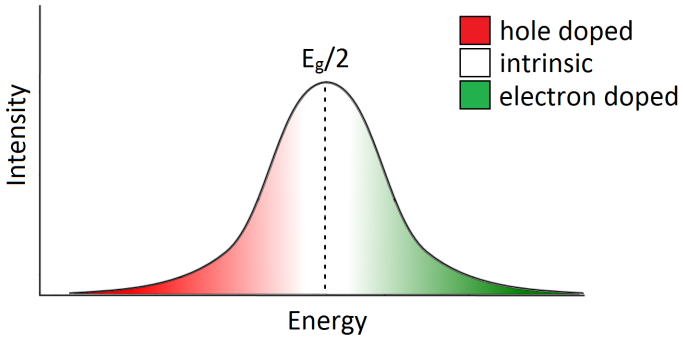

Figure 4: Intensity plotted against energy, which is directly related to the gate voltage applied on a transistor. The Fermi level can be tuned using gating methods. As the Fermi level shifts from the center of the bandgap towards the conduction band the material becomes electron doped, indicated by green in the graph. As the Fermi level shifts towards the valence band the material becomes hole doped, indicated by red in the graph. The PL intensity reaches a maximum when the Fermi level is in the center of the bandgap.

doubles approximately every two years [13]. But humanity is approaching the limit of the amount of FETs that can fit on a single chip. Hence transistors that can have more degrees of freedom then the present FETs have are needed. The TMDCs may be the material that can be used in these transistors, for example one of these extra degrees of freedom could be the optical selection rule in different valleys.

A general FET is made out of a semiconductor, three metal leads and a dielectric material. The working principle of a FET is simple. Two of the metal leads are used as source and drain and form a closed loop with the semiconductor. The third metal lead functions as a gate lead. This lead is connected to the dielectric material. Essentialy a capacitor is created. One can regulate the electric field produced in the semiconductor by using different voltages. Since in a semiconductor a bandgap is present, it means electrons can only conduct current under the right conditions. The electric field that is introduced into the semiconductor by applying a voltage to the gate electrode provides the electrons with the energy needed to cross the bandgap into the conduction band so they can conduct current. This current will flow from the source electrode towards the drain electrode.

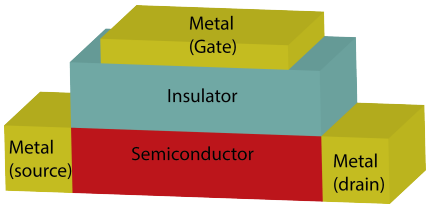

Figure 5: Structure of a field effect transistor

There is more then one way to apply a gate voltage to the transistor. The two methods that will be used for this report are backgating using an oxide and liquid ion gating. The difference between the two is first of all the state of matter, one is liquid and the other is solid. In liquid gating also the position of the ions and hence the charge accumulation can be controlled by using different ratios of gating voltage (V_G) and source-drain voltages (V_{SD}). In general the rule goes as follows, when $V_G >> V_SD$ then one type of charge is accumulated at the surface of the semiconductor but when $V_G << V_SD$ the two types of charge accumulate near source and drain electrode essentialy creating a PN-junction. [14] For the purposes used in this report only the first charge configuration is used.

A Schottky barrier forms when a metal and a semiconductor are put in contact. Due to the fact that the Fermi level and the work function of both materials are different, bending of energy bands will occur which will lead to the formation of an internal potential barrier ($e\phi_b$) as shown in figure 6 a, in this figure the band diagram for a Schottky barrier is shown, in this case the junction of a metal with a n-doped semiconductor. E_v and E_c represent the valence and conduction bands respectively. W is the depletion zone. E_{F_S} and E_{F_m} are the Fermi levels of the semiconductor and the metal respectively. Finally $e\phi_m$, $e\phi_b$ and $e\chi_S$ are the work function, barrier height and electron affinity respectively. For electrons to get from the metal into the semiconductor they have to tunnel through this potential barrier. So that means that in both the metal and the semiconductor energy states with the same energy need to be available for the electron to tunnel in. Because in a non biased schottky barrier the Fermi level of the metal aligns with the Fermi level of the semiconductor this means that these states are not available without external influence. This is because the Fermi level of a semiconductor lies inside of the bandgap where no electron states are available. So to get a current flowing a Metal Insulator Semiconductor (MIS) capacitor is used. [15]

The MIS can be viewed as three layers of material stacked on one another, first the metal, then the insulator and then the semiconductor. When a voltage is applied on the metal an electric field is induced in the semiconductor, this electric field is not homogeneous throughout the whole semiconductor but degrades over distance. However we are working with a two dimensional material so that means whereas in literature for 3D materials is spoken about conduction happening at the Insulator-Semiconductor surface we can simply speak of our

flake, since essentially it is just a surface. This electric field attracts either electrons or holes depending on the sign of the bias. Attracting holes or electrons can be viewed in the band picture as the bending of bands, downwards bending for attraction of electrons and upwards bending for the attraction of holes as seen in figure 6 b,c,d. This bending can result in alignment of either the conduction band (figure 6d) or the valence band of the semiconductor (figure 6b) to reach the same level as the Fermi level of the metal and hence at both sides of the potential barrier of the Schottky barrier there are now free states and electrons can tunnel through the barrier to proceed to conduct current. [15]

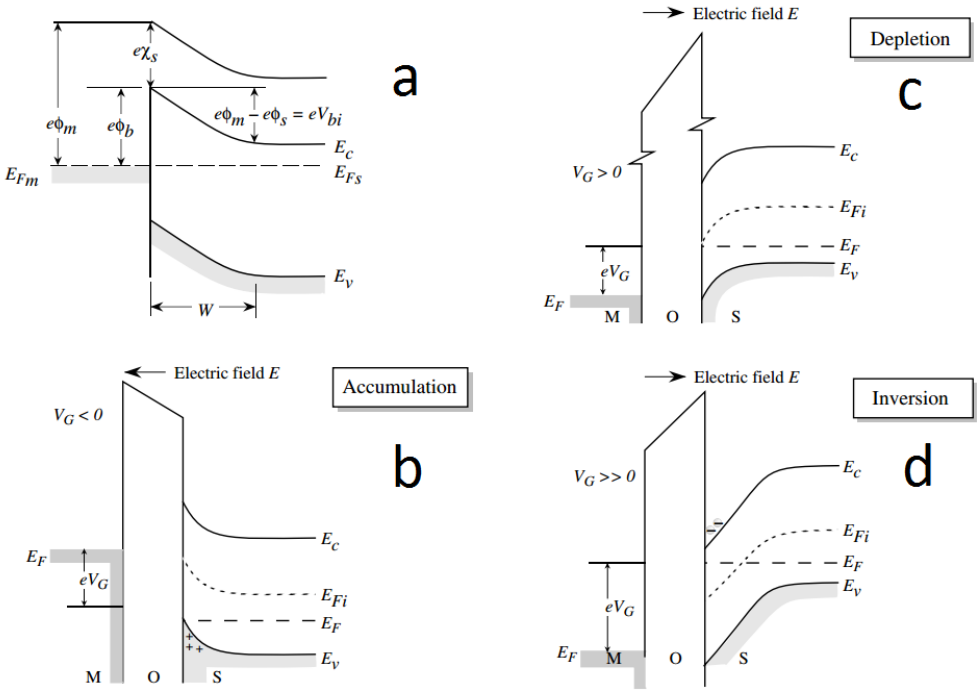

Figure 6: a: Schottky barrier band diagram. b,c,d: banddiagram of MIS under various gate voltages.

2.6 Ionic liquids & Electronic double layers

As mentioned above besides the conventional SiO_2 backgate method one can also use an ionic liquid gate. In this case a droplet of liquid containing positive and negative ions is deposited on top of the sample. When a positive gate voltage is applied to the top electrode it attracts the negative ions and pushes the positive ions towards the counter electrode. At the interface of the electrodes

a layer of positive or negative ions forms attracting negative or positive charge carriers respectively in the electrode. These two layers are called the electric double layer (EDL) and can be seen as a very thin capacitor. It is made up of the charge carriers in the electrode, the ions attracted to this electrode and the gap is formed by solvents that are attracted to the ion. Hence the capacitor gap is proportional to the diameter of these solvates which can have a magnitude ranging from 0.1 nm to 10 nm. [16] A comparison of electric field supplied by the capacitor between backgate and ion liquid gate shows that liquid ion gating is a much more efficient method of accumulating charge at a surface.

Using the simple equation:

$$E = \frac{V}{d} \tag{4}$$

In which E is the electric field, V the gate voltage and d the distance of the gap. For the liquid ion gate a maximum voltage of 5V can be used and the gap thickness is around 1 nm resulting in an electric field of 5000 MV/m whereas for a SiO_2 backgate with a thickness of 300 nm and a maximum voltage of 100V the electric field is 330 MV/m.

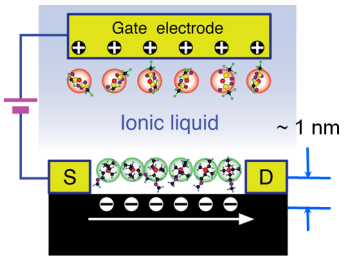

Figure 7: Schematic of the ionic liquid gating method. A potential difference is applied to the gate electrode and the source electrode causing attraction of positive ions to the SD channel and attraction of negative ions to the gate electrode. The EDL is represented by the positive ions and the negative charge carriers in the semiconductor.

3 Material & Growth

The semiconductor material, tungsten-disulfide (WS_2), is grown by Chemical Vapor Deposition (CVD). In this method the required material is a result of a chemical reaction that has occurred in an furnace of some sort. There are multiple methods to grown materials by CVD. One of the more popular methods is to use tungsten-trioxide (WO_3) powder and sulfur (S_2) flakes/powder as precursors.

3.1 Growth mechanism

The growth mechanism of monolayer TMDC on top of Si/SiO_2 using the CVD method is still under debate. Several propositions for this mechanism have been made. Two of them stick out. The first one is that suboxides form in vapor phase and attach to the substrate after which it serves as a nucleation center for further growth.[6] The second states that the whole reaction takes place in the vapor phase and the readily formed WS_2 subsequently attaches itself to the substrate. [17] Cain et al. also report about a mechanism for nucleation centers of the growth. They have investigated the seeds from which WS_2 typically grows and have concluded that these seeds exist of a oxi-chalcogenide core, in their case $MoO_{3-x}(S,Se)_y$, which is then covered in a TMDC fullerene shell. They propose that these nanoparticles form in the vapor phase and subsequently attach themselves to the Si/SiO_2 surface, then it acts as a heterogenous nucleation center for further growth of WS_2.

Crystal growth depends partially on the free energy of a surface. In 2D layers this surface is reduced to the edges of the crystal because the top and bottom surfaces have fully satisfied bonds. Wang et al. state that the growth pattern of the crystal depends on the ratio of transition-metal (M) to chalcogenide (X).[18] The ideal ratio is 1:2 as the chemical notation of WS_2 tells you. However precise control of this ratio is difficult when growing with furnaces. One can not precisely determine the concentration of M or X at points in the growth tube. Termination edges of the crystal growth therefore depend the M:X ratio. The termination edge of the growth will exist of either chalcogen atoms or transition metal atoms. In the case where there is an abundance of transition metal atoms, the sulfur terminations will grow faster, because the M-X bond is more favorable than a M-M bond. The same happens for the reverse situation where the environment of the growth substrate is rich in chalcogen. Only then the transition metal termination edges will be growing quicker for the same reason. One would also expect a difference between growth in a chalcogen rich environment with respect to a transition metal rich environment because at the termination edges both atoms have different energetic states. In the case for tungsten and sulfur, the tungsten atom can form bonds with six sulfur atoms, at the termination edge four of the six bonds are satisfied. Sulfur atoms on the other hand form bonds with three different tungsten atoms in the energetically favorable composition so at the edge one of those bonds will be unsaturated. Hence the situation is energetically different and it seems reasonable to expect different growth patterns for both situations.[18]

Another growth mechanism is proposed by Cong et al. [6] They state that first flakes of WO_yS_{2-y} are formed on the Si/SiO_2 wafer, these are quite thick. Further sulfurization produces WS_{2+x}, because the apexes of the triangles may be very reactive sites several triangles will merge together forming a larger flake. With continuous heating the thick WS_{2+x} will expand and become thinner fabricating monolayer WS_2. They state that because the center of these triangles is exposed to sulfur the longest this may cause the loss of sulfur in the center and explain why monolayer flakes have a reduced PL in the center.

3.2 Tunable parameters

To influence the growth both setups used have several tunable parameters. Each parameter has an effect on the concentration of both reactants inside of the oven. Both methods differ in tunable parameters, but the most important ones are present in both. These parameters are: Temperature of S_8 and WO_3, flow rate of the carrier gas Ar and the amount of precursors used in the reaction. The temperature is important because to introduce the reactants into the oven one must first sublimate them. Temperature also determines the vapor pressure of the material. This is the pressure molecules in the solid feel exerted on them by the solid. If this pressure is larger than that of the atmosphere sublimation will take place. In a sense this also determines the kinetic energy that the atoms will have. For growth one can imagine that if particles have to much energy they will not settle easily on the growth substrate. The flowrate is acting as a mixing mechanism. As both S_2 and WO_3 are sublimated at different locations in the tube they need to be brought together. For this a pressure drop must be created over the tube and this is the function of the Ar gas, another way of viewing it is that the Ar gas molecules will push the sulfur atoms towards the sublimated WO_3 so that a reaction will take place. Again, if you introduce a higher flowrate you will increase the kinetic energy of the particles in your system. The amount of precursors added will have an effect in the stoichiometry, in the ideal case one would have two sulfer atoms for one tungsten atom. One could take two grams of sulfur for each one gram of tungsten but in practice not all of these atoms will "meet" and form bonds together. The ratio of tungsten to sulfur also has an effect on the shape of growth[18] as explained above.

3.3 One zone furnace

This setup consists of:

- Oven with one heating element
- Quartz tube
- Band heater
- Cold trap
- Argon gas source
- Vacuum pump

The materials used in this setup are WO_3 powder, S_2 powder, Si/SiO_2 substrates and Ar gas. To be suitable for monolayer growth the Si/SiO_2 substrates first need to be cut from a large preordered Si/SiO_2 wafer and cleaned. The cutting is done by a diamond tip, whom makes fracture lines in the Si/SiO_2 surface. Before scratching fracture lines into the Si/SiO_2 wafer the wafer is coated by PMMA. This is done to avoid further scratching of the surface by residu particles from the scratching that is done by the diamond tip. Then after breaking the wafer along the fracture lines in the preferred dimensions the PMMA has to be cleaned of and the surface of the substrates must be cleaned. This is done by first letting the substrates sit in acetone at 60 °C. This is done to dissolve the

PMMA that is still on top of the substrates. Then the substrates are rinsed with acetone and IPA. After this procedure the surface of the substrates is etched by Reactive Ion Etching (RIE).

To prepare the oven for growth the S_2 powder is inserted into the tube in a ceramic boat. A tube is connected to the quartz pipe so that the Ar gas flow can be inserted and controlled at will. Subsequently the WO_3 powder is prepared on a quartz holder and the Si/SiO_2 substrates are placed on top so that the SiO_2 side is facing the WO_3 powder. Then the holder is then inserted into the tube and placed in the middle of the furnace approximately (This is also the location of the temperature sensor of the furnace).

Insertion of the quartz holder with the WO_3 powder is done once the furnace has been heated to the desirable temperature. The procedure that follows is the purging of the system with Ar gas and bringing the pressure down to a near vacuum state. Then a desired Ar gas flow (in sccm) is introduced in the system which is kept at a desired pressure. At last the seperate heating element is used to heat the S_2 powder to a desired temperature. The temperature at which the S_2 is kept is lower because S_2 does not need a temperature as high as WO_3 needs to sublimate. Values of tunable parameters such as the Ar flow and the WO_3 temperature can be found in the results section as they were varied to see the effect on the growth.

The downside of this setup is that the sublimation of the WO_3 and the formation of the WS_2 on the Si/SiO_2 occur at the same location i.e. approximately the same temperature. Whereas in the three zone furnace mentioned below these locations can be varied.

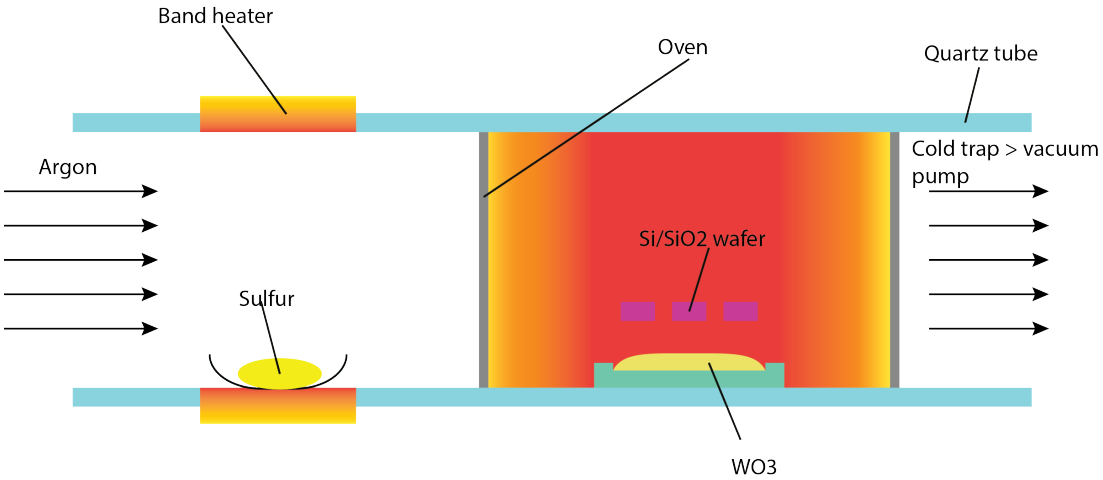

Figure 8: Schematic image of the one heating zone setup.

3.4 Three zone furnace

This setup consists of:

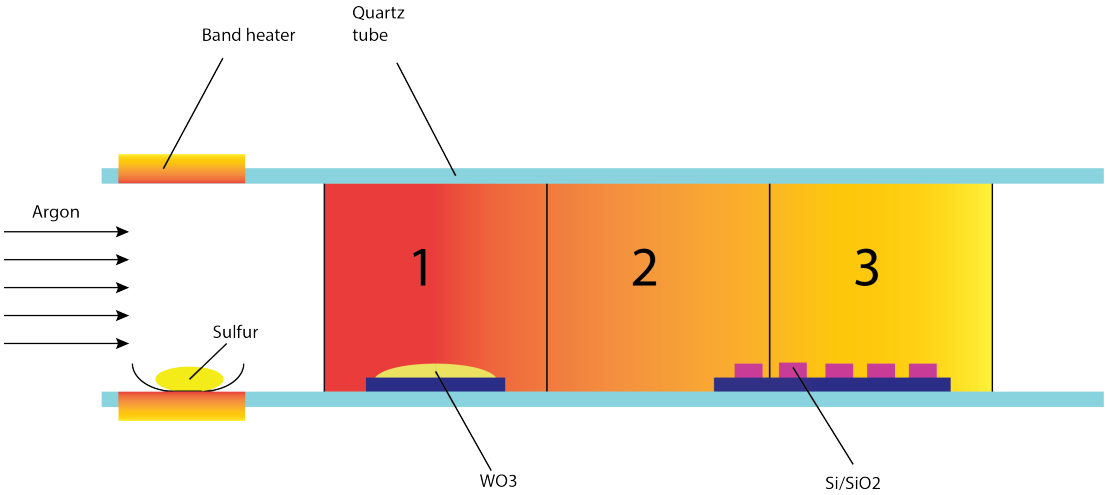

Figure 9: Schematic image of the three heating zone setup.

- Oven with three heating elements
- Quartz tube
- Band heater
- Argon gas source

The precursors used for this growth are WO_3 powder and S_2 flakes, just as in the one zone method. The method however differs significantly. First of all this growth is done at ambient pressure. Si/SiO_2 wafers are inserted into the quartz tube that penetrates the three heating zones. The wafers are distributed over the two latter heat zones. Because the two heating zones are kept at different temperatures a temperature gradient is present. This means that none of the wafers are growing in exactly the same conditions as its neighbours. This way the effect of temperature on the growth can be observed in a quicker manner than repeating the growth procedure at different temperatures.

After the wafers have been placed inside the quartz tube, the precursor WO_3 is placed into the first heating zone. This zone is kept at a desired temperature for the sublimation of the WO_3. Then the S_2 flakes are inserted in a boat upstream of both the precursor and the wafers. Also in this set up the seperate heating element is used to heat the S_2 to a desired temperature.

Once all necessary ingredients for the growth have been added to the quartz tube, the system is purged with Ar gas for 30 min. This is done to decrease the amount of air in the system to a minimum. Once the system is clear of unwanted reagents, the Ar flow is changed to a desirable flow and the heating program is started.

Although this method takes longer then the one described in the One zone furnace segment, this method seems to consistently produce flakes with a better PL than the one zone furnace.

3.5 Change of parameters and the effect on WS_2 growth

In both ovens there are several controllable parameters. Changing these parameters will have an effect on the growth of the WS_2. In this section the effect that changing these parameters has on the growth of WS_2 will be examined. The main question is how to recognise high quality growth with a relative low effort method. One of the possible indicators of a good stoichiometry, i.e. good quality, is high PL. Therefore the PL of the asgrown WS_2 is also investigated. Taking the PL image of a grown flake also indicates wether one really is looking at a monolayer flake. Because the monolayer flakes have a direct bandgap [1] the quantum yield of these flakes is much higher than the quantum yield of multilayer flakes.

3.5.1 One zone furnace

The controllable parameters in the one zone furnace setup are: the flowrate of Ar gas, the pressure in the quartz tube, the temperatures at which S_2 and WO_3 are sublimated, the dimensions of the quartz boat, the amount of WO_3 used and the time of growth. Growth comes in all kinds of sizes, on a wafer there will often be monolayer, bilayer and multilayer. Sometimes one will find neatly stacked layers that start to form bulk, at other times it seems the bulk starts to grow at random places on the monolayer. Another interesting phenomena is that monolayer tends to grow in different shapes. One can find the triangular shape, but also hexagonal shapes can be found. In short, on the three SiO_2/Si wafers that are growing in the oven at the same time one can expect to find many different shapes and forms of growth.

3.5.2 Three zone furnace

The controllable parameters in the three zone furnace setup are: the flowrate of Ar gas, the temperatures at which S_2 and WO_3 are sublimated and also the temperature at which sublimated S_2 and WO_3 after certain reactions will attach to the Si/SiO_2 surface, the amount of S_2 and WO_3 used and the time of growth. Growth resulting from this oven seems to have a higher coverage and a brighter PL in general.

4 Device Fabrication and Testing

4.1 Fabrication

Once samples are grown they need to be made into devices. This is a process of several steps. The samples are grown on top of wafers of a standard size, because these wafers are too large and contain to many grown samples it will be cut into 1x1cm or 1x0.5cm depending on the growth method that will be used. After this is done the area of interest in the growth must be isolated so that the attachment of gate & other electrodes is easier. This is done by removing

all unwanted growth near the area of interest with Reactive Ion Etching, which is the etching of the surface of the wafer by a plasma existing of reactive ions e.g. oxygen. However the whole sample will be exposed to the plasma. In order to make sure the area of interest is not etched away it is covered in PMMA. This is done in the following manner: first the whole sample is covered in PMMA, then a design is made in AUTOCAD®. This design can subsequently be loaded into the electron beam lithography (EBL) software. Then the sample is exposed to the electron beam and the pattern of interest is printed onto the sample. Then the pattern is developed by inserting the sample into a mixture of methylisobutylketon (MIBK) and iso-propanol alcohol (IPA) 1:3 ratio at room temperature. Now when exposing the sample to the plasma the area of interest will be preserved because it is protected by the PMMA. Then it is time to apply the gold leads on the sample. The PMMA that is left on the area of interest is removed in acetone, then a new layer of PMMA is applied to the whole sample so that the design for the gold leads can be printed on the PMMA with EBL. After developing the pattern the sample will be inserted into a evaporation machine to make a thin layer of gold on top of the pattern. This gold layer will cover the whole sample. Then the sample is placed in acetone again to remove the PMMA again, the gold layer that has been evaporated on top of the PMMA layer will be removed along with the PMMA. This way only the gold electrodes are left. To connect the sample to electronics used for testing it must be placed in a chip carrier. To connect the sample to the chip carrier a wire bonding machine is used. The wire bonding machine however has to exert a certain force on the sample to connect the aluminum wire. This can cause damage to the SiO_2 layer and as a consequence a high leakage current may exist. To avoid this problem the aluminum wire can also be attached to the sample by hand with assistance of silver paste. The problem without this method however is that you can not have a very high accuracy and a higher chance of shorting the gold leads is introduced. The SiO_2 layer before any treatment is resistant enough to withstand the force the wire bonding machine exerts on the sample, however after each treatment of the oxide layer one may introduce impurities and/or defects. These increase the chance of failure of the oxide layer. The gate electrode of the sample is the silicon, this gate is called a backgate because this silicon is on the bottom of the sample. Before putting the sample into the chip carrier and attaching it to the chip carrier via silver paste (at the bottom) and aluminum wires the native oxide layer which has formed on bottom of the silicon is scratched away with a diamond pen. Now it can function as a gate electrode. Another way of providing a gating medium is to use an ionic liquid. Using this method the external electric field applied onto the charge carriers at a certain gate voltage is stronger then for the SiO_2 backgate.

4.2 Device testing

To test the properties of the device it is inserted in a chamber in which temperature and pressure can be controlled. It is inserted into this chamber by the means of a chip carrier described above which also provides the electron-

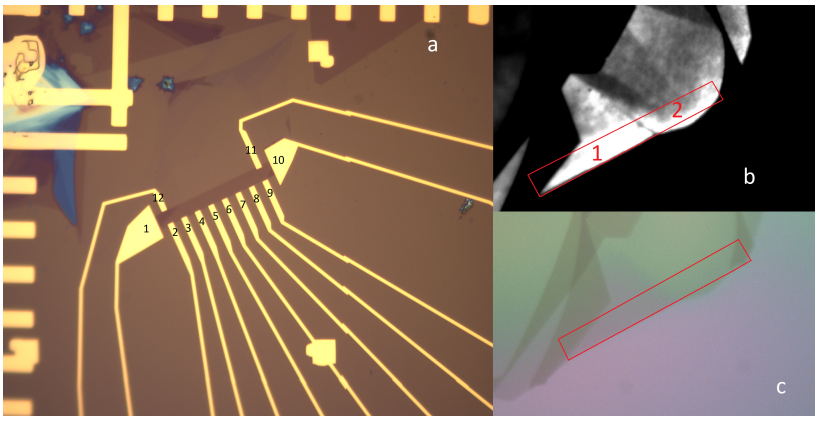

Figure 10: a) Optical microscope image of the device used for measurements, the gold leads are numbered. b) Intensity of PL shown over the area of the flake, the area made into a device has been indicated in red. The numbers in red indicate regions with bright (1) and darker (2) PL. c) Optical image of the flake which was selected for device fabrication. The region of interest is shown in the red square.

ical connection to the gold leads on the sample. Using a breakbox different electrodes can be used to make an electronic circuits. In this manner different gold leads can be used as source, drain or probe electrodes. Temperature, source-drain voltage (V_{ds}) and gating voltage (V_g) are all controlled by a computer. Pressure is brought back down to a vacuum using a vacuum pump. The downsides of this system is that it is quite prone to vibrations, mainly due to temperature oscillations and due to the vacuum pump. One way to reduce these oscillations is to detach the vacuum pump, but the chamber is not capable of keeping the vacuum for an extended period of time. Another method that is applied to reduce temperature related oscillations of the system is to manually control the valves of liquid nitrogen which is used to cool the system and the pump which is used to create a flow through the cooling chamber, this is not the chamber in which the sample is present but it is the chamber that contains the sample chamber. In this manner the cooling power supplied by the system can be brought to a minimum. A laser and a spectrometer are also present in the setup, these can be used to obtain the PL spectrum and the raman spectrum, both of which can be used to determine the composition of the material. The spectrometer is used to obtain the dependancy of the PL intensity on V_g.

In this report two different kind of PL intensity images will be provided. This is because two different kinds of charged coupling devices (CCD) are used to obtain PL intensity data. One is used for confirmation that a WS_2 is monolayer. This CCD is like a camera that shows the optical image but instead of color, the different intensities of different regions are displayed. The other CCD is used to obtain the PL intensity profile correlated to the wavelength of photons

emitted by the WS_2. This CCD is irradiated by focused light which is split in a grating and counts the number of photons of each wavelength to give an intensity profile.

5 Results & Discussion

In this section the results obtained from growth and transport tests will be presented and discussed. Growth and transport will be discussed in seperate sections. Photoluminescence results will be part of both subsections as this phenomena plays an important role in both subjects.

5.1 Growth

The 2D WS_2 semiconductors that are used for device fabrication are grown using CVD. The goal of experimenting with growth is to get a steady output of usuable samples for device fabrication. In this section the different steps and their results will be described.

The first test done in the one zone oven was to check what the effect of annealing in a sulfur rich temperature has on the sample. This was done in the following matter: all parameters were kept constant except the annealing time, which is the time the sample is left in the oven in a sulfur rich atmosphere after cooling down the oven. In all cases the quartz boat was treated with a thin layer of silver which acts as a catalyst in the CVD reaction. At first one hour of annealing was used, this lead to destruction of asgrown WS_2 so annealing time was reduced to zero. For this time growth is appearing. The structure varies from stretched hexagons to triangular flakes. Coverage is quite high and the flakes seem to grow at random positions on the surface instead of preferring impurities/defects only. The PL intensities are brightest near the corners of the triangles and the short sides of the stretched hexagonals. For an annealing times of 15 and 30 minutes the growth found on the wafer exists of almost exclusively triangular flakes. This supports the growth theory of Wang et al. who claim that in a sulfur rich environment the shape of grown flakes will be triangular. [18] The PL intensity maps of both are different however indicating that annealing time has an effect on the structure of growth regardless. For the 15 min. annealing time the PL intensity is quite homogeneous over the triangular flake although the intensity decreases towards the center of the flake and is almost not visible on the parts of the medians from the corner toward the center of the triangle. This observation supports the growth mechanism suggested by Cong et al. who state that growth starts from the center along the lines which are visible as dark lines in the PL intensity map, this means that these regions are exposed to the sulfur rich environment the longest. [6] The growth of the 30 min annealing shows bright PL spots near the corners and a completely dark center.

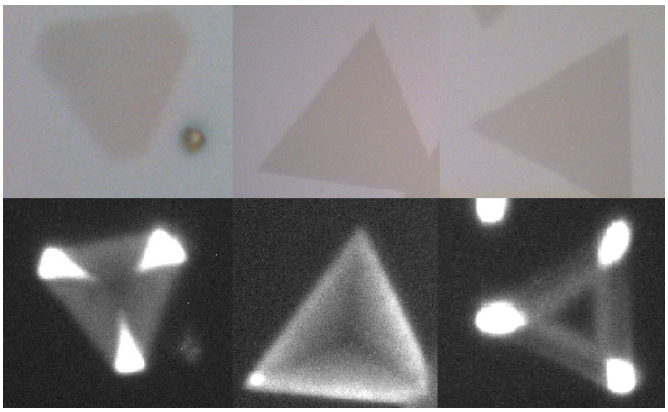

Figure 11: On the top row the optical images of 0 min, 15 min, 30 min annealing time are shown respectively. The PL intensity map of each flake is presented below its optical image. It can be seen that the PL intensity maps can be different while the optical image looks the same.

Another test was done to investigate the influence of silver on the growth of WS_2. Instead of depositing a thin layer of silver on the quartz boat it was deposited in a square pattern on top of the Si/SiO_2 surface itself. The first thing to note is that at the locations where silver was deposited there is growth of almost exclusively bulk matter indicating the preference of WS_2 to grow near the silver spots. Three substrates were used in this growth of whom only one was treated with silver. The substrate that was furthest away from the silver treated substrate had the least growth. These two observations point to the fact that silver truly aids in WS_2 growth. In the next growth neither quartz boat or SiO_2 substrate were treated with silver and growth time was reduced from 30 minutes to 20 minutes. This resulted in a much lower coverage of the substrates with flake growth, also an indication that silver is promoting growth on the substrates. After these experiments the setup was changed disturbing the environment. The result of this is that the same parameters used did not provide a steady output of monolayer growth anymore.

Another method of growing WS_2 is using three seperate heating zones instead of one. Results of this growth method will be presented and discussed below. The main difference between this setup and the one described above are the pressure in the growth region and the distance between the source material and the Si/SiO_2 substrates. Using this method an interesting phenomena occurs, namely the formation of a rough edge around growth as shown in figure 13. This growth occurs on the substrates that are furthest away from the precursor source. On the wafers closer to the WO_3 growth lacks this edge and has a strong PL intensity in certain monolayer areas. It seems that these substrates are growing in a more optimal condition than the ones that are further removed from the WO_3. Different growth on different substrates in the same experiment indicates that the distance between the source material and the substrates is

also an important parameter. One of the goals of growth with this method is to find flakes that have a high PL intensity. Monolayer that has a high intensity PL is almost exclusively found in structures that next to monolayer WS_2 also have multilayer growth. In these structures the PL of the monolayer seems to be highest when the monolayer is confined by multilayer WS_2. Another thing to note is that often in the high PL monolayer intensity maps a pattern is found in the intensity profile. This pattern seems to be periodic to some extent and exists of alternating bright PL and dark PL lines as shown in figure 12. It is possible that this is due to the growth mechanism of these specific structures, since monolayer flakes regardless of the structure show the maximum PL near edges of some sort it is possible that the dark lines are grain boundaries. This however has not been investigated in this report and is a hypothesis. Research on the structure of growth using transmission electron microscopy could be done to confirm or debunk this theory. The PL intensity of a flake does not change once it is treated with e.g. RIE, which can remove the multilayer WS_2 around the area of interest leaving only monolayer behind. This means that the PL intensity is an intrinsic property of the flake itself. It must therefore be related to the growth mechanism of these specific structures.

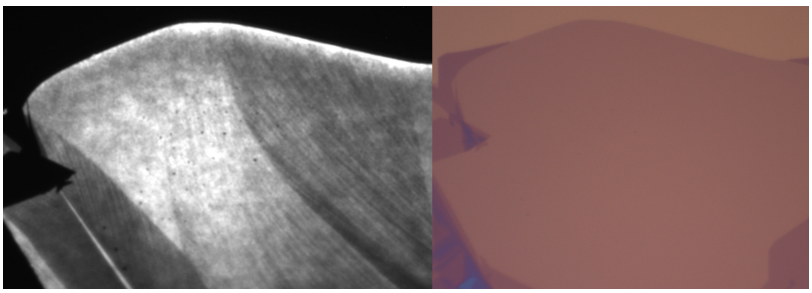

Figure 12: On the right the PL intensity map displaying the stripe phenomena is shown. On the right the optical image of the flake is shown.

Originally it was thought that the edge mentioned earlier in this text was caused by an overdose of WO_3. However reducing the amount of WO_3 failed to prevent the edge of forming again. As a matter of fact the growth on the substrates became less in coverage of the substrate and started to appear exclusively at impurities, defects or other areas with a increased surface free energy. These structures also seem to have a variety of monolayer and multilayer in the flake growth, which has proven to be an indication of a strong PL intensity. In an unrelated experiment the effect of sulfur annealing on asgrown samples was investigated by leaving a sample inside of a quartz tube oven at 850 °C. The before and after pictures of this sample indicate that instead of decreasing the edge growth it increased it. This means that when leaving the sample in a sulfur rich atmosphere for an increased period of time this edge becomes larger. However, the reason that the edge grew does not indicate that it is purely caused by sulfur exposure for a longer time. It means only that once this edge is there

treating it with sulfur annealing only increases it.

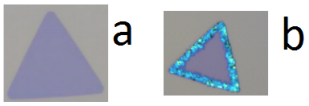

Figure 13: a: flake without edge. b: flake with edge

In comparison the three heating zone oven seems to produce samples with a higher PL intensity. In this setup more samples can be grown at once and temperature of the precursor and deposition temperature can be controlled seperately, this means WO_3 can be sublimated at a higher temperature increasing its vapor pressure, whereas in the one heating zone oven a low pressure is required to have both WO_3 sublimation and formation of monolayer WS_2 on the substrate. Because in the one heating zone oven the quartz boat with the WO_3 inside and the Si/SiO_2 substrates on top are quite close together the formation of WS_2 nucleation centers in the vapor phase must happen between the quartz boat and the substrates which is a distance of one to two mm. Hence pressure in this area must be very precise, two situations come to mind. If external pressure is to large WO_3 sublimation is surpressed and not many flakes will form. If the WO_3 vapor pressure is to high sulfur may have trouble to enter this region of 1-2 mm height also leading to a lacking formation of flakes. Since the pressure in the growth region is varying over time it is suspected that growth only takes place at a time where optimal pressure conditions reside. In the three zone oven this problem is resolved by simple putting more distance and a different temperature between the WO_3 and the substrates. This may be the reason why more growth is found on these substrates with respect to the one zone oven.

5.2 Electrical Transport

The device used for measurements in shown in figure 10. To check wether PL is a good indication for the quality of a sample the PL of the flake of interest is categorized. In figure 14 the variation of PL over two regions is shown. The two different lines in the graph belong to two different flakes. From now on the flake from whom the "channel" line is obtained will be referred to as channel flake whereas the flake from which the "triangular" line is obtained will be referred to as triangular flake. It can be seen that the channel flake has two distinguishable regions, a darker one and a lighter one, where the light one is approximately twice as bright as the darker one, the brighter region is indicated in figure 10 with number 1 and the darker region with number 2. The red line in the graph shows the PL intensity of a different flake, which is almost completely dark.

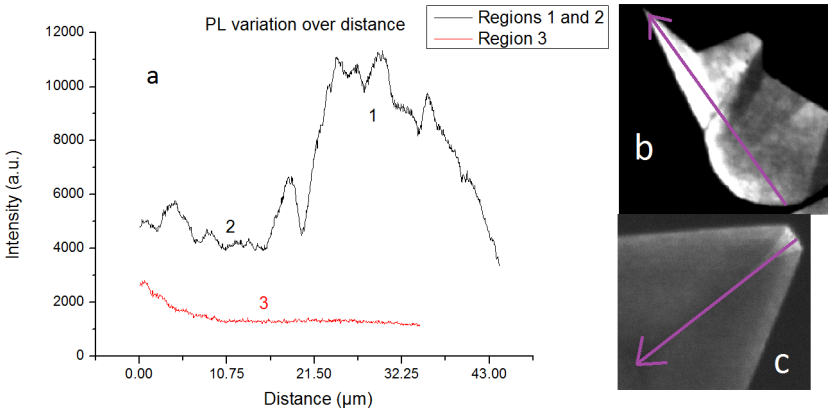

Figure 14: a) The black line indicates the variation of PL along the device, the red line indicates the PL from the triangular flake. b) the line along which PL variation for the channel flake has been obtained is indicated in purple. c) the line along which the PL variation for the triangular flake has been obtained in indicated in purple

Transfer curves of both the channel flake and the triangular flake are obtained using the SiO_2 back gate. No current is observed while scanning over a region of 20V to -100V. The breakdown current however does increase which leads to the conclusion that the current passes through a impurity path in the oxide layer instead of through the WS_2 channel. Obtaining the transfer curve was done while the sample is illuminated by a laser. This is done to investigate the dependancy of the intensity of the PL on the gating voltage.

In figure 15 the results of the backgate measurements are shown. It is clear that the PL intensity of the flakes change as the gate voltage is varied. Photon energy, gate voltage and PL intensity are plotted against each other to give the color map shown in figure 15a. Red displays high intensity where as blue displays low intensity. The intensity profile in this graph however is not what is expected from theory. An oscillation in PL intensity is visible. This disturbance is most likely due to the drift of the sample that is caused by temperature oscillations of the system. In figure 15b the PL intensity is plotted against the gate voltage for the photon energy value at which the maximum intensity occurs (2.005 eV). An increase in gate voltage from -100V to 100V doubles the PL intensity. However the intensity still remains at a fairly low value. In figure 15c,d the same graph is made but for different flakes. In 15c it is seen that the intensity has reached a maximum and decreases after -50V where as in 15d only a decrease in intensity is visible.

The backgate method is a reliable method to determine the kind of doping of the semiconductor. As for a perfect intrinsic semiconductor one would expect a symmetric profile with the maximum intensity at $E = E_g/2$ like the one

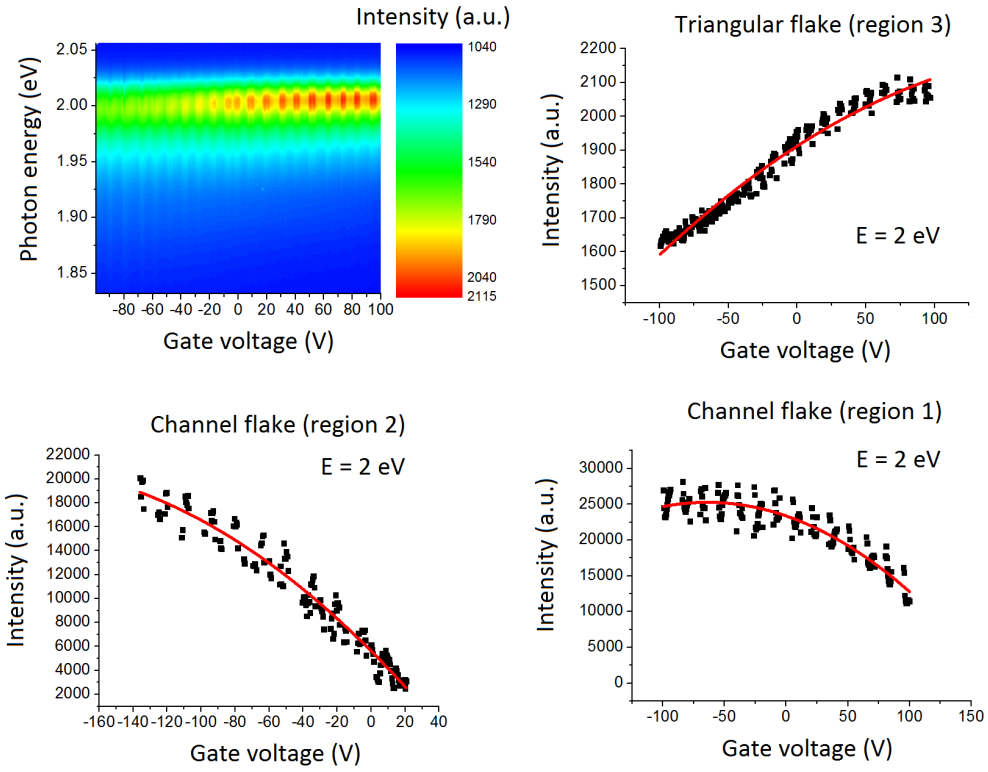

Figure 15: a: Color map with photon energy on the y-axis, gate voltage on the x-axis and the PL intensity as color profile. b,c,d: Variation of PL intensity with gate voltage for a photon energy of 2.005 eV, 1.990 eV and 1.995 eV respectively.

displayed in figure 4. Figure 15b,c,d each represent a part of this symmetric profile. Using this profile an estimation of doping of the material can be made. For the triangular flake an increase of PL intensity is observed as the gate voltage is increased indicating that this increase is part of the hole doped regime in the symmetric profile. For region 1 of the channel flake a maximum is visible in the scanning range which indicates that this part is close to intrinsic but a little electron doped. In region 2 of the channel flake the doping seems to be of electron kind as an decrease is observed when the gate voltage is increased, fitting well in the electron doped region of the symmetric profile.

Liquid ion gating can now be used to try and obtain the full symmetric profile described above because the electric field exposed on the charge carriers in the semiconductor for liquid ion gating is much larger than that of SiO_2 backgating for the same gate voltage. [19] This profile is visible in figure 16. The line shows a peak and two points of minimum intensity similar to that of the theoretical model shown in figure 4. It is not fully symmetric but this is most

likely due to temperature disturbances and the high mobility of the ions as they are in a liquid and therefore not fixed to a certain position. Another thing to note is that at the voltages at which a current starts to flow, be it either a hole current or an electron current the PL intensity has practically dropped to zero. Indicating that the Fermi level of the semiconductor can be tuned using gating methods as stated in the Theory section. The PL intensity maximum occurs when the drain-source current is almost zero indicating that the semiconductor is in the intrinsic regime at this gate voltage.

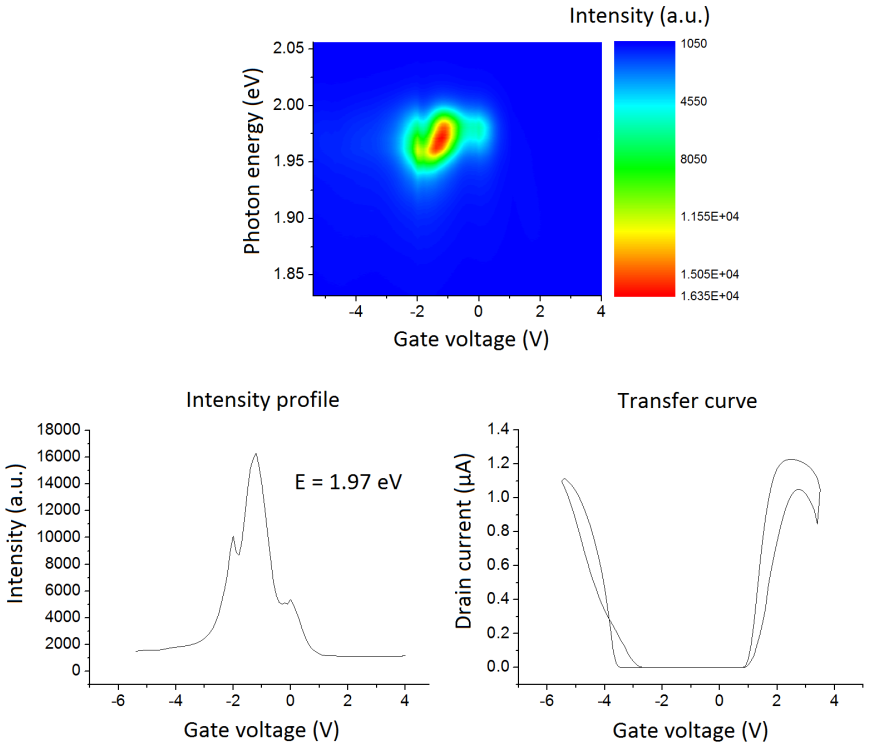

Figure 16: On top the original data, the energy was fixed at 1.97 eV which gave rise the the graph in the bottom left: the PL intensity plotted against the gate voltage for region 1 of the channel flake using liquid ion gating. On the bottom right the transfer curve of drain-source current in the channel flake is shown.

When examining the maximum PL intensity for the region 1 of the channel flake using backgating and liquid ion gating a difference is seen. Whereas the maximum PL for the backgating method is up to 27000 a.u. the maximum PL for liquid ion gating is 18000 a.u. At first glance this difference would be contributed to the liquid ion gating. However, other measurements of region 1 of

the channel flake display a much larger PL maximum intensity as shown in figure 17. In this figure two lines are visible black and red representing the backward and the forward scan respectively. The first thing to note is that the maximum PL intensity in this measurement goes up to 63000 a.u. which is triple that of the previous measurement. Another thing to note is the minimum around -2V in the backward scan. This is most likely due to drift of the sample due to the temperature oscillations. The maximima of both scans do not coincide. It appears that the maximum PL intensity of the backward scan is smaller in comparison to that of the forward scan. The threshold voltages for hole current are similar but the threshold voltages for the electron current also seem to differ. This may be due to the high mobility of the ions which can results in a faster formation of electric double layer for the backward sweep than that of the forward sweep. However more research should be done in the mechanisms behind different peak PL intensities.

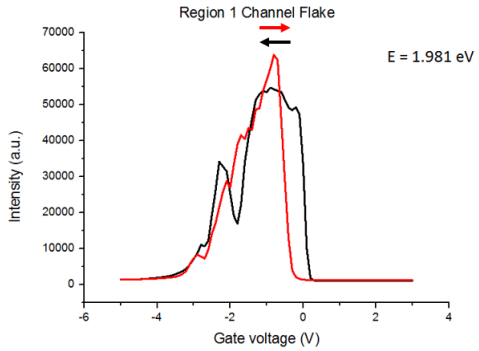

Figure 17: Intensity plotted against the gate voltage for a photon energy of 1.981 eV. The black line represents the intensity profile obtained when scanning from 3V to -5V and the red lines represents the profile obtained when scanning from -5V to 3V, indicated by the black and red arrows respectively.

6 Conclusion

In summary, 2D WS_2 monolayer flakes were grown using two methods: three heating zone furnace at ambient pressure and the one heating zone furnace at low pressure. The PL of these flakes was inventarized and used as a selection criteria. Asgrown WS_2 flakes which a non homogeneous PL intensity pattern were subsequently selected to be made into FET device. The dependence of the PL intensity on the gate voltage was investigated using first, a backgate (Si/SiO_2) and second, an ionic liquid gate.

From the two methods used to grow WS_2 the three zone method is recommended because it produces larger quantities of monolayer flakes which in general have a higher PL intensity than the ones from the one zone method.

By tuning the Fermi level of the WS_2 the PL intensity can be modified up to a scale of 10^4. Comparing transfer curves with PL intensity profiles shows that indeed the PL maximum occurs when the Fermi level of the WS_2 is in the intrinsic region. Furthermore it was shown that doping does affect the PL intensity of the sample when no gate voltage is applied. Showing that PL intensity can be used as a indicator of doping. However even in regions on the same flake a different PL intensity maximum occurs up to a factor of 3, indicating that perhaps there is more to it then just the doping of the flake. A possible mechanism decreasing PL intensity could be trap states, which can trap electrons or holes preventing them from recombining in optical radiative ways.

Further research should be done to investigate what other factors may affect the PL intensity. A proposal for such a research is to use WS_2 flakes which possess different photoluminescence maximum peaks and calculate the conductivities of each flake to see if higher photoluminescence peaks indicate better sample quality. Finally the results indicate that PL intensity is purely dependent on gating.

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