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Photoresponse of a Graphene-based Si/SiO_2 Field-Effect Transistor

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Abstract

In research on photosensitive materials on graphene, graphene is often on a Si/SiO_2 substrate and in many experiments the illumination of light is needed. In previous research it was found that the graphene Si/SiO_2 field-effect transistor has a response to light even when no photosensitive material is placed on top. Therefore, in this research the light response of a graphene Si/SiO_2 field-effect transistor at the visible and infrared regime is investigated. This is done by measuring the resistance of the graphene channel and the leakage current through the gate dielectric while illuminating the sample with either broad-band white light or monochromatic laser. It is found that the graphene field-effect transistor does not have a significant response to visible or infrared light. This is inconsistent with previous research in which a change in the graphene channel resistance was observed upon illumination with white light. Furthermore, the charging effect of impurities at the Si/SiO_2 interface is investigated and two charging mechanisms with time constants 41 s and 452 s were distinguished. This research is a step in understanding the light response of a graphene field-effect transistor.

Contents

Chapter 1

Introduction: graphene and photosystem I

In nature, photosystem I (PSI) is one of the two protein complexes responsible for the primary photochemistry of photosynthesis. It resides on the thylakoid's membrane in the chloroplast organelles of phototropic organisms with the exception of cyanobacteria for which the thylakoid is found in the cytosol. PSI can absorb light with a wavelength of approximately 700 nm and transfers the excitation energy within the protein complex [1]. Since the PSI has an internal quantum efficiency close to unity it is relevant to study its potential for implementation in optoelectronic devices such as in graphene-based electronics. Also, it has been suggested that the charge transfer in PSI is spin selective [2]. In our research group, we have been measuring the spin properties of PSI using a graphene field-effect transistor (FET).

Graphene devices have been at the center of many researches since they were first fabricated by A. Geim, K. Novoselov et al. in 2004 [3]. Graphene is a two-dimensional crystalline allotrope of carbon. A monolayer of carbon atoms arranged in a close-packed, two atom basis, hexagonal lattice, or so-called honeycomb lattice. Carbon has four valance electrons, two s and two p electrons. The honeycomb lattice is attained by strong σ bonds which are formed by sp^2 hybridization between neighboring carbon atoms. The π bonds and π^* anti-bonds formed by the remaining out of plane p orbitals give rise to the valence and conduction bands. The valance and conduction bands are quite remarkable in comparison to the bands of conventional insulators/semiconductors. At low energies they are opposite conical and touch apexes in the 6 corners of the hexagonal Brillouin zone, which are called the Dirac points (K and K' points). This is special in two ways. First, graphene has a zero band gap; second, the dispersion relation is linear for low energies. The density of states is linear and therefore the charge carrier density changes linearly with the Fermi level. For a positive Fermi level electron states are created while for a negative Fermi energy level hole states are created. For a visualization see Figure A.1. [4]

In most cases, graphene is on a Si/SiO_2 substrate and in many experiments on photosensitive materials, such as with PSI, the illumination of light is needed. If the graphene FET has an intrinsic response to light, measurements will show a composite of the response of the photosensitive material with the response of the graphene FET. If the intrinsic response of the graphene FET is well understood it can be taken into account in future research. In this bachelor research, the photoresponse of graphene on a Si/SiO_2 substrate is investigated.

Chapter 2

Charge transport in graphene

2.1 Electrical characterization of graphene

The Dirac curve

A method to characterize the electrical properties of a material is by modulating the electrical conductivity or resistivity by the application of an electric field. This is exactly what is done in a field-effect transistor and therefore it is widely used in research on new materials. The particular FET used for this research consists of a p doped Si layer, 300 nm SiO_2 dielectric layer and a graphene monolayer flake with Ti/Au contacts (see Figure 2.1a). A current can be send trough the graphene flake via the contacts (source and drain) and a voltage can be applied at the Si layer which functions as the back gate. When a gate voltage is applied at the back gate, a potential difference is created over the dielectric inducing a change in the charge density in the graphene channel. This is comparable to the mechanism of a parallel plate capacitor, therefore the charge carrier density in graphene is given by:

$$n = \frac{Q}{eA} = \frac{\epsilon_0 \epsilon_r A |V_g|/t}{eA} = \frac{\epsilon_0 \epsilon_r}{et} |V_g| \tag{2.1}$$

where Q is the charge, A is the surface area, t is the dielectric thickness, e is the electron charge, ϵ_0 and ϵ_r are the vacuum permittivity and the permittivity of the dielectric respectively and V_g is the gate voltage. In this research the dielectric thickness will be $t = 300$ nm and the permittivity of SiO_2 is $\epsilon_r = 3.9$ [5]. The equation shows that the surface charge density is proportional to the gate voltage. Changing the gate voltage on the FET basically tunes the Fermi energy level of the graphene channel and therefore the charge carrier density. For a positive charge carrier density the charge transport is dominated by electrons whereas for a negative charge carrier density by holes. The charge carrier density can be used to express the resistivity of the graphene channel in terms of V_g.

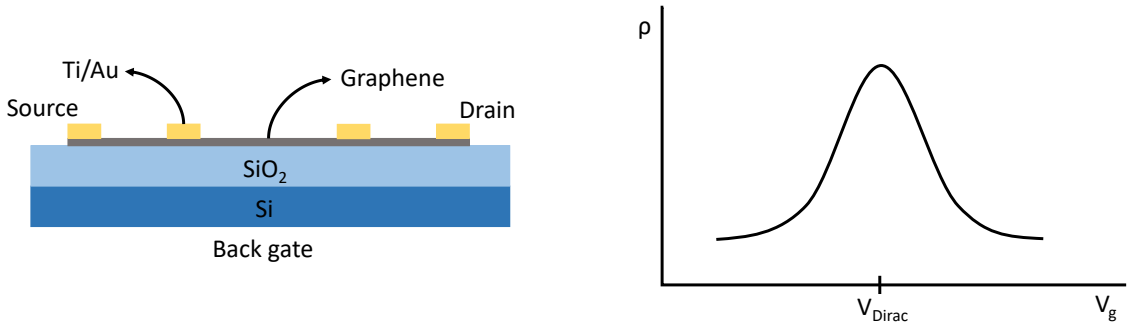
$$\rho = \frac{E}{J} = \frac{\nu_d/\mu_i}{e\nu_d n} = \frac{1}{e\mu_i n} \propto \frac{1}{|V_g|} \tag{2.2}$$

where ν_d is the drift velocity and μ_i is the hole or electron mobility in graphene. This shows an inverse proportional relation between the resistivity of the graphene channel and the gate voltage.

When plotting the resistivity as a function of the gate voltage this inverse proportionality is asymptotic to the y axis. In practice this relation will look like the curve drawn in 2.1b. It has a finite maximum resistivity and this does not necessarily have to be at zero gate voltage. The curve of the resistivity as a function of the gate voltage is called the Dirac curve and its maximum is called the charge neutrality point (CNP). The CNP is the point where the graphene is neutral, has the lowest density of states and therefore has the highest resistivity.

Ideally the CNP of graphene is at zero gate voltage. When the graphene channel is doped it has charge carriers even at zero gate voltage. The Fermi level of the system is shifted as well as the charge neutrality point. If the graphene is p-doped, the Fermi level has lowered and a positive gate voltage has to be applied to reach the CNP. This is reversed for a n-doped graphene channel. To take the doping of the graphene channel into account, the gate voltage dependence of Equation 2.1 should be altered with $n(V_g) \rightarrow n(V_g - V_{Dirac})$ where V_{Dirac} is the gate voltage for which the CNP is reached.

Eventhough, graphene has a zero density of states at V_{Dirac} it shows a finite maximum resistivity and therefore it is still conducting. This is mostly the result of thermal energy in graphene. Furthermore, there are structural corrugations [6] and the formation of electron and hole puddles in graphene [7]. Structural corrugations can be explained as a rippling of the graphene sheet leading to a broadening of the Dirac point. Graphene is not a perfect 2D material as is insinuated. It has small differences in orientation which lead to Dirac points with slightly different energies. In one part of the sheet the density of states could be zero while in other parts it is not zero. Furthermore, there is the formation of electron and hole puddles. Due to charged impurities in the SiO_2 below the graphene the potential landscape over graphene is not uniform. These variations in the potential of the SiO_2 surface induce local differences in the charge carrier densities.



(a) (b)

Figure 2.1: Schematic drawing of (a) the graphene FET. It consists of a p-doped Si layer which acts as a back gate, a 300 nm SiO_2 dielectric layer, a graphene monolayer and a Ti/Au contact structure. (b) a Dirac curve of a graphene FET. The resistivity is plotted versus the gate voltage.

2.2 The Si/SiO_2 system

The graphene FET is a well understood structure but how will the device respond to light? Our first intuition was to look for the answer in the Si/SiO_2 substrate. As mentioned in the introduction,

graphene has a zero band gap and therefore we did not expect it to respond to light. The Si layer on the other hand does respond to light [8]. Si has a band gap of 1.1 eV [5], and photons of an equal or higher energy can excite electrons from its valance band to the conduction band. This process alone would not change the electronic state of the graphene channel on the other side of the SiO_2 layer. Our hypothesis is that excited charge carriers from Si will occupy localized states in the Si/SiO_2 interface, charging the interface and changing the potential landscape over the graphene channel. This change in potential induces a horizontal shift of the Dirac peak in which the direction depends on the type of charging at the interface. In order to support this hypothesis we study the impurities and corresponding charge traps for the Si/SiO_2 system.

Types of charge defects and traps

As described by Deal [9, 10] the charged impurities and charge traps can be categorized in four categories (See Figure 2.2).

First of all we have **interface traps** which are electron and hole traps located at the Si/SiO_2 interface. These interface traps have energy levels inside the band gap of Si and can be occupied by charge carriers from Si. The interface traps are therefore filled to the Fermi energy level by electrons from the Si conduction band. Changing the Fermi energy level changes the occupancy of these traps therefore the interface traps function as an extra capacitance between Si and SiO_2.

Next we have **fixed oxide charges**. These fixed oxide charges are positive charges located in the transition region between Si and SiO_2. The positive charges are related to the structure of this interface transition region. Fixed oxide charges are stable and unaffected by gate voltages.

Thirdly, there are **bulk oxide traps**. Bulk oxide traps include any trap related to defects in the oxide layer which are electron traps as well as hole traps. The hole traps are much more abundant compared to the electron traps. The hole trap density is higher and they have very large cross-sections which leads to a hole trapping probability close to unity. These dominant hole traps are located close to the Si/SiO_2 interface. Furthermore they are neutral before charge capture and can also be discharged by electron capture.

Finally, there are the **mobile oxide charges**. These charges arise from contamination of the oxide layer by alkali ions. Ions such as Na^+ and K^+ may enter the oxide during the preparation process of the substrate for example from gas present during temperature treatments.

It seems that the bulk oxide hole charge traps could play a role in the response on light. Fixed oxide charges and mobile oxide charges are not affected by light. Interface traps have a strong interaction with Si and are likely to lose charge to Si. Bulk oxide traps on the other hand show the sought-after properties. When holes are injected in the SiO_2 layer there will be a build of positive charge in the SiO_2 layer affecting the graphene channel. This positive charge will increase the Fermi energy level in the graphene channel and shifts the Dirac curve to the left.

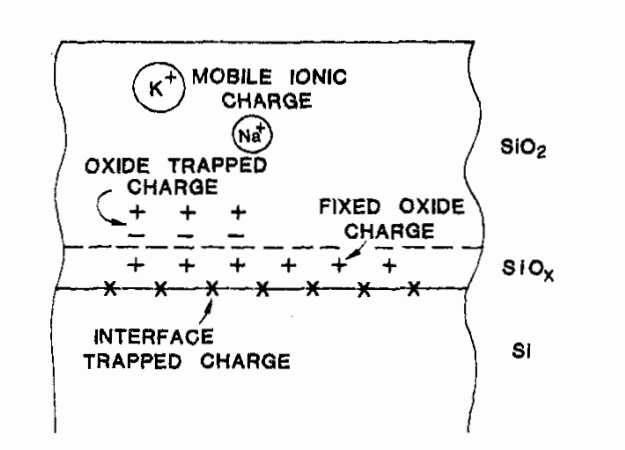


Figure 2.2: Schematic drawing of the charges or charge traps in the Si/SiO_2 system. Figure adapted from [9].

Photo-induced charge trapping

In this subsection it is investigated how charge enters the SiO_2 layer and occupies the bulk oxide traps. One way charge carriers could enter the oxide layer would be by internal photoemission for example photoexcited electrons which transfer from the Si valence band to the SiO_2 conduction band. In order for this to happen, electrons have to overcome the energy offset between the Si valance band and the SiO_2 conduction band and holes the energy offset between the Si conduction band and the SiO_2 valance band which are 4.25 eV and 4.92 eV, respectively [11, 12]. This would mean the charge carriers would have to be excited by UV light.

A second way charge carriers could enter the oxide layer would be by tunneling. Photoexcited charge carriers at the Si/SiO_2 interface could have gained enough energy to tunnel to the bulk oxide trap states in the SiO_2 band gap. This enables the bulk oxide traps to be occupied while illuminating the device with lower energy light. Applying a positive gate voltage will create hole accumulation at the Si/SiO_2 interface and may also aid the charge trapping in SiO_2.

Chapter 3

Experiments

3.1 Device fabrication

A large part of my bachelor research consisted of device fabrication. In total, four devices were fabricated. One device was used in a master research on PSI, another device was broken and two devices were actually measured. For this research the devices were fabricated by mechanical exfoiliation of graphene onto the substrate and creating contact structures by electron beam lithography (EBL) and evaporation deposition. The fabrication process will be discussed in detail in this section. Schematic drawings of the processes in device fabrication can be found in Figure 3.1.

Mechanical exfoiliation of graphene

The fabrication of the devices started with a commercially available Si/SiO_2 substrate with an oxide thickness of 300 nm on top of a heavily p doped Si layer. Graphene monolayers can be transfered from graphite onto the substrate by mechanical exfoiliation. Using Scotch tape, flakes of graphite were exfoiliated and transfered onto the substrate. This technique covers the substrate with a lot of large multilayer graphene flakes and only few monolayer flakes of the desired dimensions. Monolayer graphene can be distinguished with an optical microscope. A monolayer graphene flake on a Si/SiO_2 substrate gives an optical contrast of around 2.3% [13]. Eventhough, there are more reliable methods for confirming a monolayer for example measuring thickness with atomic force microscopy (AFM), for this research the monolayer graphene flakes where confirmed only by measuring the optical contrast.

Spin coating

The first step in creating a contact structure on the sample is applying an electron beam resist on the sample's surface by means of spin coating. The used resist is a 4% Poly(methyl methacrylate) (PMMA) solution. PMMA is a positive resist, such that exposure to an electron beam will result in local fracture of polymers, making it soluble to the resist developer solution. After the sample was baked for 90 s at 180 °C, the sample was placed in the spin coater. The spin coater was set to rotate at 500 rpm for 5 s (during which the PMMA solution was applied by pipetting on the rotating sample) and at 4000 rpm for 60 s. Thereafter, the sample was baked again 90 s at 180 °C. This process results un a uniform film of 0.27 μm thick. At this point a scratch was made in one of

the corners of the substrate. This scratch is helpful for alignment and navigation over the sample surface during EBL.

Electron beam lithography

Before starting with EBL, the contact structure first needed to be designed in a drafting software application. For the fabrication of these devices AutoCAD was used. Using the digital microscope, photographs covering the entire sample surface were captured. These photos were then aligned and scaled in AutoCAD to map the sample surface. After this step the contact structure was designed using the photographed sample surface as a reference.

With electron beam lithography the sample was exposed to a focused beam of electrons. As explained in the previous subsection, the electron beam locally changes the solubility of the resist. Although EBL allows writing contact structures with a very high resolution one of the difficulties is accurately aligning the contact structure design with the sample loaded in the EBL equipment.

After the contact structure was drawn with EBL, the sample was developed with the resist developer solution. The developer solution for 4% PMMA is a mixture of Methyl isobutyl ketone (MIBK) and Isopropyl alcohol (IPA) in a 1:3 ratio. The sample was submerged in this mixture for 60 s, subsequently 30 s in pure IPA and afterwards dried with a N_2 gun.

Evaporation deposition

The following step in the device fabrication is evaporation deposition. In evaporation deposition a metal is evaporated by bombarding it with electrons. The evaporated metal particles deposit on the sample which is placed above the evaporating metal. For the fabricated devices, first a 5 nm thick titanium (Ti) was deposited followed by a 50 nm tick gold (Au) layer. The Ti layer functions as an adhesive layer between the sample and the Au layer.

The evaporation deposition covers the entire sample surface. The Ti/Au layers are deposited on top of the unexposed PMMA resist except for the contact structure where the Ti/Au layers are directly on the sample. Submerging the sample in 50 °C acetone for 5 minutes or longer solved the remaining unexposed PMMA eliminating also the metals on top of the PMMA. At this stage, the sample only had the Ti/Au contact structure left on top. Optical microscope photographs of both samples after deposition can be found in Figure A.2 and A.3.

Tube furnace

As an optional step, the sample can be annealed in the tube furnace. In the tube furnace the sample is placed in a glass tube and heated to 350 °C while a N_2/Ar gas flows through the tube. The heating desorbs adsorbates on the sample and they are discharged by the inert gas flowing over the sample. The annealing of the sample can reduce the doping of graphene by absorbates.

Wire bonding

To be able to load the sample in a measurement setup the sample had to be placed in a 44 pin chip carrier. The sample was glued with its back to the chip carrier using silver conductive adhesive. The contacts were connected to the chip carrier using wire bonding. With wire bonding a piece of metal was welded to the contact using pressure and ultrasonic energy. With an arc the metal wire

was guided to one of the chip carrier pins and welded. The wire consisted of a 99% aluminum 1% silicon alloy.

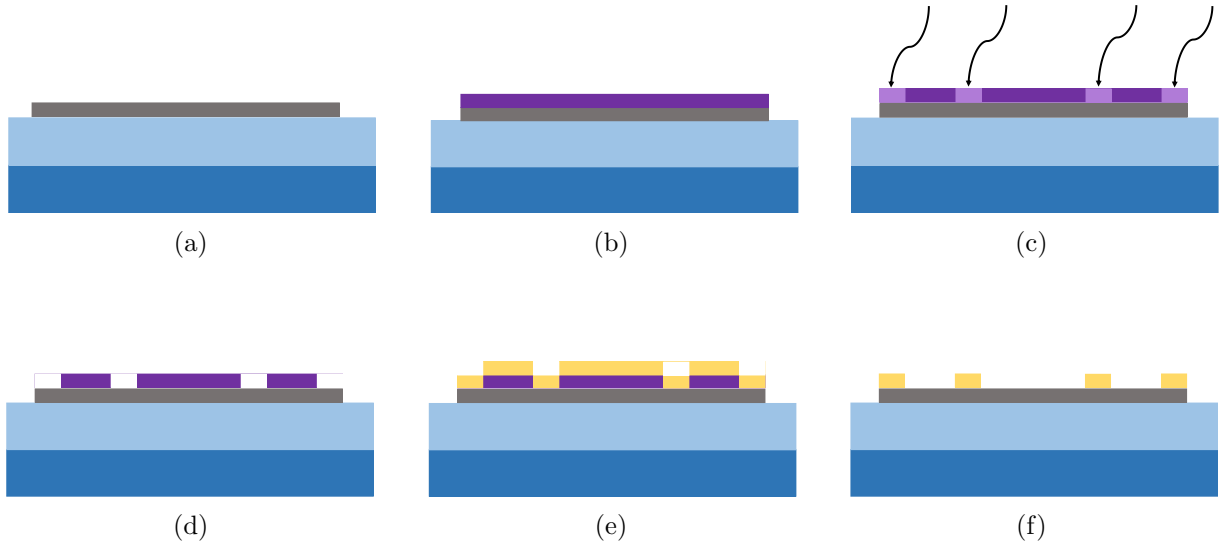


Figure 3.1: Schematic drawing of the steps in device fabrication. (a) Mechanical exfoiliated graphene on Si/SiO_2 wafer. (b) Spin coating of PMMA EBL resist. (c) Drawing the contact structure using EBL. (d) Developing the exposed resist using the developer solution. (e) Deposition of the Ti/Au layers. (f) Removing unexposed resist with Ti/Au on top.

3.2 Measurement setup

For the two devices that were measured, two different setups where used. One setup with a heating element and a high intensity white light source and another with a continuous wave Ti:Sapphire laser. In this section both measurement setups and the type of measurements conducted are explained.

Lamp and laser setup specifications

The first setup (from now on referred to as the lamp setup) consisted of a 44 pin chip holder inside a vacuum chamber. The vacuum chamber was connected to a vacuum pump, providing a vacuum of around 10^{-7} mbar. The chip holder was connected to a switch box to allow connecting to or switching connections on the nanodevice. Furthermore, a heating element with a sensor was present which could heat the device to 400 K. Finally, a high intensity white light source was added to the setup to illuminate the device. The light of the lamp was directed trough a tube directly on the device in order to minimize the influence of ambient light. Measurement equipment for this setup consisted of lock-in amplifiers (Stanford Research Systems) and voltage source equipped with an ampere meter (Keithley). The equipment was connected to a computer with the data acquisition software LabVIEW which stored the data and allowed control over the equipment.

The second setup (from now on referred to as the laser setup) made use of a continuous wave

Ti:Sapphire laser to illuminate the device. The wavelength of the laser could vary between 700 nm and 1000 nm and an intensity of around 5 mW could be achieved. The nanodevice was placed in a 24 pin chip holder in a vacuum chamber placed on an optical table. Also for this setup the chip holder was connected to a switch box. The measurement equipment for this setup consisted only of Keithley source/measurement units. The laser, sourcing and measurement could be remotely controlled using a MATLAB-based interface.

Measuring the resistance of a graphene channel

The resistance of a graphene channel was measured using a four terminal measurement (or four-point probes method). A schematic drawing of the circuit for this type of measurement can be found in Figure 3.2. With the four terminal measurement the voltage drop over a channel was measured at two contacts while a 10 nA current was sourced and drained at two different contacts enclosing the contacts over which the voltage drop was measured. As there is no current going through the contact by which the voltage drop is measured, the measured voltage drop is solely the voltage drop over the graphene channel. The resistance is then given by $R_{channel} = V/I$. Where V is the measured voltage drop and I is the sourcing current. To calculate the sheet resistance, the channel resistance needs to be adjusted to $R_{sheet} = R_{channel} \cdot W/L$ where W is the width of the channel and L is the length.

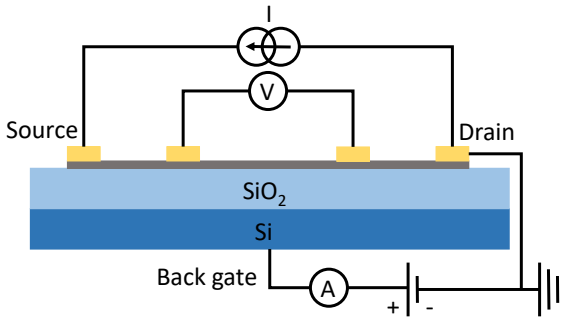


Figure 3.2: Schematic drawing of a four terminal measurement on a graphene channel.

For the lamp setup the noise in the signal of the resistance measurements was reduced using a lock-in amplifier (Stanford Research Systems). The lock-in amplifier modulates the sourcing current with a reference frequency of 13.364 Hz. At the same time the voltage meter measured the voltage drop over a channel and sent the signal to the lock-in amplifier. The lock-in amplifier takes the product of the measured signal with a reference signal of the set frequency and integrate this over a period of 300 ms (called time constant). The integration filters any signal with a different frequency than the reference signal which reduces the noise in the signal. For the laser setup the lock-in amplifiers where not available so a DC source current was sourced and the resistance measurements were done using the Keithley source/measurement units.

A voltage source was connected to the Si back gate to apply a gate voltage. Using the same source measure unit the leakage current was measured. The SiO_2 layer is not a perfect insulator and there will always be some current leaking through. Also the effect of illumination of the device could be seen in the leakage current.

3.3 Different measurement types

In order to investigate the effect of light on the nanodevice three measurements have been preformed. These measurements are described in the following subsections.

I. Time dependent response to light

In this measurement the gate voltage is parked at a non zero voltage chosen after the device characterization. The resistance and leakage current of the device is monitored over time. The light source is turned on during the course of the measurement. This measurement is simply aimed at observing the behavior of the device upon illumination.

II. Response on a step in gate voltage

The second measurement is obtained by monitoring the resistance and leakage current of the device after a sudden change in the gate voltage. The gate voltage is kept at zero voltage in the beginning of the measurement. After half an hour, the gate voltage is suddenly changed to a certain voltage. The resistance and leakage current show an exponentially decaying response to this sudden change in gate voltage. This exponential behavior comes from the charging or discharging processes in the Si/SiO_2 interface. From the exponential behavior in this response, time constants can be extracted. Investigating the time constants could enable us to distinct different processes responsible for influencing the resistance of the graphene channel. If these processes are influenced by the presence of light, we expect these time constants to vary with illumination of the device.

III. Wavelength dependence

In the third and last measurement the light wavelength dependence of the resistance and leakage current are measured. We expect the response of the device on light to be dependent on the wavelength of the light (section 2.2). This measurement can only be preformed in the laser setup, where a tunable wavelength laser is available.

Chapter 4

Results

4.1 Device characterization

Device I

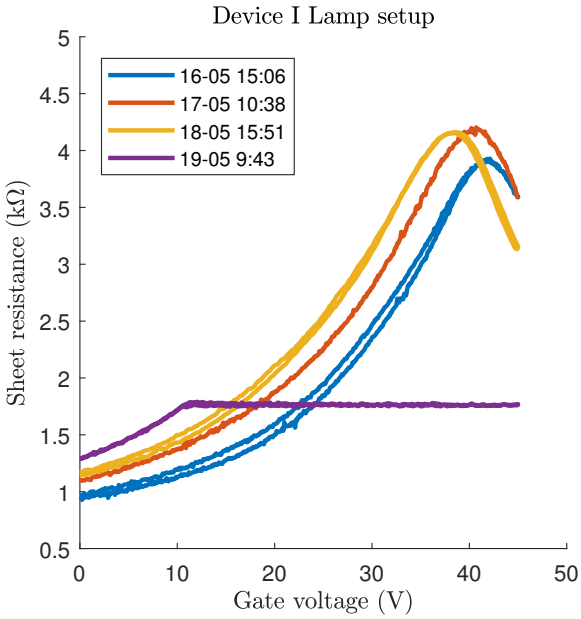
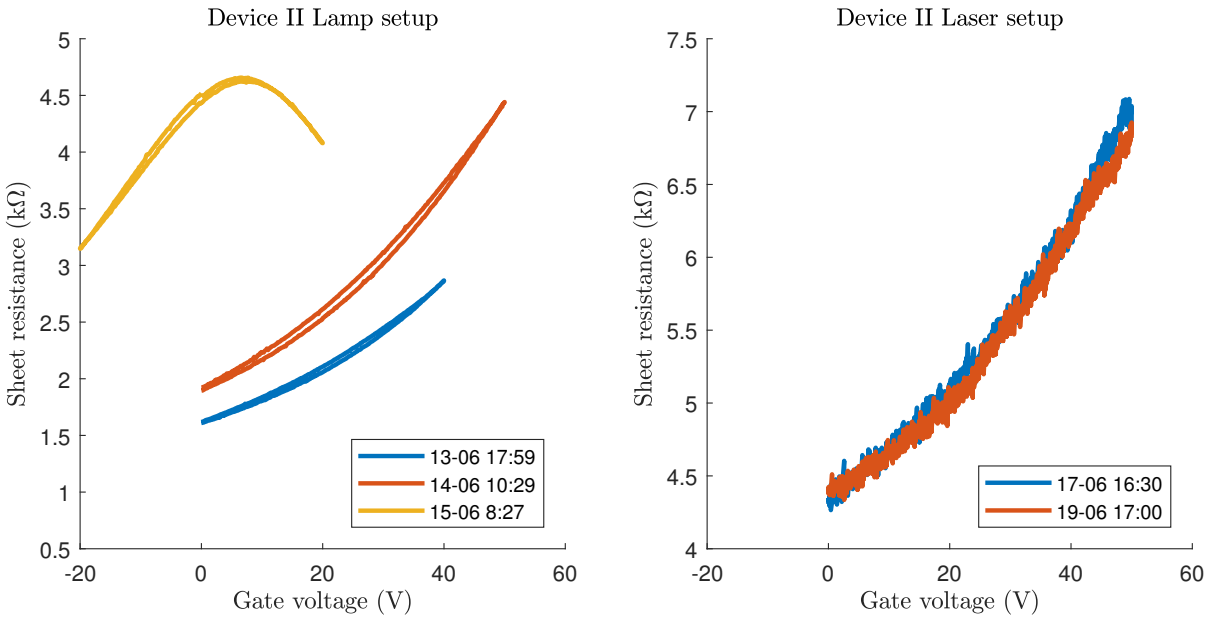


Figure 4.1: Dirac curves of device I during the measurement. The CNP shifts from 42 V to 38 V in two days. The fourth day of measuring the oxide layer broke down.

The Dirac curves of device I are plotted in Figure 4.1. For each day during the measurement a Dirac curve is shown. Due to the risk of a breakdown of the oxide layer the gate voltage was only varied up to 45 V. It can be seen that over the first three days the CNP shifts from 42 V to 38 V. This is probably due to the desorption of p dopant on the graphene channel. At the fourth day of the measurement it was found that the sheet resistance saturates after a gate voltage of 11 V. The leakage current at this gate voltage showed almost 10 nA, our sourced current, which indicated that

the SiO_2 insulator had broken down. Due to the this breakdown no light measurements were done on device I. The measurements that are done on this device before it broke were measurements of the response on a step in gate voltage.

Device II



(a) (b)

Figure 4.2: Dirac curves of device II in (a) the lamp setup. During the first two days a change in resistance is observed. The third day the device was annealed and the CNP shifted to 7 V. (b) the laser setup. The noise level is higher due to a DC measurement and the Dirac curve shows an offset compared to (a).

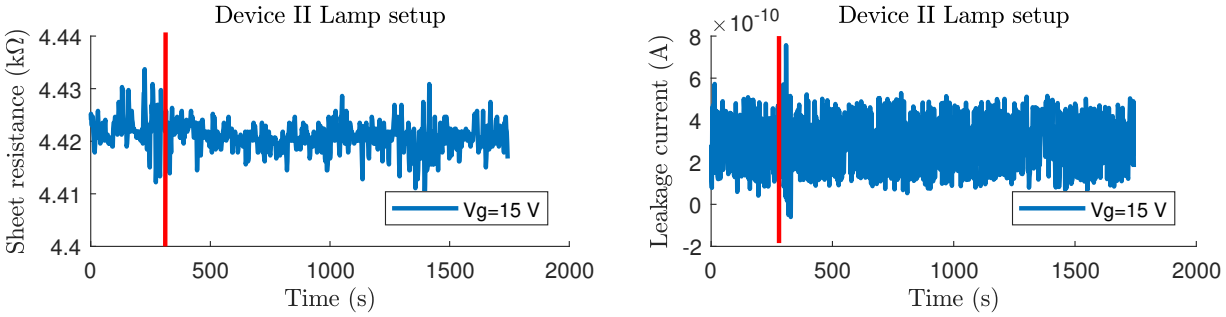
The Dirac curves of device II are plotted in Figure 4.2a for the lamp setup and Figure 4.2b for the laser setup. Again for each day during the measurement one Dirac curve is shown. During the first two days only the left shoulder of the Dirac curve was measured. The CNP seemed to be beyond 50 V and because of this reason we did not measure it. There is a change in the resistance between the first and second day. It looks like the Dirac curve has shifted rather than an increase in resistance. This is more likely because the curvature has changed. The cause of this shift is probably the same as for Device I, that is, the device being put in vacuum therefore the p dopant desorb from the graphene surface. The third day device II was annealed at 400 K for three hours in the lamp setup. By annealing the device, p doping absorbates are desorbed from the surface causing the CNP to shift towards zero. Now the CNP could be measured and was found at 7 V. It has to be mentioned that the effect of annealing on the resistance was not saturated after three hours of annealing, suggesting that the Dirac curve could have shifted further if it was annealed for a longer period. During the third day of measuring the device was transfered to the laser setup.

Unfortunately, in the laser setup the resistance of the graphene channel could only be measured

in DC, without a lock-in amplifier. When loading device II in the laser setup it was exposed to air and this might have countered the effect of annealing. Therefore the CNP is again at a high gate voltage which was not measured. The shift in the Dirac curve observed in the lamp setup was not found in the laser setup. This could be the consequence of a different pressure in the setup. A notable difference between the Dirac curves measured in the lamp setup and laser setup is what seems to be an offset in the resistance of 2.5 kΩ. As this offset is quite large, it is thought not to come from the graphene channel but from a side effect of measuring a DC signal. At this point it remains not fully understood.

4.2 Time dependent response to light

As explained in section 3.3, for this type of measurement the gate voltage is parked at a non zero voltage and during the measurement the light source is turned on. The response to light in device II after it was annealed in the lamp setup is plotted in Figure 4.3.



(a) (b)

Figure 4.3: Response in (a) the sheet resistance and (b) the leakage current of the annealed device II on light in the lamp setup. The gate voltage is parked at 15 V and the light is turned on at 300 s which is represented in both figures with a red line.

As can be seen in Figure 4.3a the resistance of the graphene channel does not show a notable response after turning on the light. The fluctuations that are observed are comparable to the fluctuations seen in measurements without light. The leakage current in Figure 4.3b does show a response to turning on the light. In the signal, directly after turning on the light, a broadening of the noise can be observed however the average leakage current does not change. This broadening of the noise can be attributed to charging or discharging of the Si/SiO_2 interface.

4.3 Response to a step in gate voltage

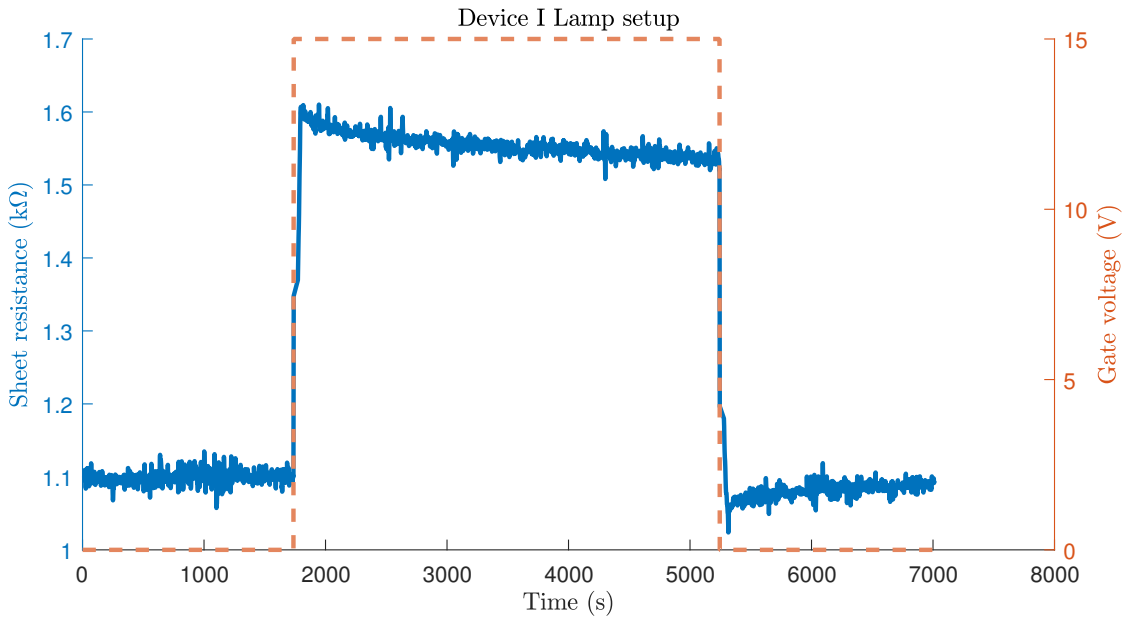


Figure 4.4: Response of the graphene channel resistance (left axis) on a 15 V step in the gate voltage (right axis). The resistance is initially stable but shows an exponential decay after a step in gate voltage.

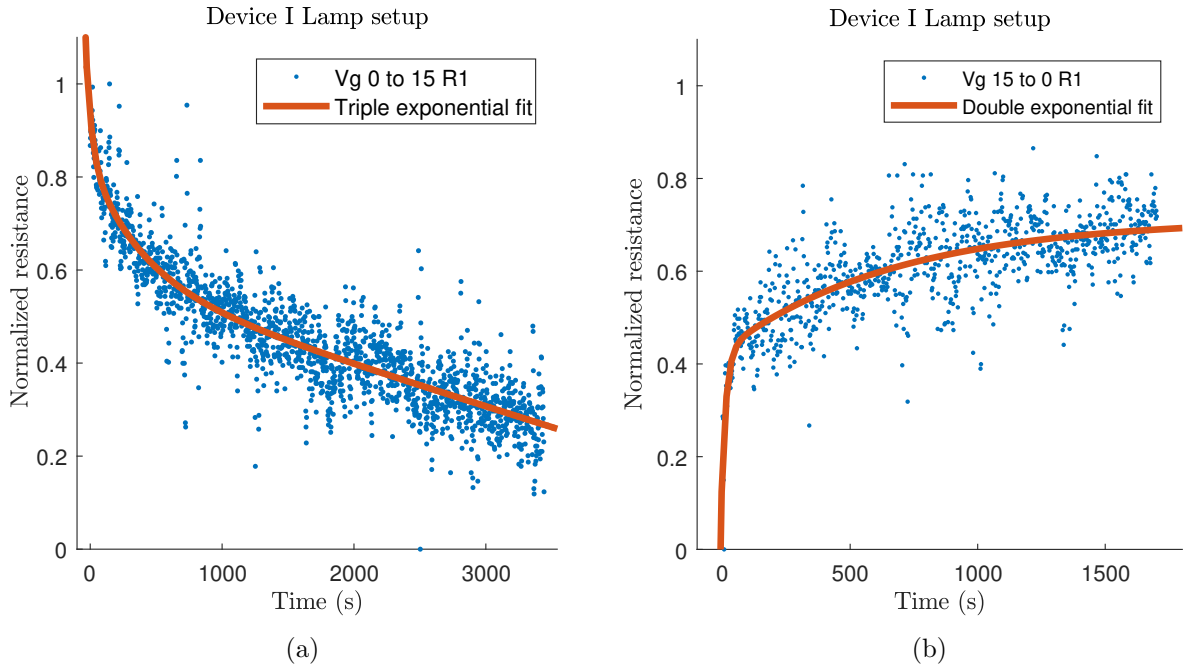
In Figure 4.4 the result of one of the measurements is shown. From this result the change of the channel resistance caused by the step change of the gate voltage can clearly be seen. The measurement starts with the gate voltage at 0 V and shows a stable channel resistance. After 1800 s the gate voltage ramps to 15 V and the resistance shows a steep increase. The resistance increases because at 15 V gate voltage the state of graphene is now closer to the CNP. Once the gate voltage arrives at 15 V the resistance directly starts to decrease. This decrease shows an exponential behavior as suggested in section 3.3. After 1.5 h the gate voltage ramps back to 0 V. Now the resistance shows a steep decrease and again decays exponentially back to its initial stable value.

From the above result we are especially interested in the decays after the step change in the gate voltage. To study these decays the time constants are extracted using exponential fitting. The fits are made using MATLAB's build-in fitting scripts which solves these type of non linear fitting problems in a least squares sense. It minimizes the sum of the squared residuals using a iterative method. For the fitting the first the region of the decay is isolated from the rest of the result. Then the time scale is shifted aligning 0 s with the first data point. Also the resistance is normalized. The coefficients which the fitting script has to find will be a lot closer to each other. This will facilitate the iterative process behind the fitting script and result in better fits. These will not affect the coefficients which give the time constants of the decay. We found that the decay could be fitted with both double exponential fits and triple exponential fits. The equation to which the decays are

fitted is given by:

$$R_{normalized} = \alpha e^{-1/\tau_1} + \beta e^{-1/\tau_2} + \gamma e^{-1/\tau_3} + \delta \tag{4.1}$$

where $R_{normalized}$ is the normalized resistance, τ_1 to τ_3 are the time constants of the decay and α to δ are also fitting parameters. Note that for fitting a double exponential $\gamma = 0$. Figure 4.5 shows a triple and a double exponential fit on the first and second decay in Figure 4.4, respectively.



(a) (b)

Figure 4.5: The exponential decays from Figure 4.4 for the step in gate voltage (a) from 0 V to 15 V fitted with a triple exponential fit (b) from 15 V to 0 V fitted with a double exponential fit.

The process described above is repeated for different steps in gate voltage on device I (15 V, 35 V, 45 V, -15 V and -35 V) and device II (15 V, 35 V, -15 V, -35 V). However no step response measurements where done with a device under illumination. As explained earlier, the insulator of device I had a breakdown before we started measuring with light. As for device II, due to limited measurement time we were not able to measure the step response with light.

Although there were large variations in the obtained time constants we were able to identify two clearly different time constants. Often the first time constant would be of the order tens of seconds and the second time constants of hundreds of seconds. If a triple exponential was fitted the third exponential was often much larger, ranging from the order 10^3 s to 10^5 s. Since the time constants had such large variations it was not possible to find a clear distinction between the time constants of the decays at different gate voltages. We calculate the average of the time constants in the range 0-100 s and 100-1000 s. The time constants larger than 1000 s are not analyzed since the duration of our measurement is too short to determine a large time constant accurately. The average is calculated for all the results of a positive gate voltage step taken together and similarly

for negative gate voltage step responses. The following time constants are then obtained for positive and negative gate voltage steps, respectively:

$$\text{Step from or to positive gate voltage:} \qquad \tau_1 = 41 \pm 25\,\text{s} \qquad \tau_2 = 452 \pm 245\,\text{s} \tag{4.2}$$

$$\text{Step from or to negative gate voltage:} \qquad \tau_1 = 39 \pm 25\,\text{s} \qquad \tau_2 = 263 \pm 168\,\text{s} \tag{4.3}$$

where the error is the standard deviation in the values used for the average. τ_1 is similar for positive and negative steps in gate voltage but τ_2 is lower for negative steps in gate voltage.

4.4 Wavelength dependence

For our last type of measurements we measured device II in the laser setup. At wavelengths from 1000 nm to 700 nm with steps of 10 nm the Dirac curve was measured. The result is plotted in Figure 4.6.

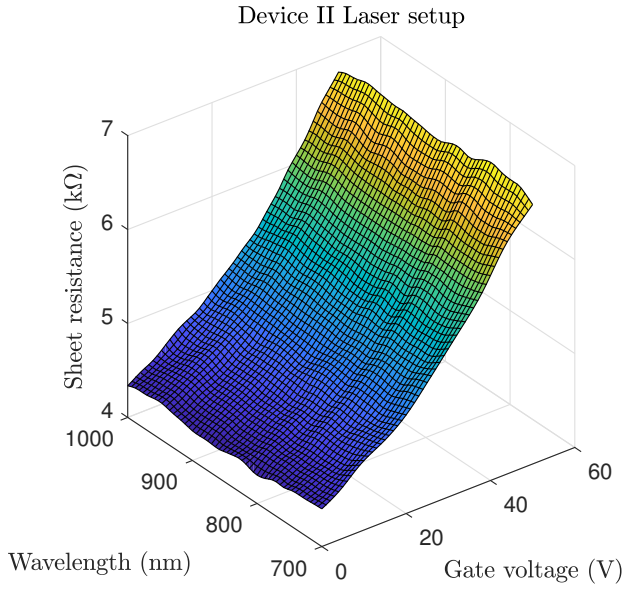


Figure 4.6: Wavelength dependence of the Dirac curve. The Dirac curve was measured at wavelengths from 1000 nm to 700 nm with steps of 10 nm. A surface was fitted trough the result for a clear visualization of the result. Due to the surface fit the noise level cannot be seen.

In the surface of Figure 4.6 small fluctuations can be found. These fluctuations are below the noise level in our signal and similar to fluctuations measured during dark measurements.

Chapter 5

Discussion

Time dependent response to light

It was expected that the resistance of the graphene channel would show an increase upon illumination with the white light source as found in previous research. Such a photoresponse was not found in device II. To formulate a strong conclusion about the photoresponse of a graphene FET on white light it should be studied more extensively. This means measuring more device and measure these devices in more regimes of the Dirac curve. So far, it can only be concluded that our device showed no significant response to the white light source.

Response to a step in gate voltage

The sign of the decays in the step response measurements is not quite what we expected. From our understanding we would expect in Figure 4.4 the resistance to show an increasing decay for the step from 0 V to 15 V and a decreasing decay for the step from 15 V to 0 V however we observed the opposite. This decreasing decay we actually see in the resistance would suggest a discharging of the Si/SiO_2 interface. Due to the charging of the interface itself the resistance initially increases but apparently other mechanisms thereafter neutralize some of this charge. This remains not fully understood.

To understand the found time constants we have to look at the Si/SiO_2 interface. Using the resistance and capacitance of the SiO_2 we can estimate the time it takes to charge Si/SiO_2 interface without defects. When calculating the so called RC time constant we find that it is much faster than a second, $\tau = R \cdot C \ll 1$ s. We were not able to measure this low time constants due to the resolution of our measurement. The time constants we did find probably correspond to other charging mechanisms such as the charging of the interface traps and bulk oxide traps. Since the interface traps are closer to and more interactive with the bulk silicon than the bulk oxide traps we expect the interface traps to be related to the smaller time constant. Furthermore the the difference in τ_2 for positive and negative steps in gate voltage could be attributed to the asymmetry in the electron and hole traps. The found time constants still needs a theoretical analysis to confirm their relation to the different charge traps. It could be that the decay is a superposition of multiple exponentials which by chance could be fitted with two exponentials. The results for the time constants showed large variations which made it difficult to provide a good analysis of these time constants. For future research I would suggest exploring the possibilities of other types of

characterization of the Si/SiO_2.

Wavelength dependence

In the wavelength dependence measurement two things were found. First of all, no change of channel resistance was measured upon illumination with the laser. Secondly, there is no wavelength dependence on the Dirac peak of the channel. The device was also measured when the power of the laser was increased to 27 mW. Even this did not induce any response in the graphene FET. The charging of the bulk oxide traps occurs via tunneling. The charge carriers which are excited in the Si layer still need some excess energy to tunnel to the trap states. It could be that a the photon energy of light with a wavelength between 700 nm and 1000 nm just was not high enough to charge these states. For further research it could be interesting to illuminate the device with wavelength in the UV regime.

Chapter 6

Conclusion

We have investigated the light response of a graphene Si/SiO_2 FET with two devices. The devices were measured both in a lamp setup with a white light source and a laser setup with a 700-1000 nm tunable laser. We measure the channel resistance of graphene with a lock-in setup in a 4-terminal geometry. Three types of measurements were done. In the first type of measurement the gate voltage was parked at a non zero voltage and the channel resistance was recorded over time. During the measurement the light source was turned on. A brief increase of the noise level of the leakage current was observed however no other light response could be identified. This is on contrary to previous measurements that showed an increase in the graphene channel resistance. For the second type of measurements the response of the graphene FET on a step in gate voltage was measured to study the charging of the Si/SiO_2 interface. From the results two time constants were found. For a positive step in gate voltage we have $\tau_1 = 41 \pm 25$ s and $\tau_2 = 452 \pm 245$ s and for a negative step we find $\tau_1 = 41 \pm 25$ s and $\tau_1 = 263 \pm 168$ s. We attribute the two time constants to two charge traps in the Si/SiO_2 interface. It is thought that the smaller time constants corresponds to charging and discharging of interface traps since these are close to the Si layer. The larger time constants corresponds to bulk oxide traps in the SiO_2 layer. For the third measurement the wavelength dependence of the channel resistance was measured between 700-1000 nm by measuring the Dirac curve at different wavelengths. Also in the laser setup we could not observe a response of the graphene FET to light.

For further research we recommend measuring on more devices. For this research the change of channel resistance upon light illumination of only one device was measured and the result is different from previous studies which were performed in the same way. One could for example study the effect of annealing the sample more extensively. We cannot exclude an effect of light on the graphene FET since it was measured in previous research. Also the use of shorter wavelength light should be considered. Charge carriers excited by higher photon energies can occupy higher energy states of charge traps and maybe induce a measurable change in the channel resistance.

Acknowledgements

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Appendix A

Additional figures

A.1 On graphene

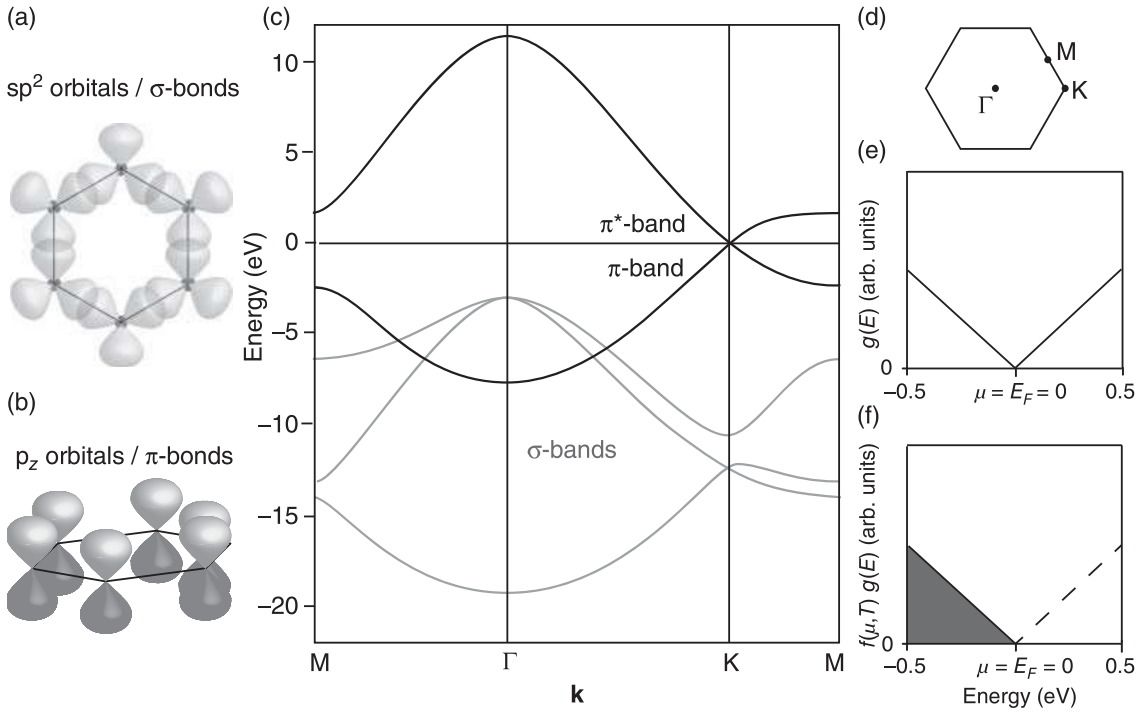

Figure A.1: Origin of electronic properties of graphene. (a) σ bonds by sp^2 hybridization. (b) Out of plane p orbitals. (c) Part of the band structure. (d) Corresponding points on the first brillouin zone. (e) Unoccupied density of states near the Fermi energy. (f) Density of states near the fermi energy at $T = 0$ K. Figure adapted from [4].

A.2 Optical microscopy on the fabricated devices

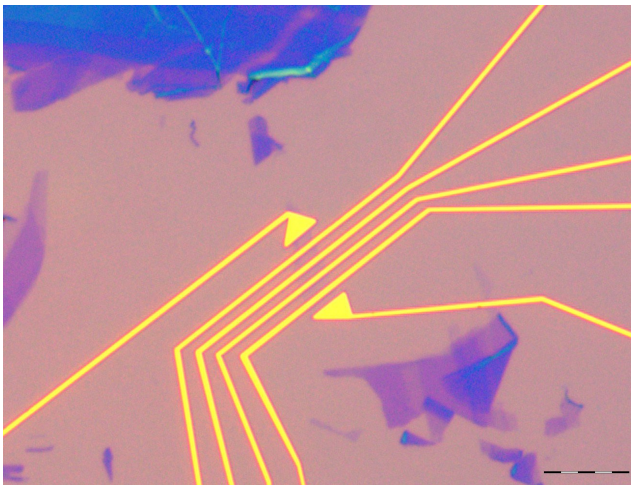

Figure A.2: Optical microscope photograph of the first device. The scale bar is 10 μm. It has two single and four running contacts, all double padded. Al the contacts were double padded so the sample could be bonded again after potential annealing in the tube furnace. Bonding twice on the same pad has a risk of breaking the gate.

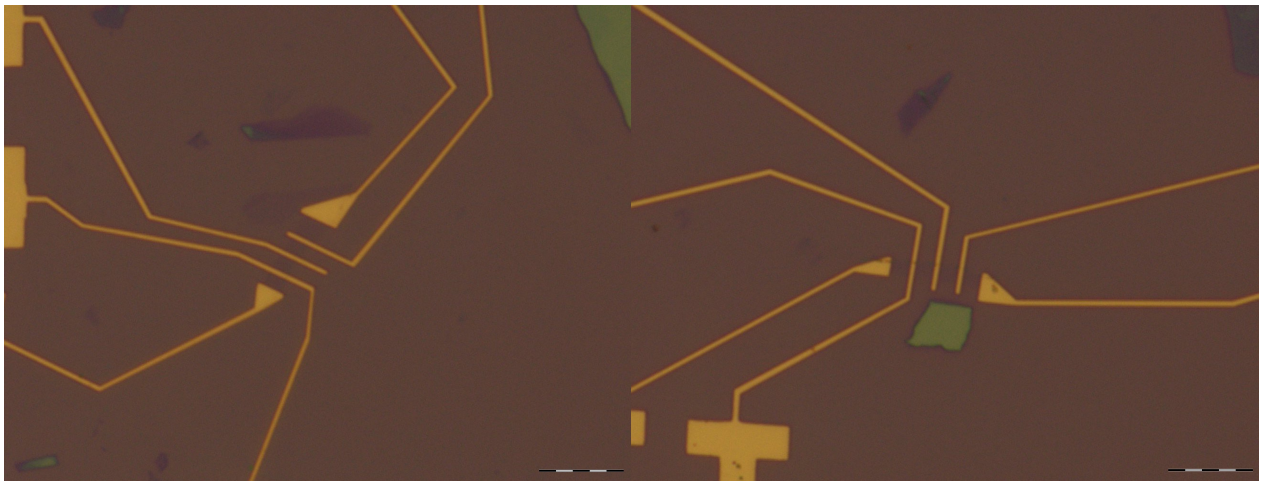

Figure A.3: Optical microscope photographs of the second device. The scale bar is 10 μm. This device has two flakes close together. Both flakes have four single and one running contact.