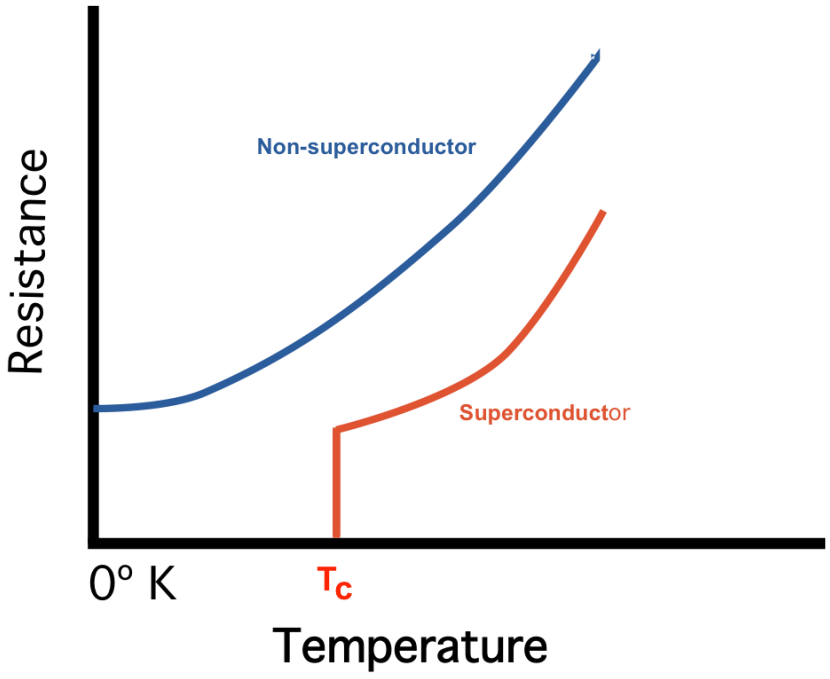
Superconductivity in multilayered WS_2 and preparation of BSCCO

From multilayered flake to device



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1 Introduction

Superconductivity is an interesting classical quantum mechanical phenomenon in the field of condensed matter physics. Heike Kamerlingh Onnes discovered it in 1911 in Leiden, the Netherlands and after 100 years of active study, it remains to be a surprising field of research. A property of superconductivity is that there is no resistance, thus no power loss. The crux is that superconductors only work at low temperatures. By doping a superconducting material, we can raise this temperature limit. This can be done by the field effect, intercalation or mechanical pressure. Imagine household applications or transport systems that can run forever without loss of power! Other exotic physical phenomena shown by superconductivity include the Meissner effect, allowing you to levitate whilst standing on a nearby magnet. In electronic devices, the superconductivity phenomenon is used for rapid on-off switches by changing either the external magnetic field or temperature [1]. Many of the physics shall be explained in this thesis. We shall focus on the field effect and its consequences on two materials: WS_2 and $BSCCO$.

WS_2 is a superconductor and by changing the amount of unit cells the material is made of, monolayer, bilayer, and bulk, one changes the properties enormously. The monolayer case has already been studied well by researchers at the University of Groningen [2]
Hence, multilayered WS_2 enters the field. WS_2 is a part of the group-VI transition metal dichalcogenides. A transition metal is a metal that forms one or more stable ions which have incompletely filled d orbitals, and a chalcogenide is in the VI A group of the periodic table with six valence electrons. In WS_2, W is the transition metal atom (Tungsten or Wolfram) and S_2 the chalcogenide atom (Sulphur). One layer of W atoms is sandwiched between two layers of S_2 atoms. WS_2 has an energy gap, which is in the infrared and visible range and this causes interesting properties as will be explained later[3]. We are testing a multi-layered WS_2 as the next step since in monolayer WS_2, superconductivity has already been found. Another interesting material is $BSCCO$, a high-T_c superconductor that we shall also test for superconductivity.

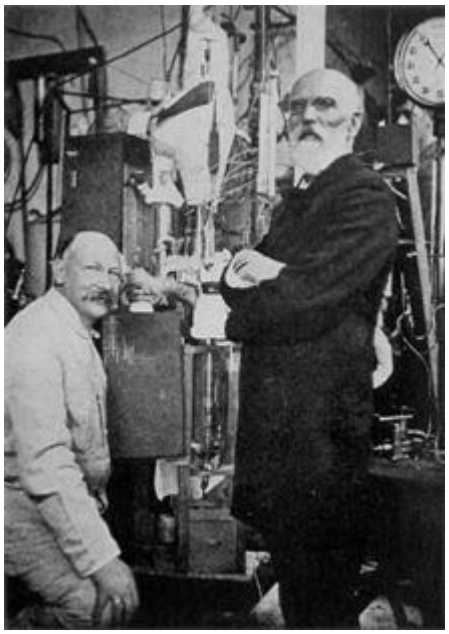

Figure 1.1 Heike Kamerlingh Onnes and Johannes Diderik van der Waals (r.), in Leiden, 1908.

2 Physics of superconductivity

2.1 Introduction to superconductivity

Superconductivity is a phenomenon when the resistance of a material becomes zero. The electrons can thus flow through the material unhindered. This is useful because there is then no power loss as the resistance can be calculated via $P = IR^2$. The process goes as follows: imagine an incoming electron as in Figure 2.1. The superconducting state is a many-body phenomenon, which involves attractive interaction of two electrons and phonon in a crystal lattice. The lattice points of the atom are positively charged and the incoming electron feels an attractive force towards these lattice points. The lattice point itself will also be partially displaced. Another electron, with an opposing momentum, will now have an easier time to travel through the lattice due to the lattice point displacement. The other electron needs to have an opposite momentum in order to obey conservation of momentum (otherwise current would flow) so the momentum k_f and -k_f should together be zero (at rest) and both electrons lose all their energy and drop to the zero-energy state.

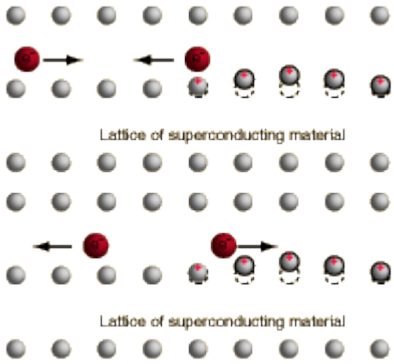

Figure 2.1 Two electrons with opposite momentum will experience attraction due to ion displacement.

A condition for the electrons to "pair up" is for both of them to have an opposite spin to be together otherwise they would violate Pauli's exclusion principle. An electron is a fermion so the Pauli Exclusion Principle applies. However, an electron pair is a boson, so the principle does not apply. Thus, many pairs can occupy the same energy state. In other words, degeneracy can now take place and the electrons form a crowd of Cooper pairs. Another demand is that the energy of phonons, the collective vibration of lattice points, should become sufficiently low to decrease the resistance experienced by the electrons. This happens at low temperatures. Once all conditions are met, the electrons move as a whole, called a superfluid.

It would also be easy to break this "pairing" because both particles are electrons and like charges repel. The energy of this Cooper pair *has an order of magnitude* of $10^{-3}eV$ which is small if we compare it to room temperature energy of $\frac{1}{40}eV$. Therefore, in order for the temperature not to surpass the binding energy, we need to decrease the temperature. By using the relationship, $E = kT$; $k = \frac{10^4 eV}{K}$ and $E = 10^{-3}eV$ we can see that the temperature has to be 10K. Of course, this is an example, as many critical temperatures are much higher. This is because the Cooper pair energy differs per material. Consider a material with heavier ions, these ions have a higher spring constant and are harder for the electrons to attract while keeping the temperature constant. This results in the electrons having a lower binding energy $\Delta = \hbar\omega_D \exp(-\frac{2\pi k_f}{m_e l V_0})$ where V_0 is the attractive potential energy due to Coulomb forces, and l the distance the ion moved for a time of half the period (when it reaches its highest point) or in formula $l = \frac{v_E T}{2} = \frac{\pi v_e}{\omega_D}$. This is called the isotope effect and the T_c affected by this can be described by $T_c \propto \frac{1}{\sqrt{mass\ of\ isotope}}$ [4].

2.2 Magnetic field in superconductors

Our materials are type II superconductors. Unlike type I superconductors, type II are not formed from a single element and this means there are impurities. Superconductivity disappears slowly as opposed to the instantaneous type I superconductors. In type II superconductors there exist 3 regimes, this is shown in Figure 2.2, the green arrows depict the external magnetic field

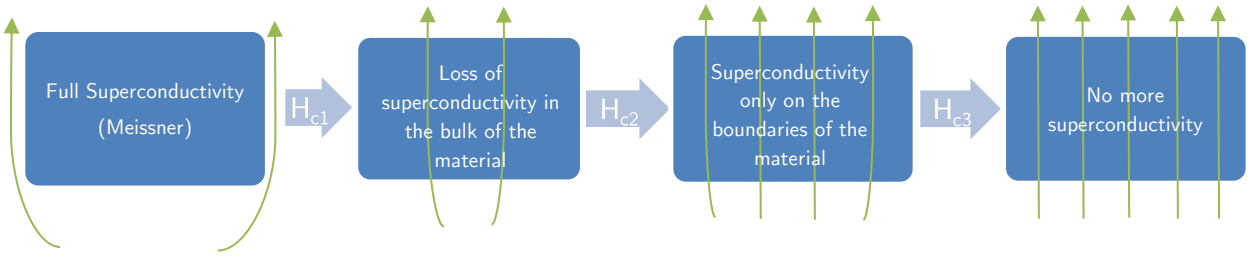

Figure 2.2 Three different phases of superconductivity.

lines.

During the cooling phase of a superconductor (while under a magnetic field) the magnetic flux that was still there is now slowly getting expelled after T_c has been reached. If the magnetic field is increased while in the superconductivity state, the superconductor changes into a partial diamagnet; regions of non-superconductor vortices appear in the bulk of the superconductor and multiple vortices of currents are formed. These are mainly formed around impurities. The superconducting region creates a current to oppose B_{ext}. The penetration depth, how far the external magnetic field can penetrate the material before being canceled by the induced field, is a defining characteristic of a superconductor and is called the London penetration depth which is $\lambda_L = \sqrt{m/\mu_0 n q^2}$ [5] where m is the mass of the charge carrier, n the charge carrier density, q the charge and μ_0 the magnetic permeability in free space. This is illustrated in Figure 2.3, the green-colored circles depict current generated by the penetrating magnetic field. The red-colored supper current is induced because the net current has to be zero and this causes a magnetic field that expels B_{ext}. Between Hc_2 and Hc_3 the field becomes strong enough to penetrate everywhere except for the edges. Once the vortices overlap, superconductivity is destroyed and this is called the orbital limit. Above Hc_3 there is no more superconductivity present. A classical way to view the orbital limit differently goes as follows: the spin up and spin down Cooper pair revolve around the nucleus and create a centripetal force that is dependent on the magnetic field. Once this magnetic field is too big, the electrons shoot off as a car would by speeding in a too sharp turn.

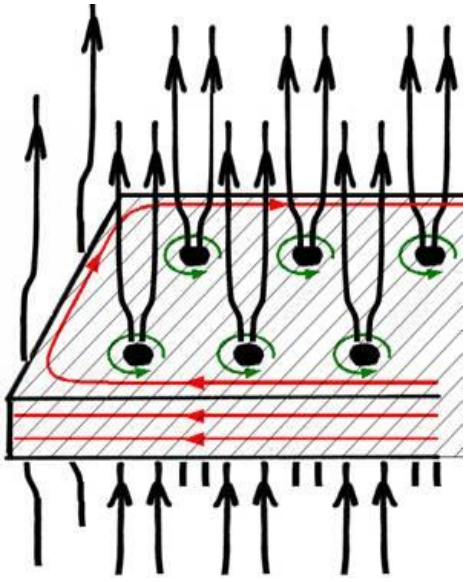

Figure 2.3 Between H_{c1} and H_{c3} a quantized amount of magnetic field is let through, called fluxons.

In WS_2 the spin-orbit-couple (SOC) is more pronounced due to heavier atoms resulting in electrons closer to the nucleus, with more revolutions per second concluding in a larger B_{eff}. This causes a higher splitting in the valence band.

One can also pin the flux by applying a magnetic field to the material and then lowering the temperature below T_C, effectively trapping the magnetic flux because it becomes a perfect diamagnetic material. This can lead to

interesting phenomena where the superconductor causes a steady levitation effect by having all the magnetic field lines from an external magnet getting expelled but locking the superconductor in place. Applications of superconductors are, among many others, bearings that do not wear out and the famous Maglev trains [6] as shown in Figure 2.4.

How does a magnetic field break superconductivity on the quantum scale? For this, we have to go back to Cooper-pairing again. The pairs that exist due to the low temperature and are now one whole. To break this pairing, one thus needs to supply energy to break all the bonds as the fluids acts as one condensed entity. The magnetic field supplies this energy and breaks the spin-up spin-down Cooper pairing as the magnetic field makes it so that parallel spins go along the field and antiparallel spins go against the field thus ripping apart the Cooper pairs. This could be thought of as the Zeeman Effect due to the internal field generated by the movement of the electron around its nucleus. Once the Zeeman energy is bigger than the superconducting energy gap, the Cooper pair breaks. The expression for the Zeeman energy is $H = \frac{\mu_B}{mc}\sigma \cdot (E \times p)$ [7], where σ is the Pauli matrix, μ_B the Bohr magneton and p the momentum of the electron, E the electric field and hence the change in potential experienced by the dipoles of the atoms (∇V). The superconducting energy gap is $\frac{7}{2}kT_c$ [8]. Combining this gives rise to the Pauli limit $\frac{1.8kT_c}{\mu_B}$ [9].

Figure 2.4 Maglev train being tested for the Chuo Shinkansen Tokyo-Osaka Maglev line in Japan. The extended nose is to reduce drag and move more smoothly through tunnels. The line should be operational by 2027 [33].

2.3 Ising superconductivity

In an Ising superconductor, internal magnetic fields protect the Cooper pair from the external magnetic field as much as possible. Consequently, we can exceed the Pauli limit, which according to Bardeen, Cooper and Schrieffer theory, BCS, is $B_p = 1.86T_c$ [10]. To clarify, Cooper pairs are bosons and form with a net angular momentum $S = 0$ or $S = 1$ due to a triplet of electrons. When a strong enough magnetic field is applied, spin-splitting ensues and this destroys the Cooper pair. This is especially strong in heavy metallic elements, with $4d$ electrons in the outer shell, such as WS_2.

Our goal is to find out for which Bc_2, the upper critical field, superconductivity stops. We also apply an electric field out-of-plane to the electron gas. For centrosymmetric potentials, this electric field causes a Rashba spin-orbit coupling that is in-plane. This can help to preserve the Cooper pair up until a higher Bc_2. See Figure 2.5a). For non-centrosymmetric potentials, this contributes to the SOC and as a result lowers B_{c2}. See figure Figure 2.5b).

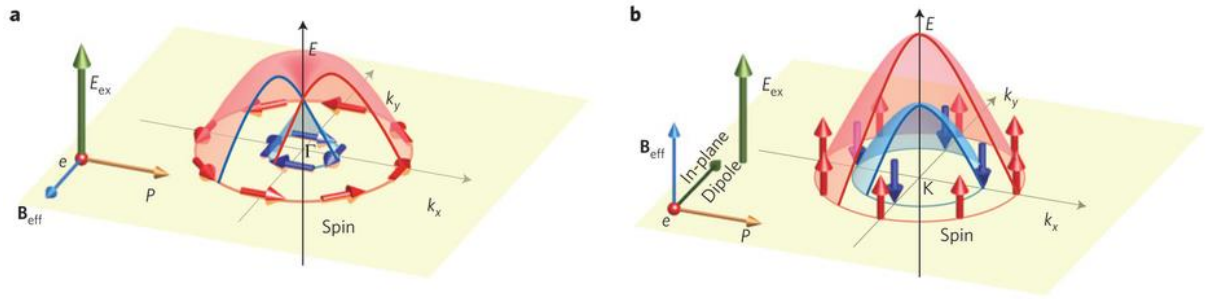

Figure 2.5 a) In layer inversion, an electric field can break symmetry and induce B_{eff} by Lenz's law. b) In a non-inversion symmetric structure, this causes an increase in splitting a la Zeeman [23].

Let us consider all scenarios starting with scenario D in Figure 2.6. We see that when B_{ext} ($=H$) is perpendicular to the plane, there is no coupling between the spin and the field, hence you can increase B_{ext} significantly until the Cooper pair gains a higher Zeeman energy $H = \pm m \cdot B$ than E_g. Here m is the magnetic moment and the superconductor energy gap $E_g = \frac{7}{2}kT_c$, according to BCS theory [8]. However, when you apply an electric field in-plane, the critical field at which the Cooper pair breaks is only $\sqrt{2}$ as strong as Bc_2 [11]. This is scenario C. Scenario B would occur when B_{ext} is orthogonal to the hexagonal reciprocal lattice leading to a 100 times increase in B_{c2}. We do *not* want to apply the portrayed out-of-plane magnetic field as this contributes to the Zeeman SOC and breaks the Cooper pairs at a lower Bc_2. This would be scenario A. Here we want a magnetic field *in plane* to reduce the coupling between B_{ext} and the spins to a minimum.

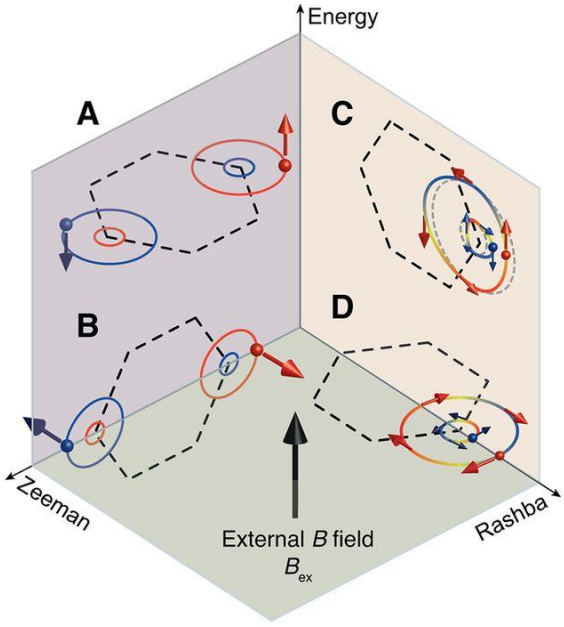

Figure 2.6 Different scenarios can occur depending on inversion symmetry [11].

By going from a monolayer to bulk system, we go from a non-centrosymmetric to a centrosymmetric potential and hidden spin polarization occurs. This means that one individual layer produces a dipole field (due to asymmetry)

but another layer produces one opposite to this field, effectively cancelling all momentum. Hence, the overall momentum of the electrons becomes zero. The result is that B_{eff} vanishes. We can see this in Figure 2.7 where R denotes the Rashba effect and D the Dresselhaus effect.

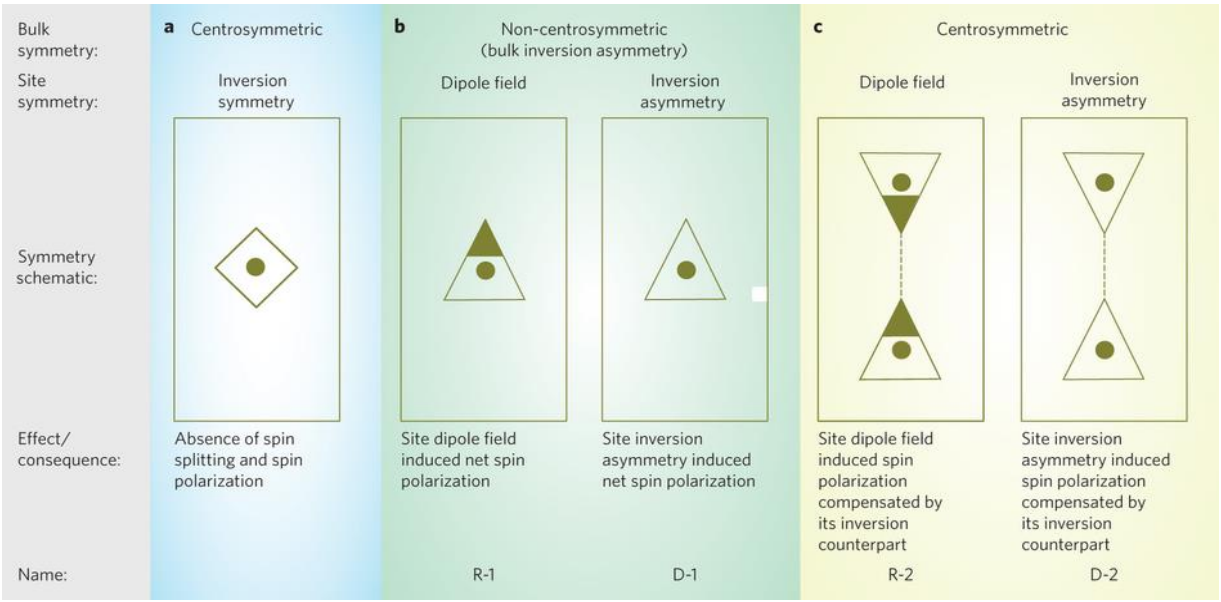

Figure 2.7 In a, we see a point of inversion symmetry (centrosymmetry) causing no spin splitting. In b, either a local dipole field (either intrinsic or due to external electric field) or the site inversion asymmetry leads to local Rashba (R-1) or local Dresselhaus (D-1) effect. In c, their inversion partner compensates the spin polarization from each sector [27].

The Dresselhaus spin–orbit effect was discovered by Dresselhaus in 1955 for zinc-blende structures, but is generally present in crystals with bulk inversion asymmetry (*BIA*). The strength of the Dresselhaus spin–orbit interaction depends only on the atomic elements forming the crystal structure. Thus, the Dresselhaus effect comes from the lack of inversion symmetry of the crystal, called bulk inversion asymmetry (*BIA*). The Rashba effect comes from the inversion asymmetry of the structure in single layers or 2D systems. The Dresselhaus and Rashba spin–orbit interactions lead to different spin patterns. For the Dresselhaus spin–orbit interaction, the leading term is described by an effective magnetic field *B* proportional to $(k_x, -k_y)$. The effective magnetic field of the Rashba spin–orbit effect *B* is proportional to $(k_y, -k_x)$ [12]. This effect of splitting due to asymmetry is used in valleytronics, a field evolved from spintronics that exploits the different energy levels as in Figure 2.8 below.

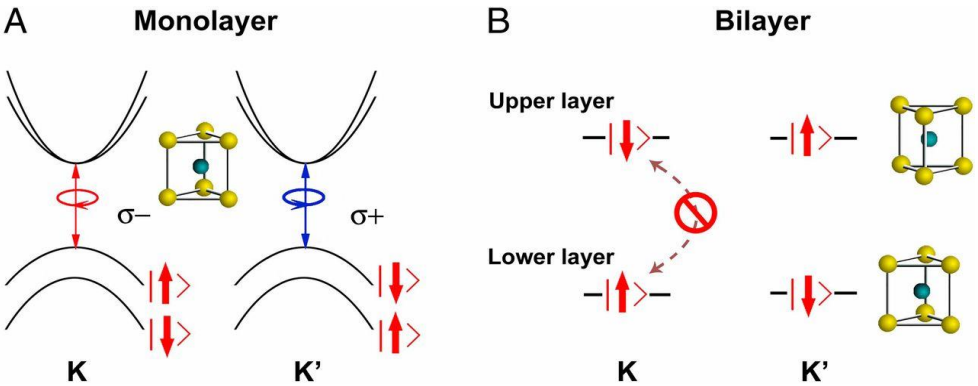

Figure 2.8 K-valleys. Here we can cross the bandgap by shining circularly polarized light as in the figure. Clockwise-polarized light gives rise to a transition in the K+ valley and counter clockwise in the K- valley. Spin conservation has to be uphold. In B) a lack of inversion symmetry makes a transition no longer possible. This research is called valleytronics [32].

3 Device physics and crystal structure

3.1 Band structure

To explain what happens when we increase the layers of our sample, WS_2 is used as an example. The band structure in WS_2 is formed as in Figure 3.1. The d-electron orbits of the metal atoms hybridize at point K and are not moved by interlayer coupling as they are in the middle of the *S-W-S* sandwich. The states near the point Γ have characteristics of anti-bonding p-orbits of the group VI chalcogenide atoms and they strongly change when the thickness of the WS_2 changes. Why does this change? Tungsten is paramagnetic and the two layers that wrap around it are made of Sulphur, a diamagnetic. This causes interlayer coupling [13]. Hence, the bandgap decreases as the thickness increases because the overlapping d-orbitals cannot fill the same energy level obeying Pauli's exclusion principle. The bandgap changes from about $1.3eV$ to $2.1eV$ when the thickness decreases. The energy on the y-axis is approximated using Hartree-Fock approximations. [14]

Because our TMD is multilayered, the bottom of the conduction band is not right above the highest point of the valence band, leading to an indirect bandgap. The thinner the material, the more the system reaches a direct bandgap due the quantum confinement effect (and the more the valance band maximum goes to the K points). Phononic energy has to be supplied to the crystal in order to cross the same energy difference (denoted by the red arrow).

As explained before, one feature of thin TMDs is spin-orbit-coupling due to the electromagnetic interaction between the electron its spin and the magnetic field generated by the electron its orbit around the nucleus. In Figure 3.1 this happens at the K points and it is the same as the energy difference that electrons experience in an external magnetic field of 10^2T (Zeeman splitting energy) [14]. This value due to the spin-orbit-coupling can be exploited in the field of spintronic devices.

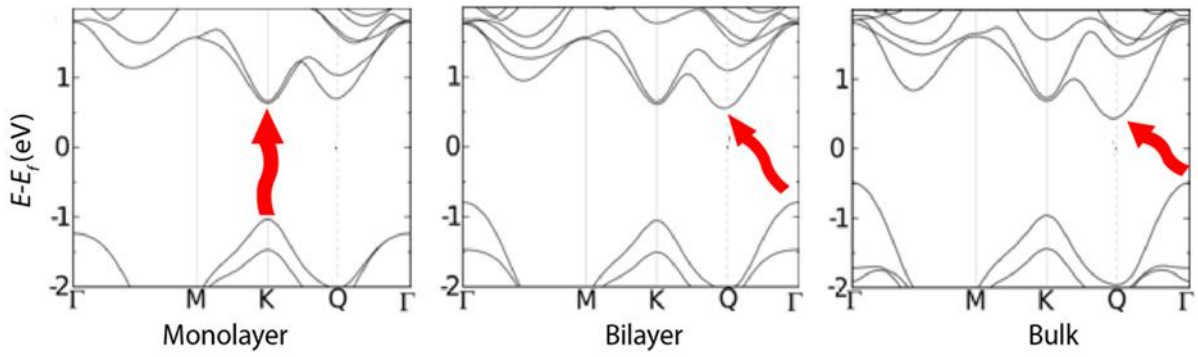

Figure 3.1 Band structure WS2. Author's adaptation from [30].

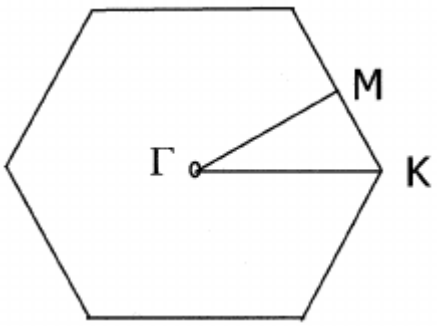

Figure 3.2 Hexagonal Brillouin zone.

3.2 The stacking of the layers

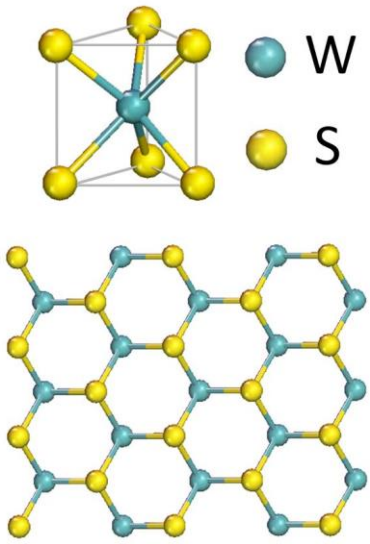

Figure 3.3 Crystal structure WS_2 [25].

WS_2 is a covalent bond and forms a network of bonds that are a foundation for more layers to form on. The stacking of the layers happens thanks to Van der Waals forces. This is called van der Waals epitaxy (from Greek "an ordered manner"). The van der Waals forces hold the different layers together. As you can see in Figure 3.3, the WS_2 shows a hexagonally packed structure, its lattice parameter $a = b$ and has a value of 3.153Å and the lattice parameter c a value of 12.253Å. These values were obtained by knowing that, in equilibrium, the lattice experiences zero forces in any direction as it is then stable (causing a zero-stress tensor) and using this knowledge in the Density Functional Theory. [14]

As the name implies, $BSCCO$ has a more complicated structure as in Figure 3.4 and mainly the part with the $CuO2$ superconducts. This cuprate superconductor has a critical temperature that is very sensitive to hole doping of oxygen atoms and the number of Cu-O layers in the unit cell. Thus, many variations in T_c are possible and this can be altered by changing the number of Cu-O layers; the general formula for Bi-based high temperature superconductors is $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ [15] where n is the number of Cu-O planes. Like in any other crystal, the X-ray powder diffraction patterns and the distance between the planes determine the lattice constants of this orthorhombic figure. For the 2212-$BSCCO$, the lattice constants are a=b=3.82Å and c=30.85Å. [16]

$BSCCO$ is a very interesting superconductor as it can reach temperatures around 110K, classifying it as a high temperature superconductor (HTSC)

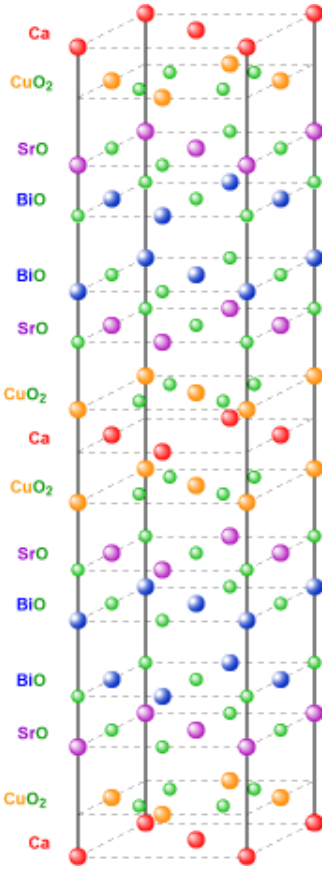

Figure 3.4 Crystal structure BSCCO [26].

3.3 FET-doping and Ionic liquid gating

In order to study the superconductivity of the samples, we do *not* need to shift the Fermi level up or down. Nevertheless, to make devices, we *need* to make sure the sample conducts. We can tune this conductivity by shifting the Fermi-level into either valence or conduction band. Naturally, we then need to change the semiconductor from an intrinsic type into extrinsic by doping. This is doable but there is a better way to control the Fermi level.

The better way is the field effect transistor (*FET*). This is a gate on top or below the insulating layer, which has a positive or negative voltage over it. The whole structure is called a metal oxide semiconducting field effect transistor (*MOSFET*). By applying a positive voltage over the gate, the holes on the other side of the insulator are pushed away and only electrons remain. These flowing electrons (when the source and drain voltage is > 0) constitute a current and this is called the inversion layer. Because the displaced holes are moved away from the channel, a reacting electric field is generated until there is no more vertical movement and the channel is stable. By applying a negative voltage over the gate, the electrons are pushed away and holes become the dominant charge carriers. Unfortunately, due to this reactive electric field, the FET method only shifts the Fermi-level a little bit (either toward the CB for $+V_g$ or toward the VB for $-V_g$). Also, the insulator has to be relatively thick to prevent leakage of charge and this limits the charge density. The limit of how much voltage can be applied is capped by the breakdown voltage which is 150V for silicon oxide.

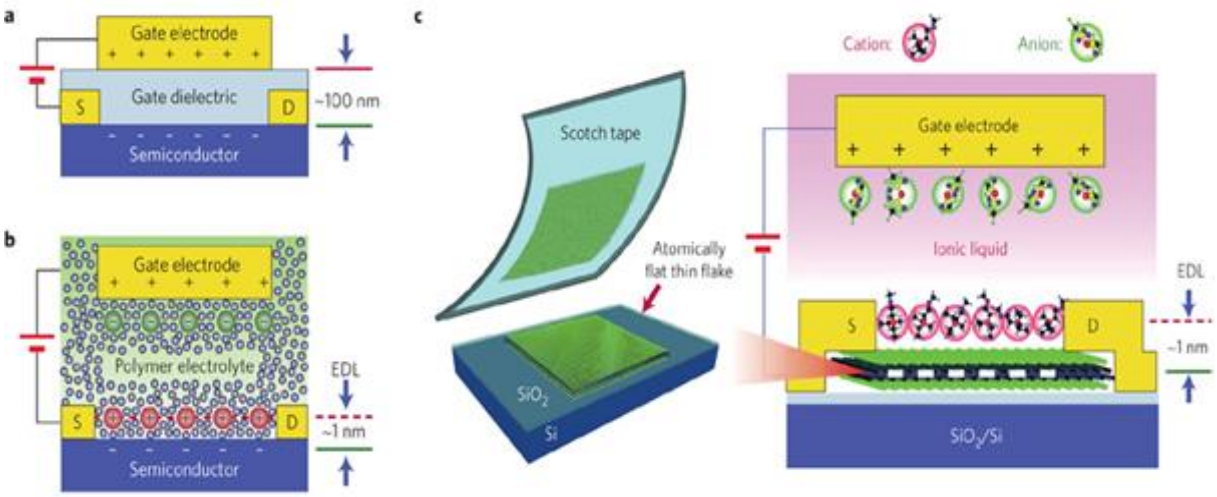

Figure 3.5 Conventional FET device with thick (~100 nm) gate dielectric. b, An EDLT device in which the dielectric is replaced by an ionic-salt liquid such as DEME-TFSI. When the gate has a voltage on it, a thin electric double layer forms on the surfaces of the semiconductor channel. c, Modified liquid-gated EDLT device in our work ($DEME^+$: red spheres; $TFSI^-$: green spheres). The $DEME^+$ cations accumulate on the channel of the cleaved WS_2 flat surface, and an electric double layer, which acts as a capacitor with nanoscale thickness, forms at the liquid/solid interface [24].

By applying ionic liquid gating, we can significantly increase the conductivity. A positive voltage is applied to the gate far away from the source and drain. Instead of an insulator, an electrolyte (the liquid) is in its stead and hence the positive ions are pushed to the gate in between the source and drain. These holes now attract electrons due to the Coulomb force from the thin flake and henceforth an electric double layer (*EDL*) is formed. The ionic liquid is now frozen as the temperature is lowered to the glass transition temperature T_g of 182K [17]. This thin layer acts as the "gap" in between the lower part of the silicon oxide and the liquid. Because this distance is so

small, the capacity is at least 100 times higher than a solid gate where the insulator is much thicker. The limit of how much voltage can be applied to the liquid DEME-TFSI, before a chemical reaction takes place and renders the solution useless, is 5V, empirically found. This chemical reaction happens because the voltage makes it so that the ion takes up a sulphur atom from WS_2 and neutralizes with the positive ion to be dissolved. The sulphur atom is negative as it is more electronegative than the tungsten.

From a simple calculation, one sees that the electric field is thus much higher for ionic liquid gating and thus also its charge density.

$$FET: E = \frac{V}{d} = \frac{150V}{300 * 10^{-9}m} = \frac{5MV}{cm} \text{versus } EDL: E = \frac{5V}{0.001m} = \frac{50MV}{cm}$$

Equation 1 Calculation of the electric field: FET vs. EDL.

In Figure 3.6 we see an example of ionic liquid gating. As one can see, the liquid is held together by surface tension and can be frozen once enough charge carriers are in the EDL.

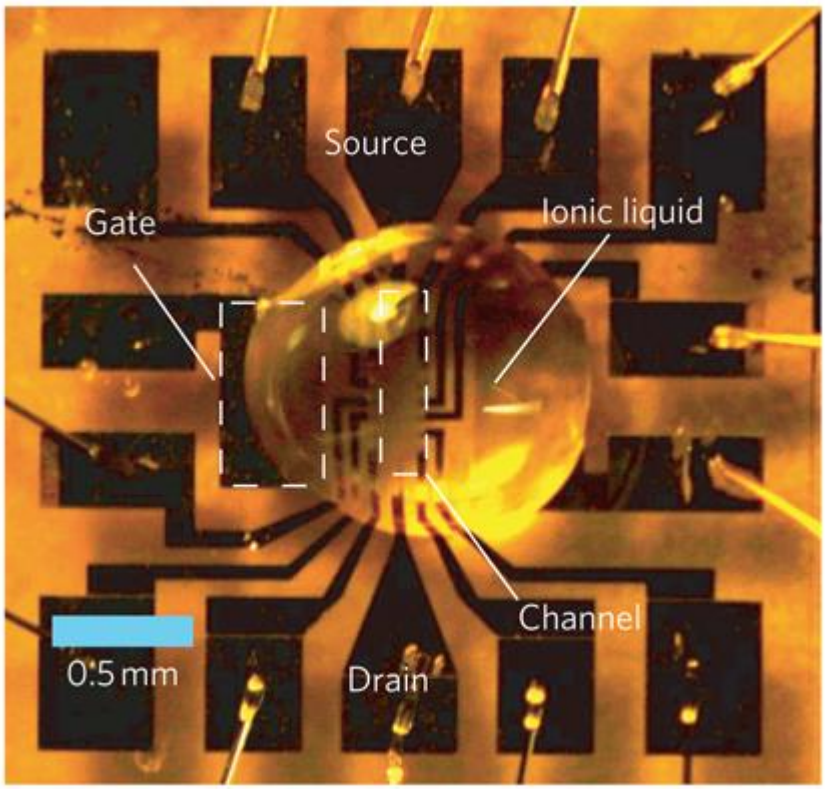

Figure 3.6 Example of ionic liquid gating [34]

3.4 Schottky-barrier and energy diagrams

The reason why semiconductors are useful is that they only allow current to pass when a certain voltage is applied. This is called the threshold voltage. One can change this by tuning the Fermi-level (the chemical potential by all electrons) and moving it either towards the valence or conduction band. This can be done by applying a negative or positive gate voltage respectively as explained before.

For our testing purposes, the samples are all semiconductors and the electrodes (made of gold) are metals. The junction between both types of conductors gives rise to a Schottky barrier due to a mismatch in Fermi-levels of the two different materials. Because of a different type of semiconductor; either intrinsic, n-type or p-type, different *I-V* characteristics will appear. One can thus control the current allowed to flow by adjusting the doping and gate voltage. You can distinguish between the different types by realizing that it takes a small positive voltage for the channel to get into the conduction band (n-type) and a small negative voltage for the channel to get into the valence band (p-type) as in Figure 3.7.

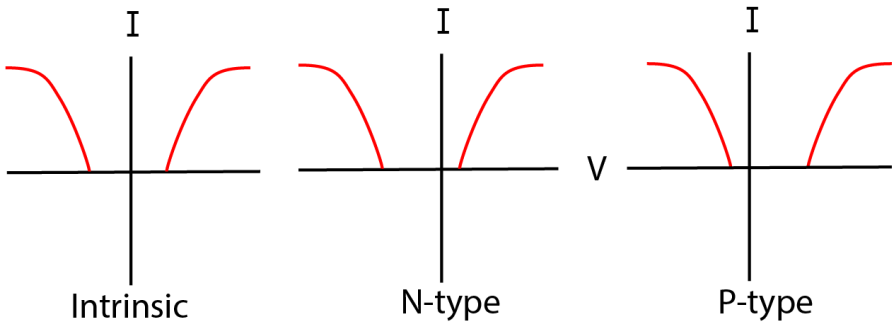

Figure 3.7 I-V characteristics for a semiconductor (transistor) using alternating current.

The semiconductor-metal energy diagram is shown in Figure 3.8. For an n-type the Fermi level is close to E_C, for a p-type the Fermi level is close to the E_v. The ϕ represents the work function and the Fermi levels have to align (the system wants to come into equilibrium). This causes E_C and $E_v$to bend and a Schottky barrier to form which is defined as Φ_B.

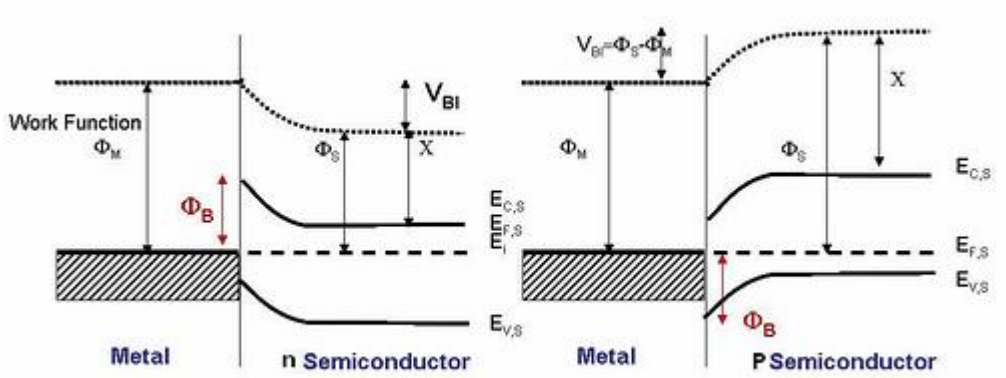

Figure 3.8 Energy diagram for a metal-semiconductor junction a.k.a. a Schottky junction. Here X represents the electron affinity. [28]

The energy that has to be supplied (by changing the built-in voltage V_{BI}) to overcome this barrier is defined as $q\Phi_B = q(\Phi_M - \Phi_s)$ where Φ_M and Φ_S are the work function of the metal and semiconductor. X is the electron affinity, the energy needed to bring an electron into vacuum.

4 Fabrication process

There are two different approaches to making samples. On one hand, layers can be detached from an already existing crystal, called the exfoliation method; on the other hand, the crystalline layer can be grown directly on a substrate surface as in Chemical Vapor Deposition (*CVD*) method. We use the exfoliation approach in which a piece of tape is used to peel graphene flakes off a chunk of the crystal. This results in micrometer-sized crystal fragments, which are placed between electrodes to make a transistor.

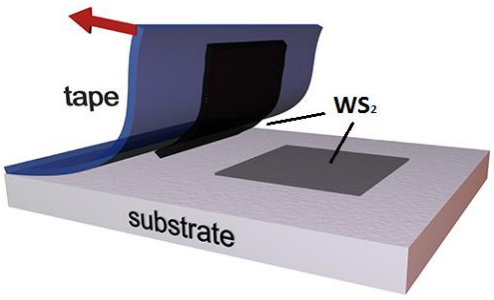

Figure 4.1 The exfoliation method.

By repeated peeling, you go from multiple-layer to fewer layer. In the end, the glue from the tape is dissolved using acetone to detach the tape. Now one last peeling with an unused tape is done. When we have a thin enough layer, we put it underneath the microscope to start color-coding. After this we can make our device. The precise, more elaborate, steps are listed below.

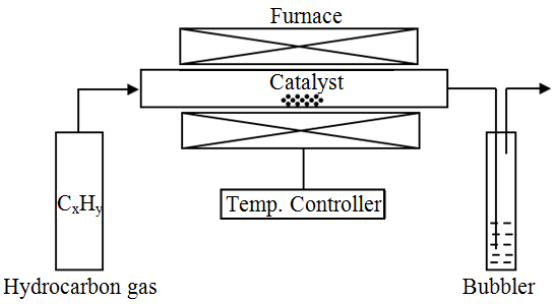

Figure 4.2 An example of a CVD set-up. The crystal flakes grow at high temperatures.

4.1 Steps taken

The very first thing we do is obtaining the marked wafers. If we do not have marked wafers, we either make them or use an unmarked wafer. Making markers is described in Process of making markers.

If we want an unmarked wafer, we separate the gold from the wafer to have a clean wafer of silicon oxide. We clean it with acetone first, this dissolves much of the gold from the wafer. The nitrogen blowtorch is used to blow off part of the residue without oxidizing it. Now part of the acetone is still left and we use IPA to remove this residual acetone. We can use this clean substrate later.

Next, we start the cleavage; we need a small box for the sample and necessary equipment such as tweezers and Scotch tape. We use the Scotch tape to peel off crystal layers onto more tape. Finally, we move over the thin layers of the crystal of interest onto the sample as if it were tape. This is easily done as the van der Waals forces between the substrate and the WS_2 is stronger than between the tape and the WS_2. See Figure 4.1.

Suppose we already have sample on the marked wafer like in Figure 4.3. The steps to go from flake to device are listed below.

Figure 4.3 Flake of WS2.

Step 1. We have to spin-coat the sample in order to prevent oxidation. We put a few droplets of PMMA A3 on top of the sample. PMMA is a positive photoresist, meaning it will evaporate while under exposure of UV light.

Now the sample is put in the spin-coater; 10 seconds at 1000RPM and 60 seconds at 4000RPM so that the coating has been spun over the sample. Next, we bake the sample at 90C° for about 5 minutes.

Step 2. We find big enough flakes to put the electrodes on and we try to distinguish the different layers (mono, bi, triple etc.). We take pictures when we find a good region, which is defined as having big, sharp flakes. The sharper the flaker, the better as this means the flake is along the crystal line (e.g. 60° or 120°). We do this with the help of the CCD camera. We fix certain parameters such as the intensity of the LED (preferably high). The camera is cooled down to -20 degrees Celsius to avoid any thermal radiation distorting the image. This is done using the Peltier effect, which is opposite to how a thermocouple works. *The Peltier effect* works by applying a voltage difference between two materials in the microscope and thus creating a temperature gradient, making sure the camera cools down.

One also has to figure out which filter in the CCD ought to be used. By knowing that gold has the highest reflectivity, we determine that the blue filter gives the darkest image. We can redirect the light out the optical microscope via the knobs on the side of it to either the computer or visual output. Once the focus is in order, we save the image as a .TIFF file. By using Micromanager and Origin to find out the peaks in intensities, we can pinpoint which layer thickness corresponds to what green channel count. This is the photons picked up by the CCD. We also take color pictures using the CMOS camera to use them in designing our electrode layout.

Step 3. Now we find the coordinates for the sample to be put in. By knowing preexisting markers (also laid upon a flat square plat next to the substrate), we can found a coordinate system which we use later. We find the [0,0], the [0,8] and the [8,0] coordinate in the relative coordinate system and find the absolute coordinates. By filling in the [0,0], [0,8] and [8,0] coordinates in the left part of the screen we get new absolute values. We note the error between the absolute values dx. We also note the coordinates in the absolute system (.....;.....)

Step 4. In the design step, we insert the image of the sample and orient it accordingly. We also scale the image to make sure that the dimensions in AutoCAD are fit accordingly. We can do this by giving a value of 100 micrometer between each marker. Because the pictures that are within our region of interest (such as flakes we want to measure) are taken with a higher magnification, we want to fit this on top of the pictures taken with a lower magnification. This is done by moving the high-res picture and fit it to the marker of the low-res picture.

After the orientation and scaling has been done, we design Hall-bars on top of the flake. The left- and rightmost part of the Hall bar are the source and drain. Electrodes are to be applied in between these and measure the conductivity. We can do this a maximum of 20 times as this is the maximum amount of devices due to the socket pin limited later imposed by the chip carrier. We need the Hall bars to later find out the charge density and $\rho_{\blacksquare}$ as will be explained in 9.1.

We have 2 patterns with different doses in our sample as in Figure 4.4. For the area with a width of 0.4-1µm, we give it a dose factor of 1. For the area of 1.2 to 2µm we give it a dose factor of 0.75. This is to make sure the Hall-bar shape is formed.

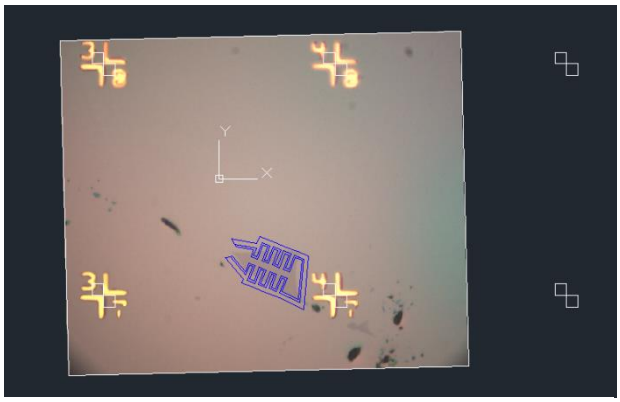

Figure 4.4 Design of Hall-bars in AutoCAD.

Step 5. The next step is E-beam lithography etching using the electron beam. See 12.1.

Step 6. The Development takes place. Put the exposed pattern in a 1:3 MIBK:IPA fresh solution for 30 seconds (only for etch pattern). Then flush with IPA for 1 minute and finally dry with the nitrogen gun. Afterwards put the waste mixture in a class 3 jug to dispose of it. The

sample is put in a vacuumed bag and filled up with nitrogen to stop oxidation from taking place. *Optional:* After we have exposed it to the electron beam, we cut up the whole into n parts, where n is the number of devices, using a diamond-tipped cutter.

Step 7. We start Oxygen plasma etching in the FND cleanroom in an ICP-RIE setup. The exposed part after EBL gets etched away leaving the Hall bar structure of crystal. The sample is put in a transition load lock box to vacuum it to a lower pressure level (to act as a transition region). Now the etching process begins according to the design; the sample is slid into the higher vacuum chamber where it starts. After etching, the vacuum chamber is evacuated and ready for the next use.

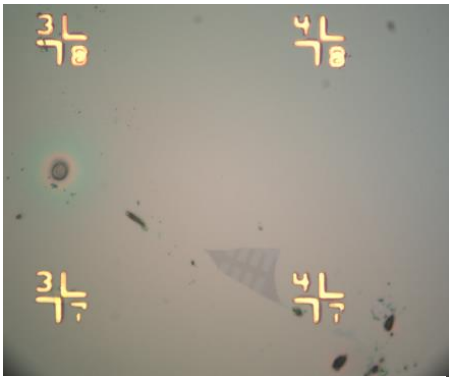

Figure 4.5 Result after EBL.

Step 8. We Lift-off the sample in Acetone at 60C° for 4 minutes, do it again in fresh acetone for 1-2 min, finally soak it in IPA for 1-2 min and then dry it with the nitrogen gun.

Step 9. Spin coating as described in Step 1.

Step 10. We check the sample under the microscope again. A clear result like Figure 4.5 should appear.

Step 11. AutoCAD design of device. The electrodes should not touch each other like in Figure 4.6

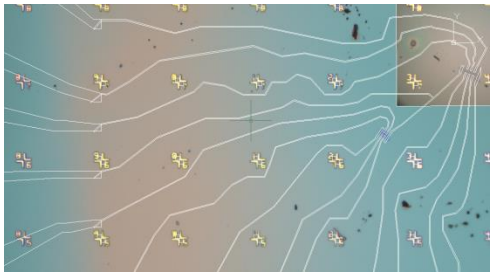

Figure 4.6 Electrode design in AutoCAD.

Step 12. E-beam lithography again, like step 5.

Step 13. Development of the sample in MIBK:IPA 1:3 ratio for 50 seconds. Then flush with IPA for 1 minute and finally dry with nitrogen gun

Step 14. We coat the sample with a metal layer. Namely Gold and Titanium. This is applied to measure the sample as these serve as electrodes. We use the TFC-2000. The recipe of the metal is Ti/Au 15/50nm (use 15/15 with closed shutter to clean the chamber).

Step 15. Lift-off sample as described in Step 8. A result like Figure 4.7 should appear. Note this figure is to show the process, a different sample is portrayed.

Figure 4.7 Result after lift-off.

Step 16. Preparing the chip carrier; we dispose of the aluminum wires from an old chip carrier and clean the now empty chip carrier using acetone.

Step 17. Finishing the sample; We rough up the surface using a diamond pen in order to let the silver paste stick better to the sample. Silver paste is unlike regular thermal paste both electrically and thermally conductive. The paste needs to dry for 10-15 minutes. Next, we use tiny pieces of glass to deposit ionic liquid onto the sample as explained in 3.3. Now we attach aluminum wires to connect the chip to the chip carrier. As aluminum is not easily oxidized like copper, hence the reason why we use this material.

Step 18. Measuring the conductivity. We put the sample into the cryostat as quickly as possible and we measure transfer curves, the resistance as a function of temperature and the 4-probe resistance while having the sample parallel to the magnetic field with increasing field strength up to 12T. The temperature can be lowered to 1.8K. The cryostat has a probe which holds the

sample. On this device, the potentiometer measures the angle and the stepper motor changes the angle of the sample. See Figure 8.5for a detailed picture. We measure the critical field temperature, which we define as the temperature where the resistance is half the normal resistance. There is no standard as many people define T_c as the temperature when the resistance is zero. The normal resistance is the resistance measured without before the drop into the superconducting regime. The pressure is to be held stable around 7mBar, but can be altered by the inlet valve to decrease or increase the temperature. We lower the power supply to let only sensor B work as this is closer to the sample. Sensor A requires more power and measures the temperature of the inlet flow.

The procedure is continued in the Results.

4.2 Process of making markers

When markers are not at hand, we need to make them from scratch. We use a mask and a silicon substrate for this. Chemicals that we use are the photoresist, the gold-titanium film and cleaning agents such as acetone. Firstly, we clean the sample by drenching it in acetone and using the ultrasonic bath to dissolve any unwanted particles into the acetone. Secondly, we pre-bake it to evaporate any potential water on top of the substrate. Next, the photoresist is spin-coated on top of the substrate and soft baked to remove any possible water again. Afterwards the spin-coated substrate is put under a UV-exposure machine, along with the photomask. The photomask has two faces, one made of quartz and the other made of chromium. The quartz face must be as close to the substrate as possible because this blocks the UV-light and avoids a diverging beam. The UV-light only destroys part of the photoresist that is exposed to it (hence not blocked by the photomask). Thus, a substrate with a patterned photoresist remains. Now, a metal coating (Au/Ti) is deposited on top by melting these metals and depositing it on top of our sample. The machine used for this rotates the metals at a material specific frequency and deposits it onto the substrate. Now lift-off happens and a pattern of metallic coating remains to form the markers.

5 CMOS versus CCD and the usage in device fabrication

We have two cameras at our disposal: the CCD camera from QSI (QSI 683) and the CMOS camera from PointGrey (Sony Pregius IMX250). Both have their advantages and disadvantages. In the device fabrication, the CMOS camera is used to obtain color images for designing the chip and the CCD camera is used for color-coding. As we can see in Figure 5.1, each CCD column has one signal output while, even though each CMOS column has one output as well, the CMOS sensor makes sure each column is measured in parallel. This avoids lag in the measurement.

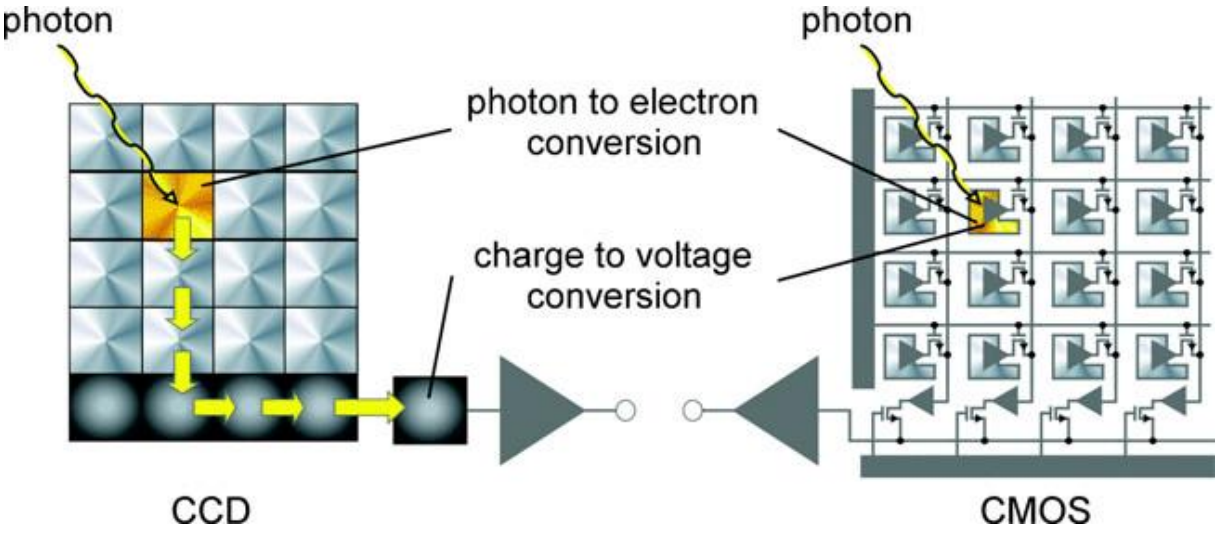

Figure 5.1 The operation of the CCD and CMOS [29].

5.1 The CMOS camera

CMOS stands for Complementary Metal Oxide Semiconductor and besides the regular workings of a MOS; the Complementary part means it has both negative and positive MOS parts.

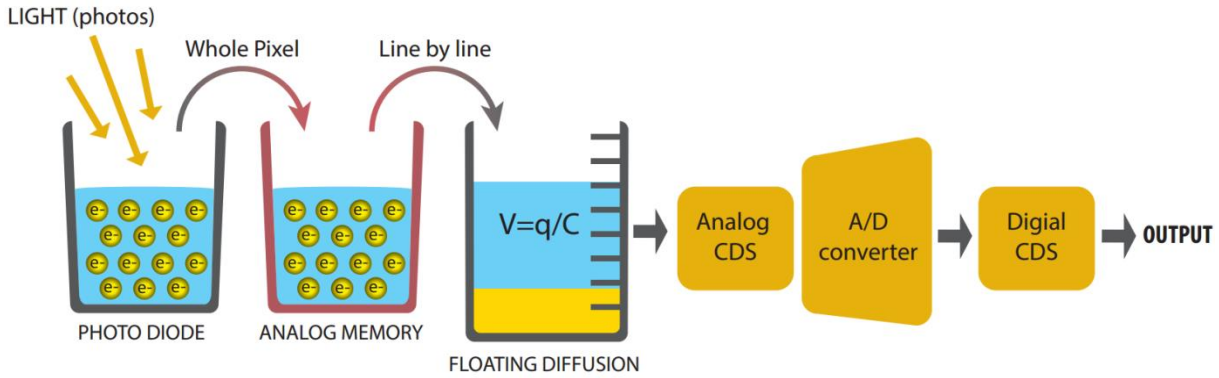

Figure 5.2 Operations of a CMOS floating diffusion measurement system [22].

The CMOS we use makes use of the floating diffusion, as in Figure 5.2. Floating diffusion, is a region in active silicon, which is electrically isolated from all other nodes. This is also called a depletion region and the voltage between the p and n side is measured. First, the light gets absorbed by the photodiode, converted into electrical charge and recorded in the analog memory. By measuring the voltage value of the incoming signal, each pixel will have its own value.

The signal, still analogue, undergoes Correlated Double Sampling. This is to measure the voltage of the pixel twice, once for incoming light after which it resets (the received light is set to 0) and then again. If the two values differ, the process undergoes a negative feedback loop.
This makes sure most of the noise is removed. Afterwards, the signal is digitized. In the end, the value of each row is measured, like in a CCD.

5.2 The CCD camera

CCD stands for Charge Coupling Device. The big difference between CMOS and CCD is that the photo sites are passive. There is no active noise-reduction or other operation. CCD sensors are double layered and transfer their charges from one layer to the next before the read out is conducted. It is almost like two sensors sandwiched together. The manufacturing process for creating this kind of sensor is very complicated and often results in a significant portion of manufactured sensors having errors, so they must be checked very carefully at the factory level. This means the CCD is more labor-intensive to fabricate.

Therefore, you may ask yourself: "If CCD sensors are four times more expensive, are significantly more complicated to work with, why would any camera maker decide to work with them?" This is because the pixels that are next to each other on CCD sensors affect each other. When one pixel overflows with energy, it affects the pixels around it. The pixels work together as a unit, much the way chemicals on a film plane do. It is believed this gives the sensor its results a more organic look.

5.3 Process of capturing images

Because the CCD camera did not give a good focus for color-coding, an alternative route was taken. The high-resolution black-white .TIFF file was therefore cast aside for the moment and we proceeded to work with the colored .PNG file.

The downside was that the binning of the data points was done in much larger stacks and the intervals therefore got wider. The upside was that, once the image was split into three channels, a better distinction can be made between the several layers as the peaks are sharper. See Figure 7.1. Before we found that the problem was due to the focusing, we thought it was due to the quantum efficiency of the two separate methods. Hence, both cameras specifications were looked up and compared, see 12.3. It appeared not to be the case; an extra blue filter was the culprit and the QSI was back in operation for color-coding again.

6 The contrast depending on thickness of the sample

As can be seen in Figure 6.1, the stronger the difference between the adjacent colors, the bigger the difference in the number of layers. There is a difference in contract because of the dielectric constant in the material *and* because of the waves interfering with another. When we use monochromatic optical light, and shine the light directly upon it from above, we cannot use Bragg´s law because that only works for light that is not perpendicular to the surface. Instead, the explanation is that the electric field is attenuated in the substance (compared to vacuum). In addition, the second reason is that the reflection intensity changes because the light reflecting from the different layers interfere with each other, thus either reinforcing the wave or attenuating it. This contrast is shown in Figure 6.1.

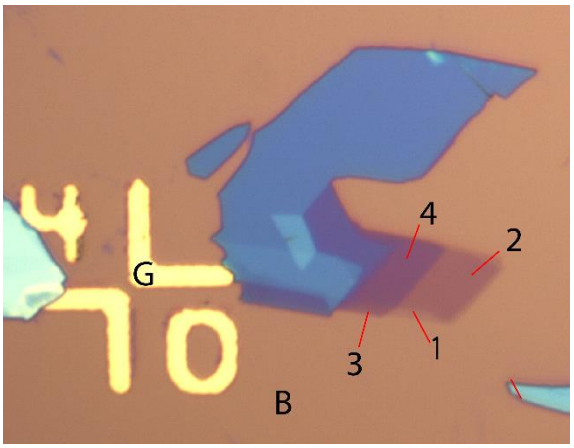

Figure 6.1 Substrate and flake. G: golden marker B: Background. 1-4: Increasing layer thickness, from light to dark.

Now the contrast is coded in for example ImageJ using RBG channel splitting to show a color. This method is called optical imaging. Optical imaging often uses the CCD method for its higher resolution. The sensors, as explained before, are on a thin silicon wafer, which is divided into an array of light sensitive areas that save data from the sample by having an electrical charge change its value as the light intensity changes too. Every small signal detected that is associated with each pixel can now be made to appear on the computer monitor.

The physics behind this is like the following: The Bayer color filters in CCD divide incident light by R, G and B wavelength ranges. These R, G and B values could reproduce a reflection spectrum from the surface of the sample. The relative wavelength range, with transmission larger than 20% of a commonly used Bayer RGB filter in a CCD, is 435nm – 520nm for the B filter, 520nm – 590nm for the G filter and 590nm – 720nm for the R filter [18]. The contrast spectrum C(λ) of the substrate can be calculated by the Fresnel equation under normal incident conditions via Equation 2.

$$C(\lambda) = \left(\frac{R_0(\lambda) - R(\lambda)}{R_0(\lambda)}\right) \text{ [31].}$$

Equation 2 Contrast spectrum

An example is show in Figure 6.2. Here, R_0 is the reflected light intensity from the air/silicon system and the $R(\lambda)$ the reflected light from the air/WS_2/silicon system. Hence, we can get the total interfering reflection. Because we are interested in distinguishing between the different layers using the CCD images, we try to find out the attenuation in each layer.

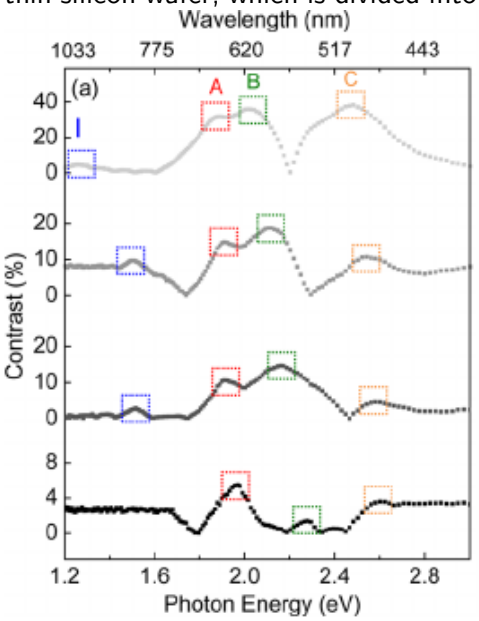

Figure 6.2 Example of contrast difference calculated using Equation 2. Bottom to top depicts a change from monolayer -> bilayer -> multilayer -> bulk. Different light energy is shone upon the sample (horizontal axis) and this shows different peaks. This can be attributed to direct and indirect bandgap transitions. The labels I, A, B, and C denote different peaks [35].

7 Determining thickness via optical microscopy attenuation

7.1 WS_2 attenuation

By measuring the peaks and their subsequent relation to the background, Figure 7.1 was obtained. The diagrams in Figure 7.1 are known as color-coding diagrams. By normalizing to the background, the intensity of the different layers could be measured. In the bottom right, the flake is portrayed showing 4+ layers. Now the area that was selected to determine the layer number is encircled in the bottom right part. The layer numbers are shown in the top right. As the green-channel for the CMOS camera was used to color-code, the x-axis of the bottom-left graph shows the pixel counts versus the green channel counts. For the QSI capture, the red channel was found to be better to distinguish than any other was so this is added as a comparison. Note that it is easier to distinguish peaks using the CMOS camera, the downside is that the resolution of that camera is lower. The layer numbers here are not the actual layers as this can only be determined statistically by taking many different samples like in Table 1 *WS2* attenuation.

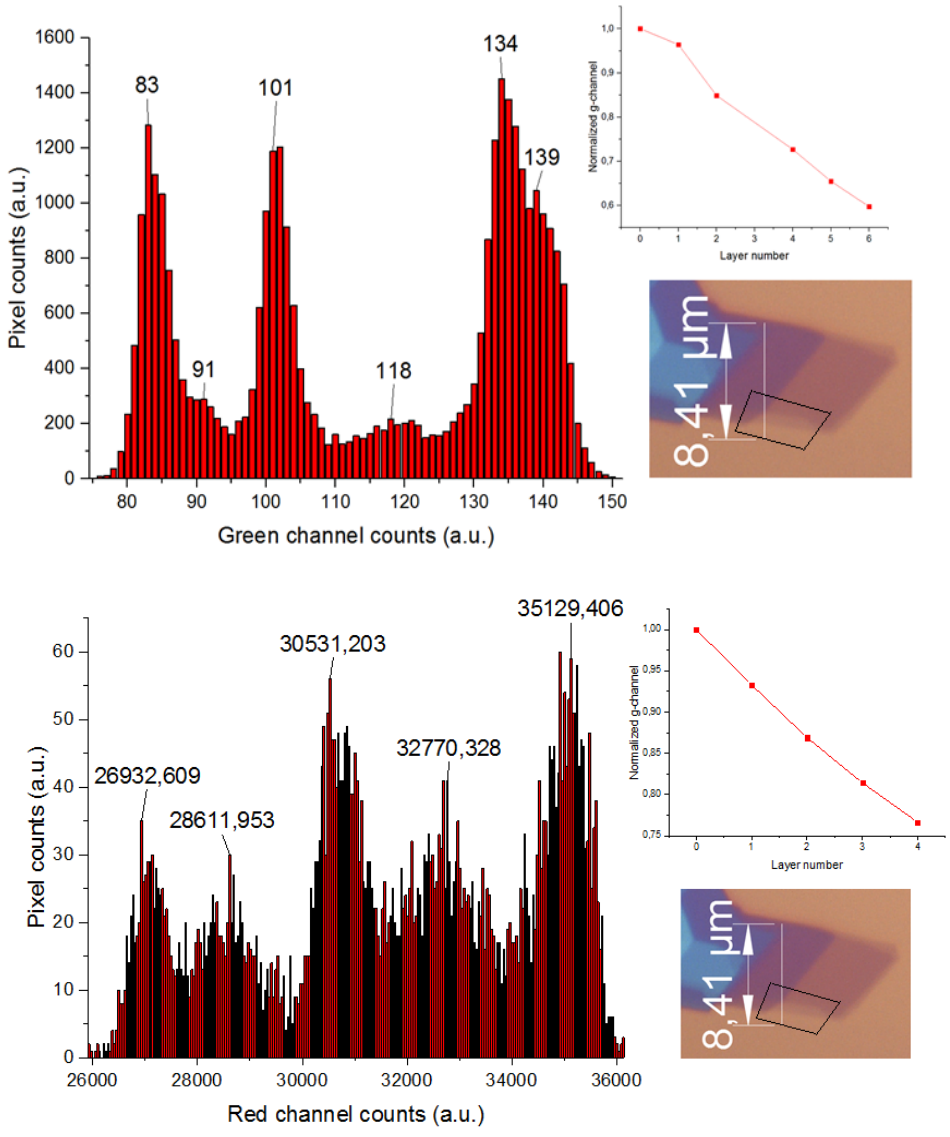

Figure 7.1 CMOS (above) and QSI (below) color-coding for two different channels.

7.2 Attenuation in WS_2; summary

In Table 1, we see the different samples their attenuation summarized in one graph. The linear relation was drawn along with a supposed attenuation coefficient of 8% per layer. Several lines were drawn with the QSI camera, and without (only using the PointGrey and splitting channels). The Wj10 samples were grown bottom-up via the Chemical vapor deposition technique. The large variation distribution in some layers can be attributed to the thickness difference of the substrate. By comparing the photoluminescence pictures of the different samples, we can however say that these are indeed belonging to that layer. An attenuation of about 6% per layer was found.

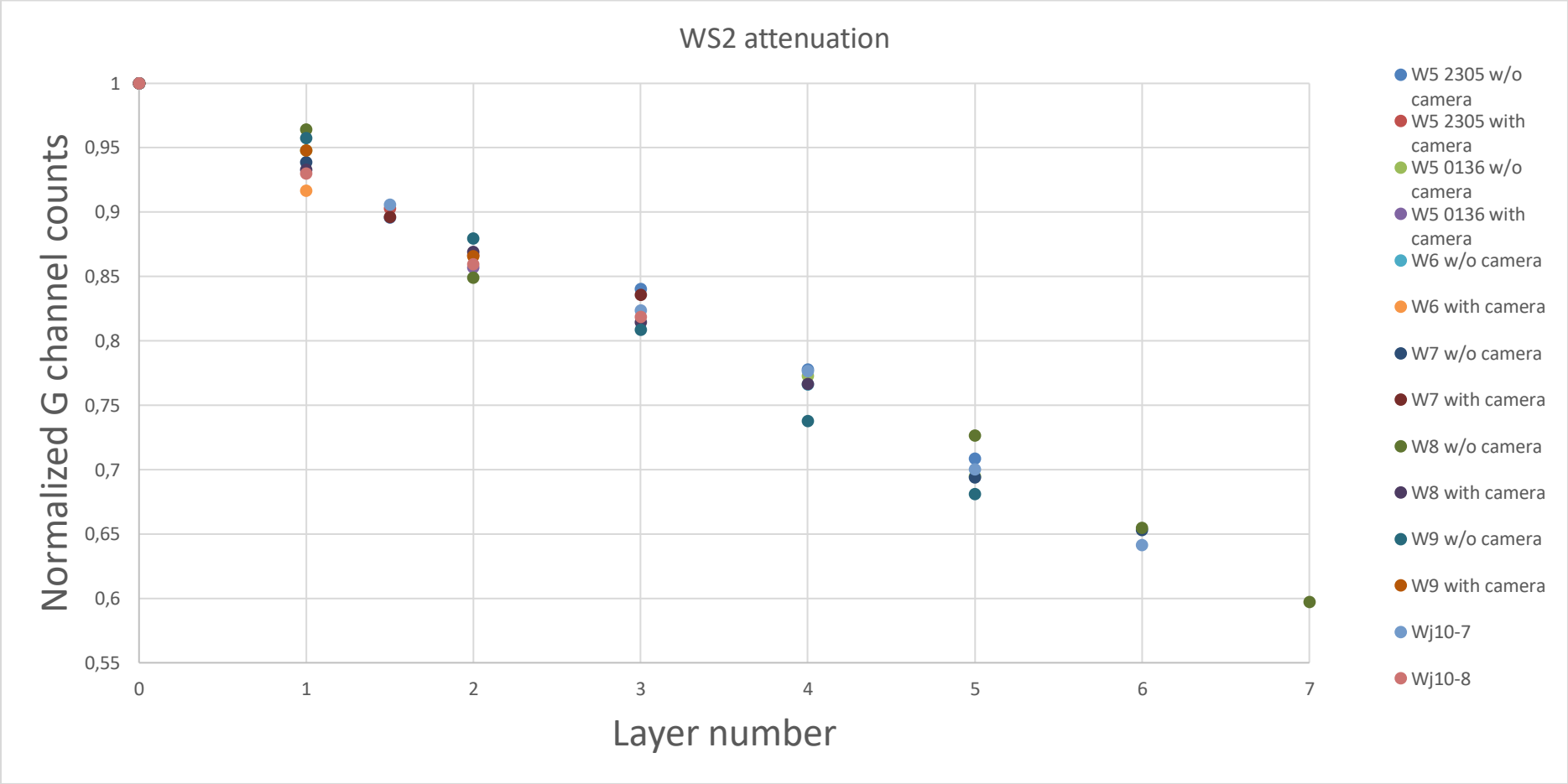

Table 1 WS_2 attenuation.

7.3 Red versus green filter attenuation in WS_2

In determining the thickness-attenuation relationship, it was found that the red filter gives sharper images for the bigger flakes than the green image in WS_2. This can be explained by the fact that red light has a longer wavelength than green and resolves smaller features not as good as bigger ones. Hence, the features go below the wavelength, the image gets blurry. Therefore, the green filter is better for smaller sized flakes. However, we primarily use the red filter as we want bigger flakes because it is easier to apply electrodes to. The flakes, which are easiest to apply electrodes to, are primarily in that size regime where the red filter gives the sharpest image. In Figure 7.2 is a comparison of the color-coding of three different samples taken with the red and green filter to show if there is a trend line.

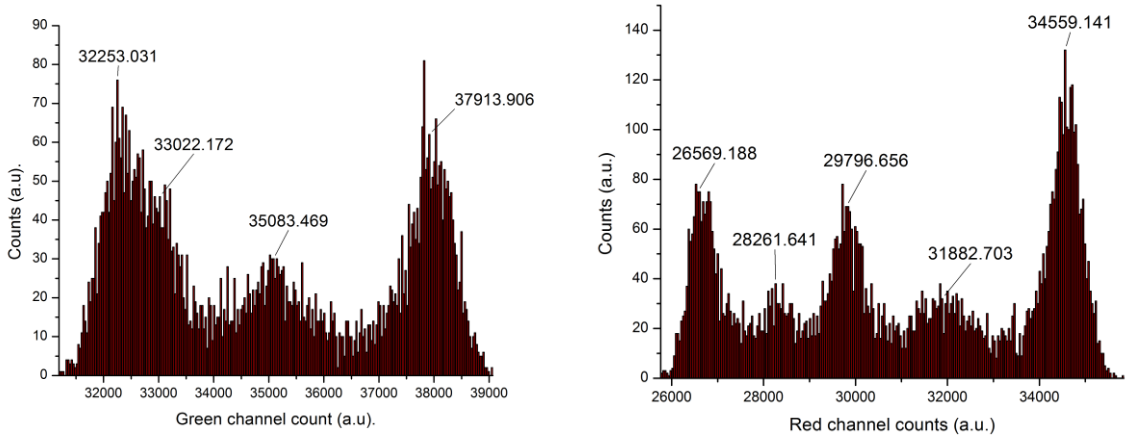

Figure 7.2 W8-3140 1-second exposure time. Different peak distinguishability for two different filters.

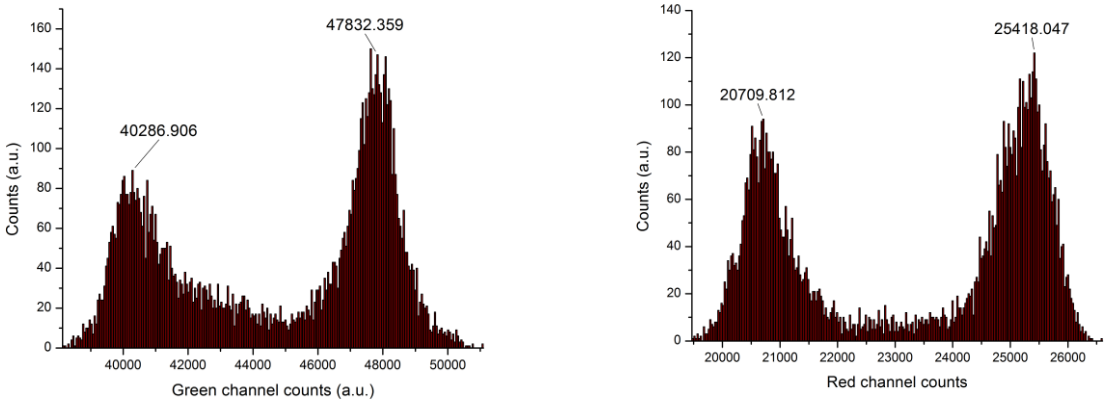

Figure 7.3 W6-0385 2-second exposure time. Different peak distinguishability for two different filters.

7.4 BSCCO, the road to device making

$BSCCO$, a very interesting material, is also tested for superconductivity. No one knows if it is a superconductor as a monolayer and this is uncharted territory in the semiconductor world. Below, the procedure is listed how we are planning to find out if it truly is a superconductor on the monolayer scale.

We first obtain the wafer after which we clean the surface with plasma etching again. After similar preparation steps in the scotch tape method, we move to the glove box and use the sharp shaving blade to cut the sample. There are two vacuum chambers at our disposal; the modern one is used for cleaving and the other one used for spin coating. A vacuumed cylinder is used to transfer the sample from one to the other. Before this transfer takes place, we have to prepare the old vacuum chamber by purifying the atmosphere within. We do this by trapping the impurities that exit the chamber inside a copper rod. The copper rod is cooled in liquid nitrogen so that the impurities that pass through the tube freeze and turn into solid. Afterwards, the rod is taken out of the liquid nitrogen and heated. The oxygen vaporizes and is spread into the outer atmosphere. This is done five times to make sure the full volume of the box is passed through the "filter", especially after a long time of neglect. Once the rubber gloves start to fill up, we know the volume flow rate at the inlet is higher than the outlet. The outlet takes out the gas with the same volume flow rate, at the beginning of the sequence, but this decreases because there will be fewer impurities in the vacuum chamber.

The more modern chamber uses copper-oxidation as the process of purifying but this is slower than the method mentioned above. It was decided that we let a continuous flow of helium pass through the chamber in order to clean more time efficiently.

After having cleaved the sample, we spin-coat it with PMMA in the vacuum chamber filled with helium. Next, we fill up the transfer tube with argon from the modern vacuum chamber and take pictures to determine color-coding and find out big enough flakes to measure the conductivity. B-6 is especially good for applying electrodes as the flakes are huge.

Even though we knew that $BSCCO$ decays rapidly in an oxygen environment, the measurement showed a high resistance. Culprits could be the PMMA that does not spread well in the helium environment, thus oxygen penetrates the PMMA. By applying a 2-probe measurement, we found that the resistance was 30kΩ for a sample of T_C=91K.
The solution to this was change the method of measurement and make sure there is no transition whenever to oxygen. We do this by altering the vacuum chamber and probe and cleaving the $BSCCO$ from the crystal straight onto the marked wafer into an argon environment. The problem is that we have to be lucky that a flake moves right on top of the electrodes. Another problem that we have to overcome is the leakage current through the $SiO2$. A remedy of this is found and put in Sample transfer.

7.5 Attenuation BSCCO; summary

The same procedure was applied to our $BSCCO$ sample. An attenuation coefficient of about 5% per layer was found. The method uses was the same one applied to WS_2, this works well for the first few layers but later it levels off to a steady attenuation as the layers grow.

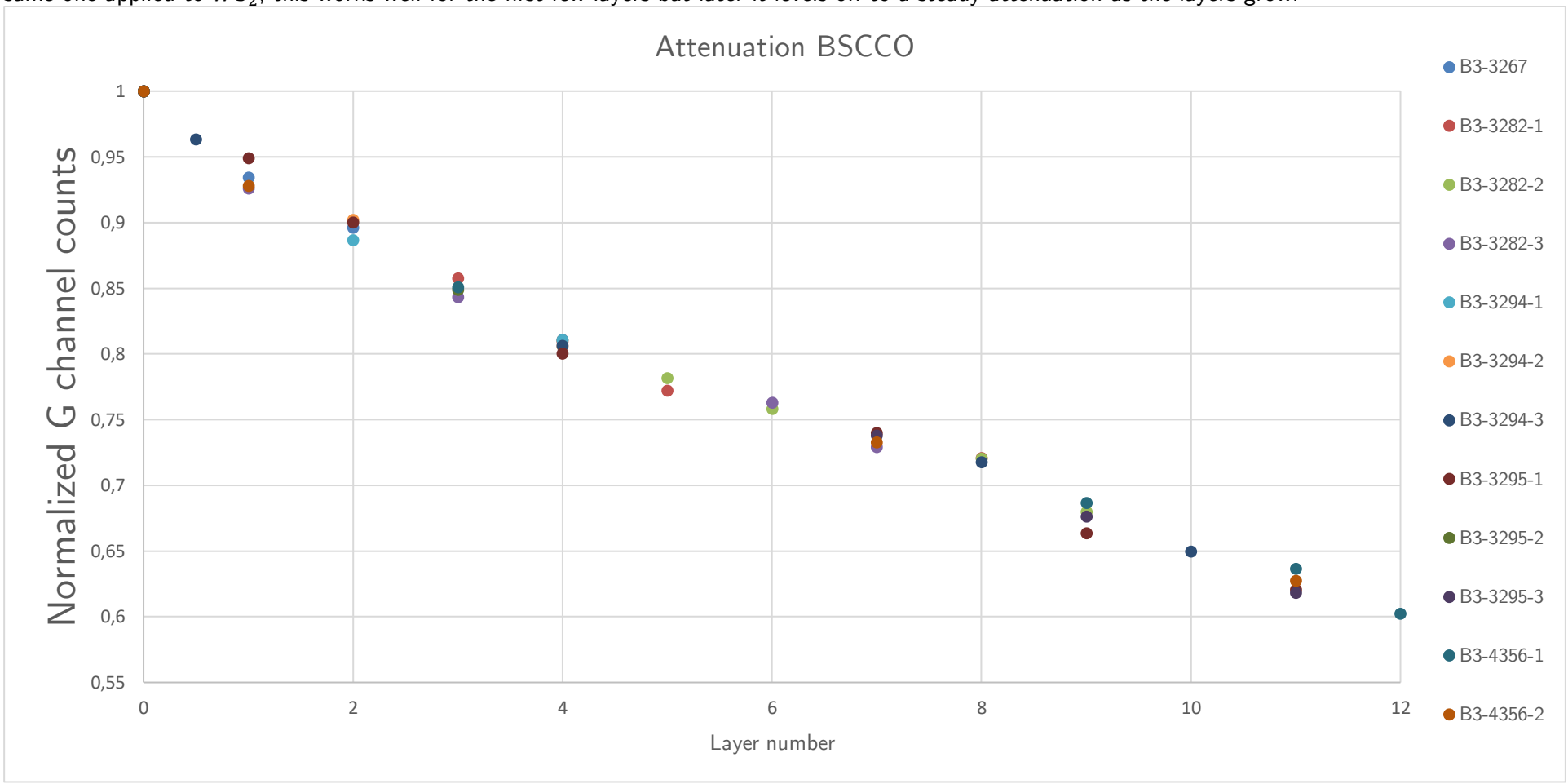

Table 2 BSCCO Attenuation.

8 Equipment

Figure 8.1 EBL machine with the EBL software on the desktop.

Figure 8.2 Metal depositing machine with console to control procedure.

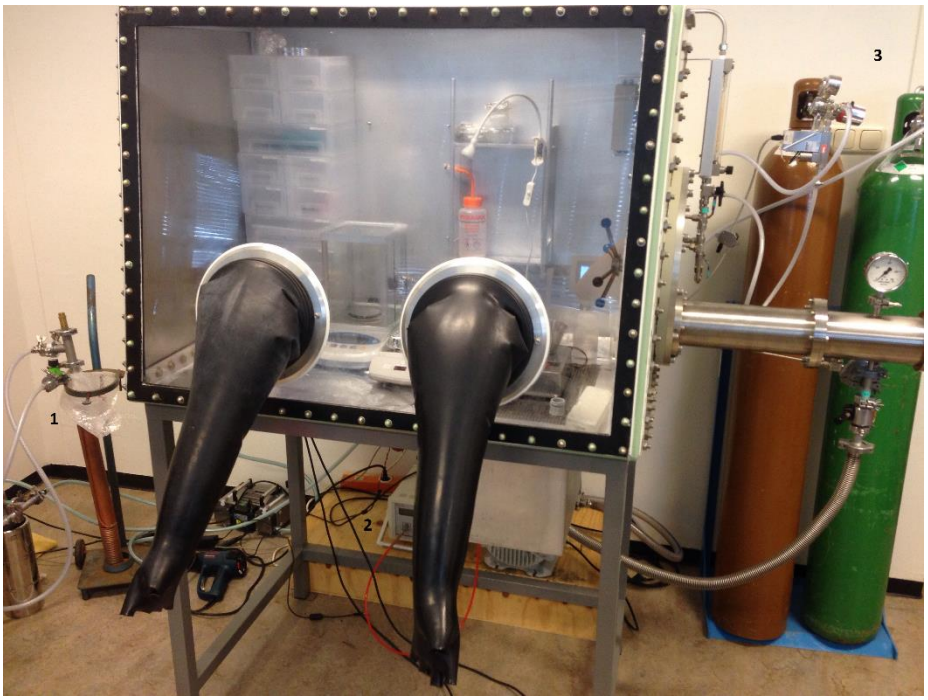

Figure 8.3 Glove box with charcoal filter copper tube 1. Oxygen PPM meter 2. Helium and argon tanks 3. The tank is regenerated by the oxygen particles being trapped by the charcoal. Once saturated, one manually needs to thaw the frost in the trap, which releases the oxygen to the outer atmosphere. Although more labour-intensive, this is faster than the copper filtration method.

Figure 8.4 Glove box with copper filtration. The copper is used to remove oxygen; this oxygen pipe is regenerated by passing a hydrogen/nitrogen mixture through it while it is heated: the water formed is passed out of the box with the excess hydrogen and nitrogen.

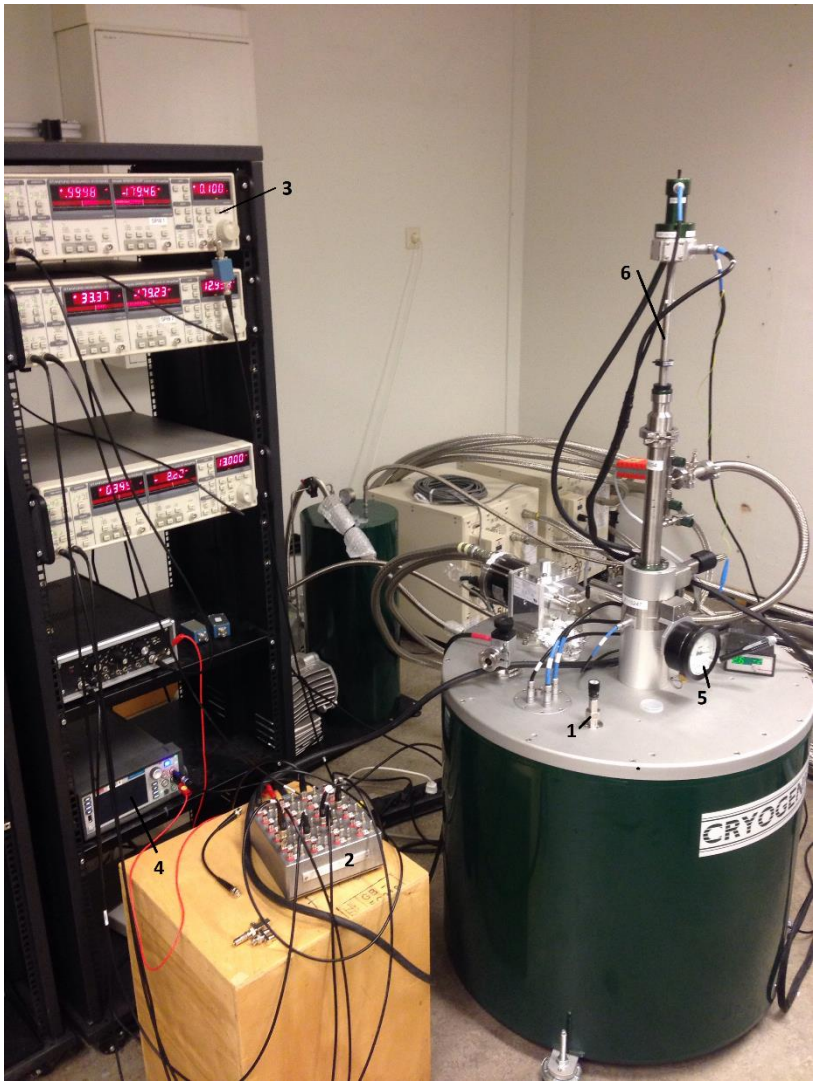

Figure 8.5 1. The inlet valve in order to cool the cryostat. 2. The controller that measures voltage, current and feeds data to the lock in amplifier. 3. AC-current lock in amplifiers. Normally 3 in current set up. This is used to voltage and feed a source drain current. 4. DC-current box used to put potential on the gate. 5. Pressure gauge. 6. Probe with sample at the bottom inside the Cryogen vat.

Figure 8.6 Cutting machine to cut wafer. The tip is made of diamond.

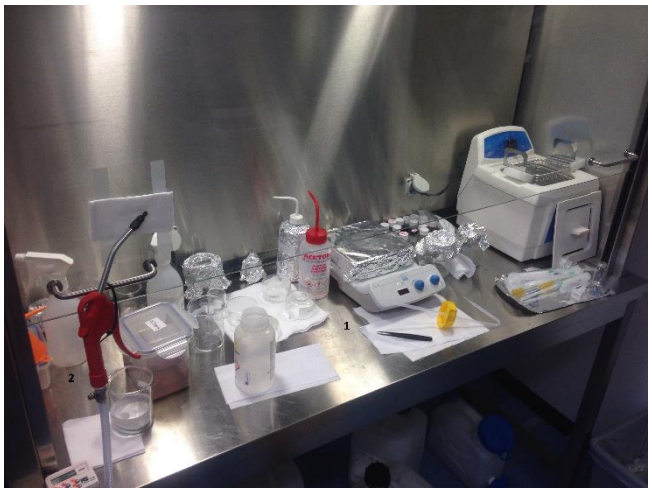

Figure 8.7 Workbench with: 1. Nitrogen blowtorch 2. Baking machine.

Figure 8.8 1. Spin coating machine. 2. PMMA used to spin coat frequently. 3. Gloves for hygiene/safety.

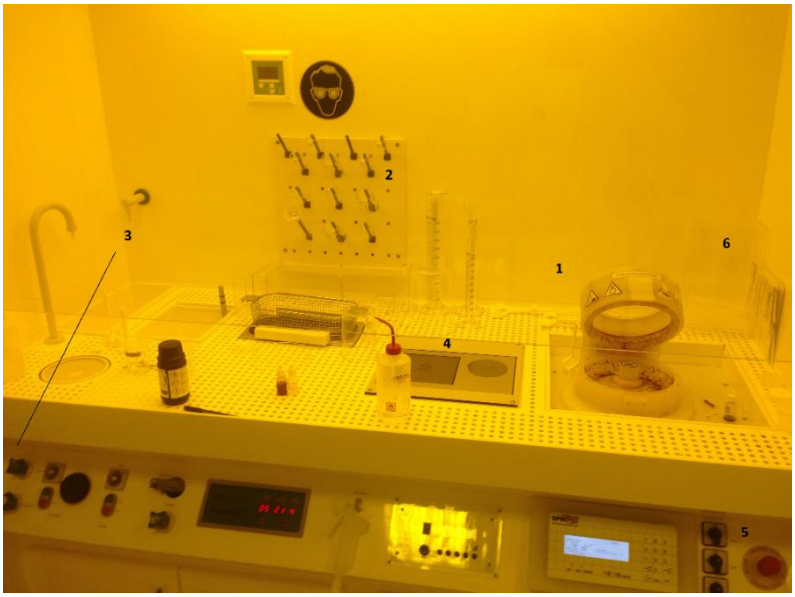

Figure 8.9 1. Spin coating machine 2. Board with several beakers for use 3. Tap for mineral water to clean equipment 4. Baking device 5. Power switch + safety glass drop switch 6. Pipettes

9 Measurements steps

After going through all the Fabrication steps, we test the sample for superconductivity. We are interested in several parameters:

1. The transfer curve.
2. The resistance-temperature relationship.
3. Angular dependence, find out the parallel angle for different B_{ext}.
4. The resistance-temperature relationship for the perpendicular angle.
5. Hall Resistance-B field relationships for the perpendicular angle.
6. The carrier density extracted from parameter 4.
7. The Hall mobility for each superconducting state

1. Firstly, we want to find out the transfer curve of the different contacts of the sample when a gate voltage is applied. All resistances on the sample are measured, that is the contact resistance, 4-probe resistance and source drain resistance. Their relation with one another is

$$Contact\ resistance = \frac{Source\text{-}drain\ resistance + 4\text{-}probe\ resistance}{2}$$

Here the 4-probe resistance is the resistance between the connections except the source drain connection. If all these electrodes have the same distance between them, it will simply be a multiplication of one connection channel resistance. The factor 2 comes from the number of contacts. The contact resistance is used to determine if the sample is dirty, if it is higher than other readings we know something is amiss. It is higher for a lower voltage as then the Schottky barrier is "harder" to pass through. The physical process of charge carriers being able to "pass" through the channel is explained in Schottky-barrier and energy diagrams.

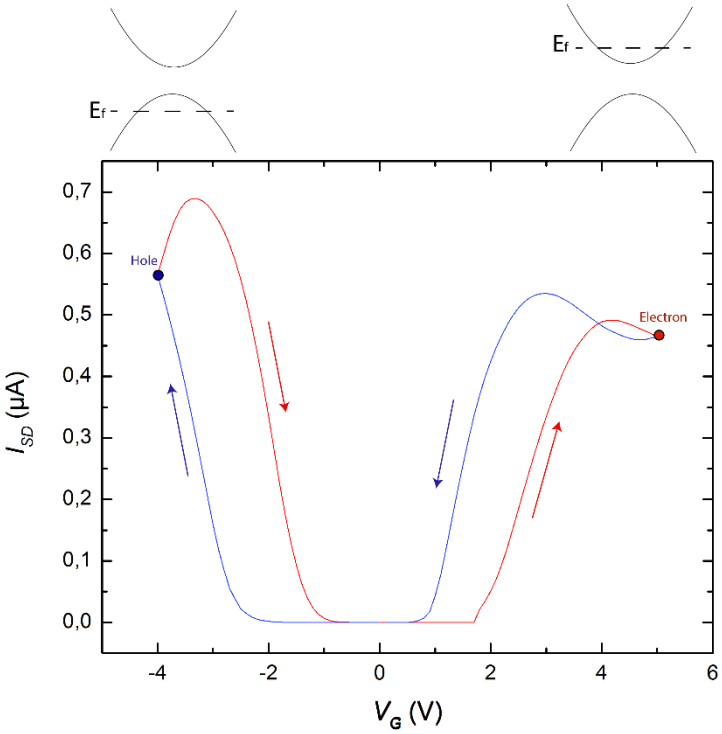

Figure 9.1 Transfer curve for 4-layered WS_2 with illustrative band diagram where E_f is the Fermi level.

In Figure 9.1 we see a forward and backward scan. This hysteresis can be explained by ions having to pick up speed. The source drain voltage is set to 0.1V and the source-drain resistance can be determined by using Ohm's law. LabVIEW already lists the 4-probe resistance and it is 4.5kΩ for the maximum V_G of 4.25V. The source drain resistance is $\frac{0.1\text{V}}{5\mu\text{A}} = 20\text{k}\Omega$. Thus, the contact resistance is $\frac{20k\Omega + 4.5k\Omega}{2} = 12.25\text{k}\Omega$. As seen in Figure 9.1, the source-drain current increases. This is due to the ions forming an EDL. At around 4.25V this increase dozes off again. Another thing to mention is that we are plotting data for anything but monolayer; hence, there is no longer any ionic trapping. Ionic trapping happens in a monolayer due to a strong V_{eff} that pushes the electron toward the ionic liquid charge center and Coulomb traps it in a lower potential well. The effect in the monolayer case would be that the ions reduce the conductivity

under a higher gate voltage similarly to Figure 9.1. In bulk layers, this effect is weaker but still happens as one can see.

2. Now, the resistance-temperature relationship is to be found out. We apply a gate-voltage, which is the highest gate-voltage from the transfer-curve measurement, and slowly decrease the temperature to the base temperature of 1.8K. An S-shaped curve follows from the resistance versus temperature plot. At low temperatures, the resistance is negligible until a temperature high enough is reached to break the Cooper pairing and the resistance increases enormously. When the temperature increases further, the resistance levels off again. Half of the normal resistance is what we define as T_c, the critical temperature, and we use this for our next measurement. The T_c in Figure 9.2 is at about 2.98K. The black curve is for a negative voltage, meaning the dominant mobility is of holes. The charge carrier density is too low in this case and this causes no jump to superconductivity; the holes are not near enough each other to form Cooper pairs. We will also need this data later to find out the carrier density versus T_C relationship.

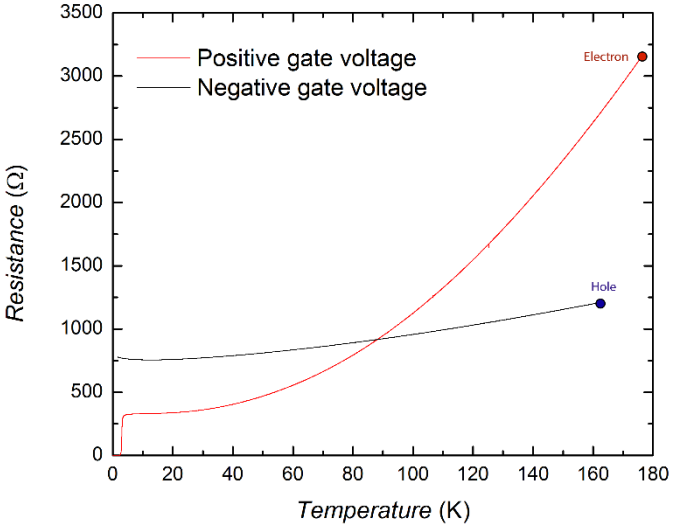

Figure 9.2 *R(T)* curve showing a non-zero T_c for the superconducting regime (red) and a zero T_c for a negative gate voltage (black).

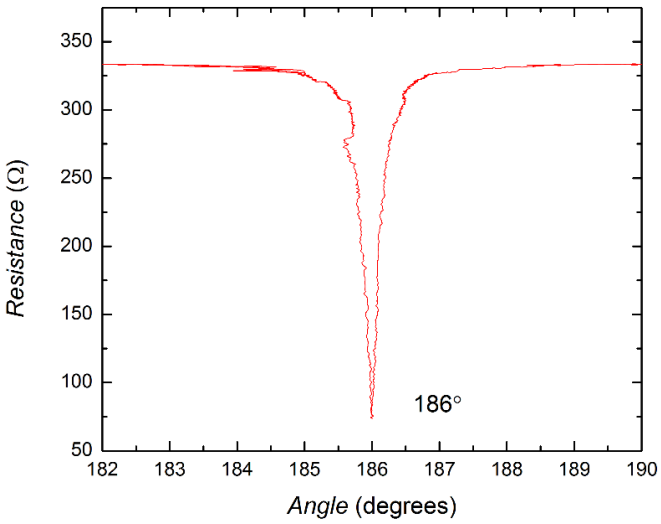

Figure 9.3 Finding out the parallel angle.

3. The angle where our sample is parallel to B_{ext} is needed for our next experiment so we shall determine that now. We fix the temperature at T_c and vary the angle using the stepper motor. By applying a high magnetic field of 12T, the lowest resistance should be most obvious. The lowest point of the resulting plot is where our sample is parallel to the magnetic field. We want our sample to be parallel to the field because then the Zeeman-effect inhibits the Cooper-pair breaking. If it were perpendicular, the Zeeman energy would actually contribute to Cooper-pair breaking. We see that the angle where the magnetic field is parallel to the sample is 186°.

4. Now we repeat step two but for the perpendicular angle to measure this critical temperature depending on B_{ext}.

5. We measure the Hall resistance R_{xy} now. We perform a parametric sweep by changing T. In addition, the R_{xx} resistance is measured. The R_{xx} resistance clearly shows at what magnetic field the superconductivity stops.

6. This resistance can tell us the charge carrier mobility by applying $n_{2d} = \frac{B_{ext}}{eR_H}$.

The remainder of the steps are shown in Results.

9.1 Results

We apply the measurements steps to the sample for different gate voltages applied. The results for the 4-layered sample for step 5 are shown in Figure 9.4.

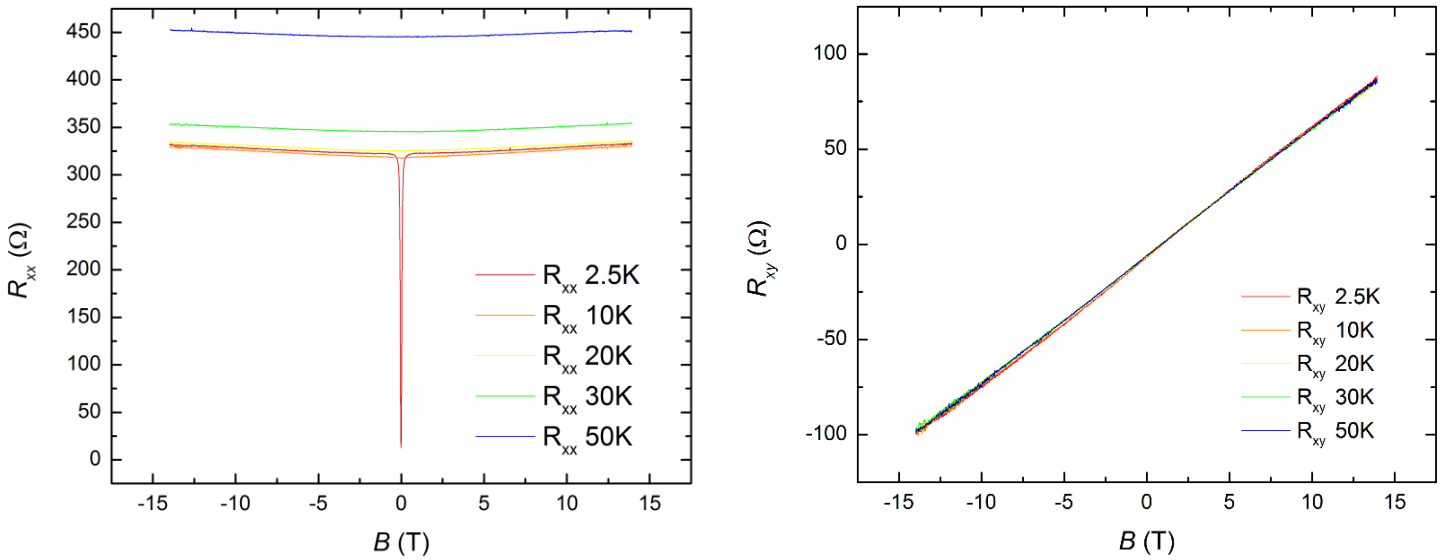

Figure 9.4 Graphs for R_{xx} and R_{xy}.

Figure 9.4 shows a resistance breakdown for 2.5K at a magnetic field strength close to zero. From here, we can determine the critical current via $I_c = \frac{2\pi R B_c}{\mu_0}$ [5] where μ_0 is the magnetic permeability of free space. The right graph is used to extrapolate the carrier density as in step 6. This is down in Figure 9.5. The different colors depict a different V_g.

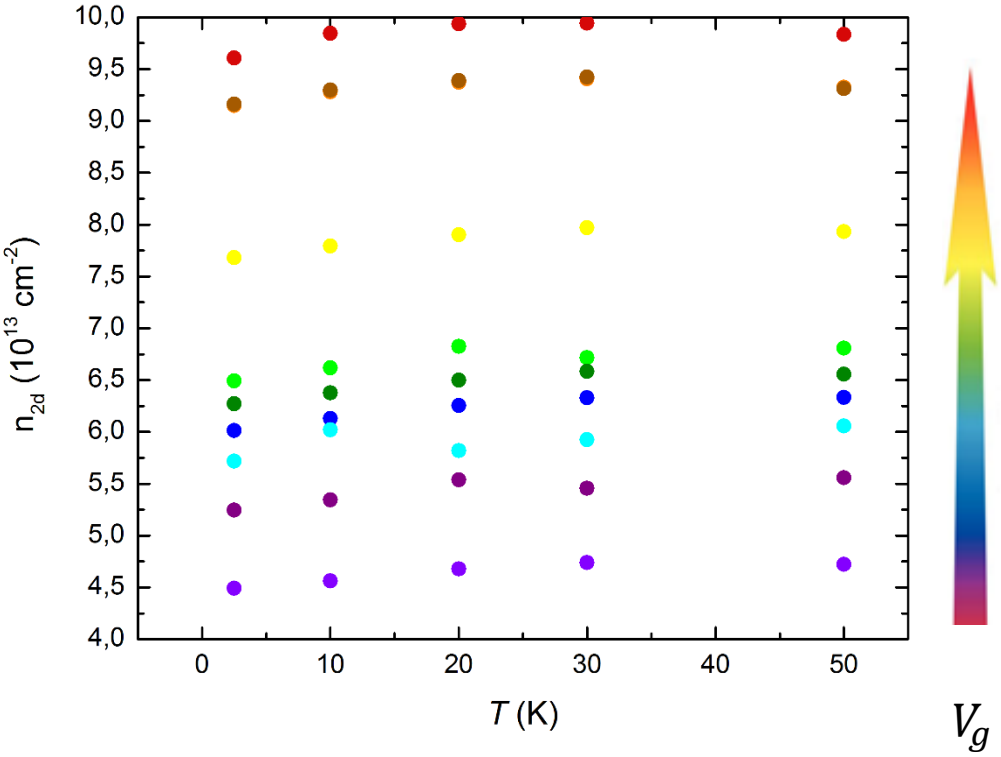

Figure 9.5 This shows that the carrier density increases but has a maximum around 30K.

In Figure 9.5, the carrier density stays relatively the same because we have entered the metallic regime for these temperatures. The colors depict different gate voltages, for higher gate voltages we see a higher carrier density as more ions are pushed towards the EDL.

As one can tell, the different colors in Figure 9.6 depict a different carrier density. An increase in temperature causes an increase in resistance for each carrier density. This is because the Cooper Pairs are broken. It takes more energy for a higher charge density to break the superfluid, as there are more Cooper Pairs leading to a higher T_c.This explains the shifting of the data for different carrier densities.

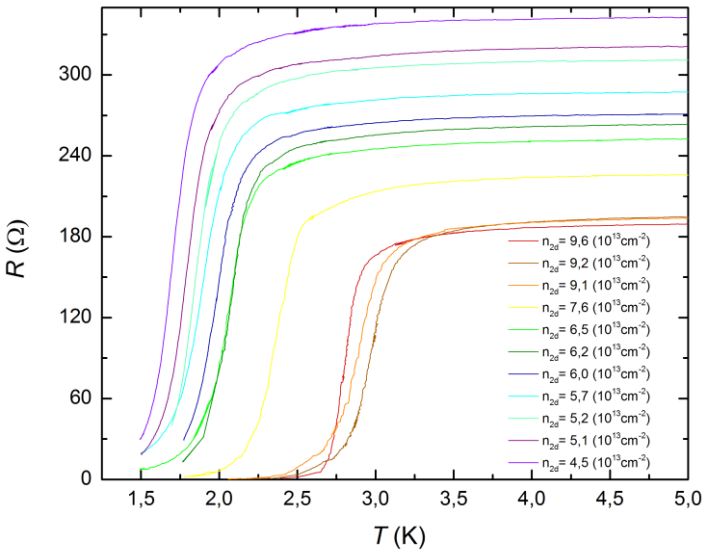

Figure 9.6 Temperature-resistance relationship for different carrier densities.

Another measurement we need to do is to find out how the T_c varies for each magnetic field. This is shown in Figure 9.7. The two graphs depict a different gate voltage. The left one has a higher V_g and the right one a lower V_g.

As one can tell, there is a higher resistance for a larger magnetic field. This is because of several effects mentioned in Physics of superconductivity. Also, the T_c rises for a higher V_g.

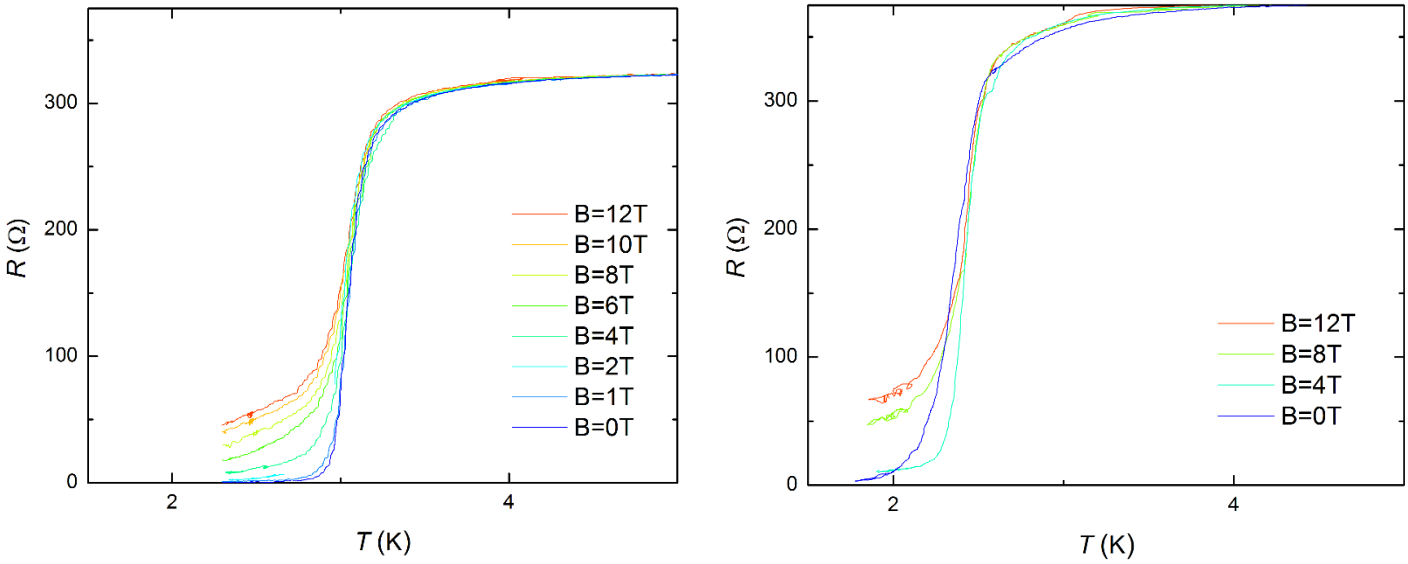

Figure 9.7 The result of T_c versus B_{c2} for different V_g

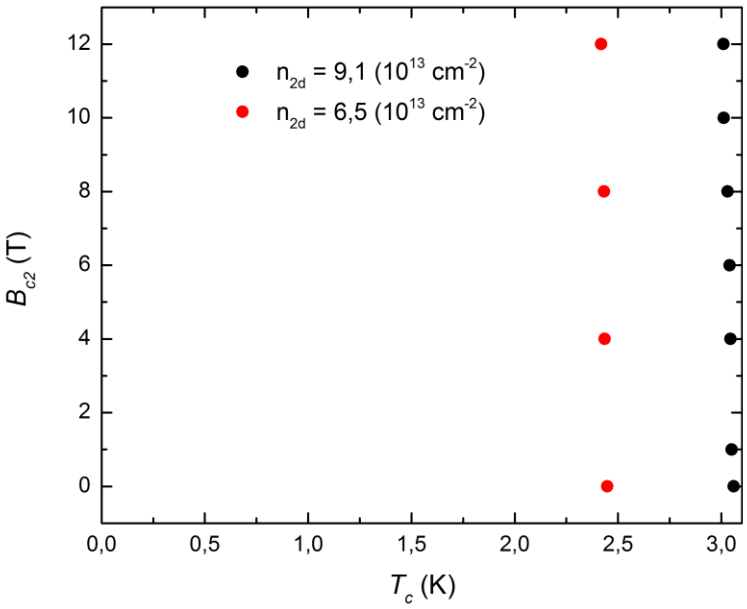

Figure 9.8 Two different carrier densities showing a different upper critical field for several temperatures measured.

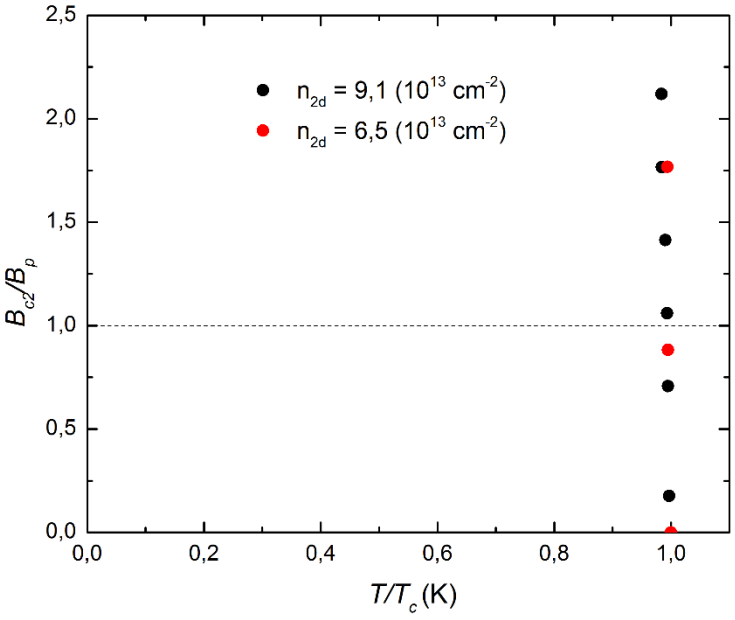

Figure 9.9 Normalized values where B_p is the Pauli Limit and T_c the critical temperature for $B_{ext} = 0$.

In Figure 9.8 we see a linear relationship between B_{c2} and T_c. The upper critical magnetic field does not affect the critical temperature. We can also normalize the values to show when our data is in the Pauli limited regime. This happens below the dashed line. Above, we have exceeded the limit and this can be attributed to scenario B in Figure 2.6.

Now we need to correct for the dimensions for which the measured the resistance. We do this by taking into account the square resistance $\rho_{\blacksquare} = R \cdot A$ where A is the aspect ratio of the part the current flows through between electrodes. By measuring this in AutoCAD as in Figure 9.10 we obtain $A = \frac{W}{L} = 0.6$. Another interesting measurement is the Hall mobility; a measure of the mobility of the electrons or holes in a semiconductor. We do this by measuring $\rho_{\blacksquare}$ at 10K and applying $\frac{1}{\rho_{\blacksquare}} = \sigma_{\blacksquare} = n_{2d} e \mu$ leading to $\mu = 1/\rho_{\blacksquare} n_{2d} e$ where μ is the electron mobility, n_{2d} the carrier density, σ the conductivity and e the charge of the electron. The temperature is 10K because we need a stable region without superconductivity. This gives us Figure 9.11.

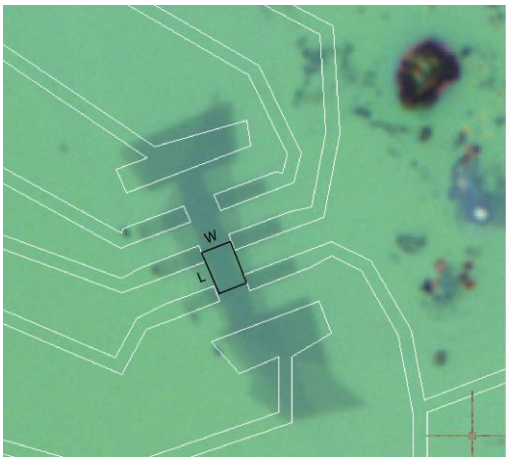

Figure 9.10 Dimensions for square resistance

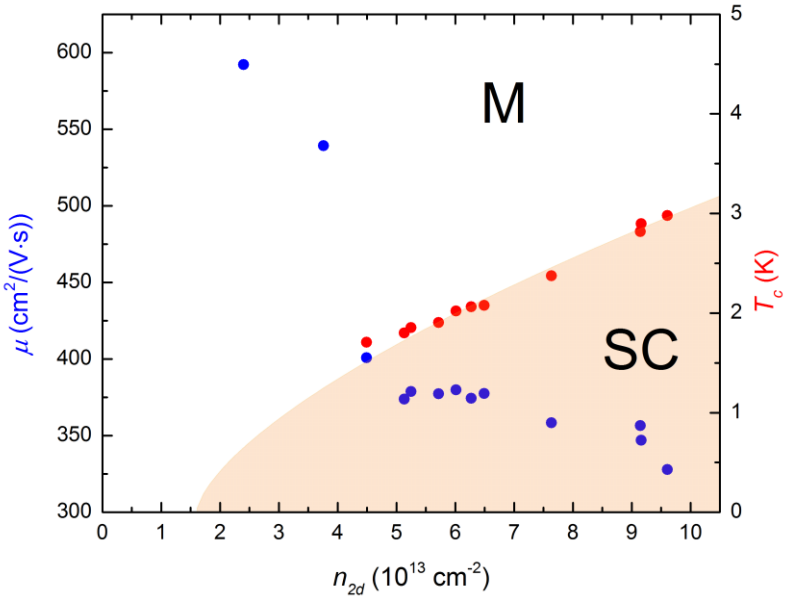

Figure 9.11 Electron mobility μ and T_c versus carrier density n_{2d}. SC and M denote the superconducting and metallic regimes, respectively.

This shows that there is an increase in electron mobility as the carrier density decreases. Consequently, one can conclude we enter the metallic regime. T_c scales with ${n_{2d}}^{2/3}$ and this is called scaling theory [19].

We can repeat the above measurements for different layers and find out if the material properties change significantly. In the end, a phase diagram for all the layers can be made to show a transition from different regimes (e.g. superconducting, metallic) for different carrier densities.

10 Conclusion

After numerous experimental procedures, many data were obtained and analyzed. The results listed below for the reader's convenience.

- WS_2 showed a transfer curve that seems to drop beyond a certain voltage point. A cause could be that there is ionic trapping, albeit weak.
- A weak magnetic field breaks the superconductivity at a temperature of 2.5K.
- A higher gate voltage resulted in a higher charge carrier density. This led to an increase in T_c. The cause was a higher energy need to break the superfluid state.
- Upon changing the T, there was no change in n_{2d} when in the metallic regime.
- Superconductivity in 4-L WS_2 was found in the electron-doped regime.
- Even more so, it was found that the transition from a superconducting to a metallic regime happens for a lower charge carrier density.
- By cleverly avoiding the orbital limit, by applying a magnetic field parallel to the sample, and using ionic liquid the Pauli limit was exceeded. As mentioned before, the Rashba-effect protects the Cooper pair from breaking in the top layer as this is the only superconductive layer.
- Finally, the superconducting dome was mapped and follows the scaling theory. There are two curious points that fall high in the metallic regime, which can be investigated further.

There are still many things to be researched such as bi- and triple layers and to find out interesting properties that could lead to vastly different results. We leave that chapter open but the key thought is that there are many more materials and device techniques to be studied. Perhaps you are one of the researchers who will find out more?

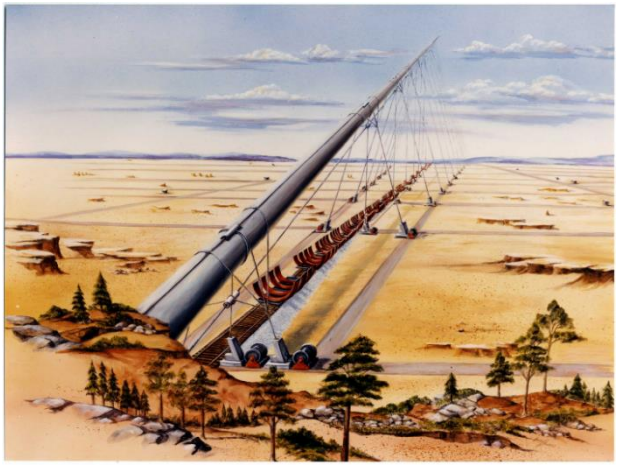

Figure 10.1 The StarTram, realizing low-orbit launches in a cheap way. Finding HTSCs would be ideal for this application.

10.1 Acknowledgements

I would like to thank especially my supervisor, Sasha Zheliuk for his effort and inspiration to be a curious, hardworking scientist. In addition, Justin Ye as second supervisor was always an enthusiastic help, creating a nice atmosphere in the group.

For the rest, I would like to thank all members of the Device Physics of Complex Materials group for their help in this thesis. These were Chunrui Han, Jie Yang, Qihong Chen, Ali A. El Yumin, Lei Liang and Puhua Wan.

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12 Appendix

12.1 EBL procedure

Loading the sample

1: Start StartSEM

2: Insert the sample into the machine and select the patterns that were designed in AutoCAD

3: Vacuum the load-lock chamber to $2*10^{-5}$ mbar in SEM control>Pump

4: In the software, click load lock> load sample > reset coordinates > name your sample e.g. "etch1".

5: We need to position the EBL above the faraday cup so go to Adjustments > Stage Control > Faraday Cup > Go. (Alternative way: go to Z=25 first, then go to Faraday cup)

The faraday cup measures the current from the electron beam and based upon that decides the electron beam "dosage" needed.

6: Reduced Raster>Magnification Focus>Beam open. Zoom in until Faraday cup completely disappears, then press measure.

7: Patterning parameter>measure. Now click the calculator icon. For small and large structure, pick a step size of 0.015µm and 0.040µm respectively. Under "enhance parameter" go to settings and click auto.

E-beam Adjustments

Small structure

E.1: Sem Control>AutoBC off, adjust brightness

E.2: Write field alignment: find an impurity and go to its edge

E.3 Select 30KeV electron beam energy. This will give an area doze of 640µC/cm^2

E.4: Open position list>scan manager>write field-alignment>manual> 120µm write field>select 10µm and 1µm markers>scan selection

E.5: Put it back at the impurity position 4 times. Check stigmation to avoid Fresnel fringes.

Build coordinate system

Find a marker and after having a marker centered in your screen:

C.1: New image window>scan image>P1=origin=centered of marker>drag marker to center and check box.

C.2: Find the next marker far away in the x-direction and do the same

C.3: Repeat for the vertical direction.

C.4: Click adjust.

Before exposure steps

C.5: Stage control>put in coordinate (x-150,y-150)>open small window. Here LMB is magnification and RMB changes the focus.

From the G2S2 database design: Select patterns>select write field>small marker>delete empty write fields. For the coordinates, type in the numbers found in the notebook (these are the coordinates found using the optical microscope>scan selection (this step should be done in e-beam design software)

C.6: Now before exposure go to position properties in position list
C.7: Adjust the markers as done before. Click expose.
Large structures
Sem Control>AutoBC off, adjust brightness
Select 10KeV electron beam energy. This will give an area dose of 240μC/cm^2.
Write field alignment: find an impurity and go to its edge
In Open position list>scan manager>write field-alignment>manual> select a 600μm write field > select the 50μm and 5μm markers>scan selection. Adjust the marker 4 times again.
Repeat steps C.1 until C.7

12.2 Metal coating procedure

For cleaning:
Pump in auto menu
Close shutter to clean the chamber
Find recipe => select => check recipe
Switch on the ion gun power supply
Recipe => start recipe
System map => thickness 15/15
Check frequency 20/50Hz. 1Å/s. Not any higher to avoid PMMA from melting.
Write down pressure and power use percentage.

For depositing:
Titanium: -open shutter from 0.140kÅ to 0.145Å as this gives a deposition of 0.005Å
Gold: -open shutter when 1Å/s current is reached. It closes automatically at 5kÅ.

Wait 2 minutes to cool down the source material, the ion gun and the sample.
Switch off the power supply.

12.3 QSI and CMOS quantum efficiency

In trying to find out the problem why we got blurry images, the quantum efficiencies of both cameras we used were sought out. This was because we got better-focused images from the CMOS. The quantum efficiency is defined as the incident photon to converted electron ratio. We notice a higher quantum efficiency for the CMOS camera but we used the CCD camera due to the higher-resolution.

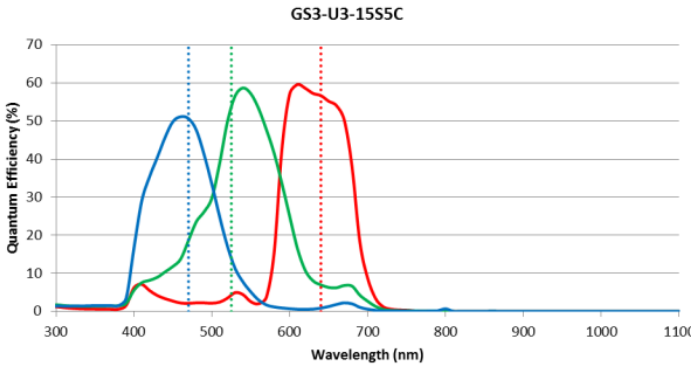

Figure 12.1 CMOS quantum efficiency [21]

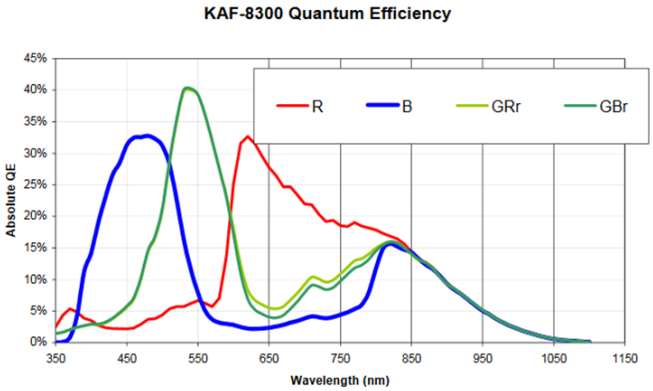

Figure 12.2 CCD quantum efficiency [20]

12.4 Sample transfer

With respect to BSCCO; in order to transfer our sample to a high k-dielectric (which solves our problem of leakage current) we put a PC film on top of the flake by spin coating it. We then raise the temperature in order to melt the PC film and have it fill every nook in cranny. Afterwards, we cool it down to solidify it into its place. Next, UV-gel is applied on top of our structure. In the next step, we apply a glass sheet on top of the UV and we harden the gel by exposing it to UV-light for 5 minutes. All the parts that were mentioned; the PC-film and the glass are now joined together. By lifting off the structure by the glass plate, we lift everything but the substrate.

Now the whole structure, with the flakes at the very bottom, is stamped on top of a high k-dielectric insulator to fix the problem. As the final step, we dissolve everything, but the substrate, the k-dielectric (in our case Hafnium) and the flake, by exposing it to chloroform. This can lead to many interesting applications like another layer of transporting charge that is formed by applying a gate voltage and a negative bottom voltage. Whether the charges do not recombine in this case is to be seen.