A Validation and Performance Analysis of a Distributed Control Scheme for DC Microgrids

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Abstract

This Bachelor Integration Project validates the performance of a novel distributed control scheme for DC microgrids. The control scheme is designed to acquire the objectives of current sharing and voltage regulation. Extensive simulation scenarios are applied to the control scheme in order to validate its performance. The controller attains the control objectives with more general ZIP loads. Moreover, the controller is altered to successfully achieve power sharing which is a nonlinear control objective. To conclude, the control scheme also performs well while applied to a larger network including the applied ZIP loads.

Contents

1. Introduction

The demand for renewable energy sources is growing rapidly along with the ever growing energy demand of the global community. Due to their finite and pollutive nature, the trusted fossil fuels will gradually be replaced by renewable energy sources (Setiawan & Asvial, 2016). Moreover, the Alternating Current (AC) power network that coincided with the utilization of fossil fuels has developed its setbacks which are high energy costs, long distance transmission lines and limited funds to construct large new power plants (Justo et al., 2013). Taking these setbacks into consideration among the facts that the current AC power network infrastructure is aging, the energy consumption standard is higher than ever and the number of DC loads is increasing due to advance in power electronics, the demand arises for a more configurable, flexible and informative energy system (Kaygusuz, 2012). Since renewable energy sources (e.g. Photo Voltaic (PV) systems, fuel cells and batteries) predominantly provide and accept direct current (DC) electricity, all-DC microgrids are proposed as an answer to this demand (Nasirian et al., 2015). A DC microgrid consists of Distributed Generation Units (DGU) and Energy Storage Systems (ESS) (Cucuzzella et al., 2019). The DC microgrid can either be connected or disconnected to the main grid. In connected mode the microgrid either receives or injects power to the main grid. Moreover, the DGUs main function within the microgrid is to generate power and support the microgrid system (Lopes, Moreira & Madureira, 2006). In disconnected mode the microgrid is cut off from the main grid and relies on its own capacity. In this case the microgrid is enabled to shut down its loads that have lowest priority (Shahabi et al., 2009). The advantages that DC microgrids have over the AC grid include, but are not limited to, decreased complexity and cost and improved efficiency (Karami & Cuzner, 2016). Moreover, the utilization of DC microgrids counteract the power generation losses that occur during the conversion from DC to AC and vice versa. (Hirsch, Parag & Guerrero, 2018).

Even though the application of DC microgrids bears ample advantages, it also has its challenges. Two of these challenges are current sharing and voltage regulation between the DGUs. Current sharing prevents the over stressing of any source and voltage regulation is required to ensure proper functioning of the end loads (Cucuzzella et al., 2019). In addition, often either one of these challenges is but not both simultaneously. Trip et al. (2019) proposed a novel distributed control scheme that achieves voltage regulation as well as current sharing between DGUs by local communication between neighbouring DGUs. Moreover, the proposed controller achieves these objectives by merely utilizing the local and connected DGU current measurements without requiring voltage measurements. The advantages of a distributed control structure over a centralized are: improved efficiency, reliability, expendability and stability (Nasirian et al., 2015).

This Bachelor Integration Project (BIP) contributes to the existing knowledge through the provision of new insights on the behaviour of the control scheme designed by trip et al. (2019). More specific, the performance of the controller designed by trip et al. (2019) is validated by exposing it to more realistic scenarios. These scenarios are: the application of

more common ZIP loads, the introduction of the power sharing objective and the upscaling of the network that is employed. These scenarios will be simulated in MATLAB and Simulink.

This BIP will proceed in the following structure. In chapter 2, the problem at hand is identified and described after which a stakeholder analysis is made. Furthermore, the system in which this BIP operates is defined and described. Moreover, the scope is defined and a problem statement is formulated. In chapter 3, the research goal and questions will be formulated in order to structure the research. In chapter 4 and 5, the design cycle that is utilized for this research is identified and the applied methodology and tools are explained. In chapter 6, a risk analysis is performed regarding this BIP. Chapter 7 states the assumptions that are made for this project and the parameters that are assigned to the DGUs in the simulations. In chapter 8, the load of the DGUs is modified after which the controller response is simulated with the updated loads. In chapter 9, the objective of power sharing will be investigated while also applying the loads used in chapter 8. In chapter 10, the behaviour of the controller is evaluated when applied to larger networks while also applying the modified loads. Moreover, this scenario will be executed with the current sharing objective as well as the power sharing objective. In chapter 11 and 12, the results of the simulations are evaluated and interpreted after which they are discussed. Chapter 13 will conclude this BIP.

2. Problem Analysis

In this chapter, the problem at hand is described after which a stakeholder analysis is made. Subsequently, the system that is used in this BIP is defined. Next, a scope is set for this research and to conclude, a problem statement is formulated which will be the incentive for this research.

2.1 Problem at hand

The problem of this BIP is that the model that is employed by Trip et al. (2019) may be affected by uncertainties, unmodeled dynamics and unknown external disturbances. Moreover, the paper of Trip et al. (2019) does not employ the average model instead of the switching model which implies that the system may respond different in real life than in simulations. This may indicate the need for a remodeling of the system and other uncertainties and a comparison between the theoretical response of the system and simulations.

2.2 Problem Owner

The problem owner of this BIP is pr. dr. ir. J.M.A. Scherpen. As chair of the Discrete Technology and Production Automation (DTPA) research group she has an extensive interest and influence in the outcome of this research as she is also responsible for the research output of the DTPA research group.

2.3 Stakeholder Analysis

The second stakeholder of this is M. Cucuzzella. Cucuzzella is the daily supervisor of this BIP and thus has a high influence on the outcome of this project as his expertise focuses mainly on DC microgrids. Moreover, he also had a stake in the controller that is proposed which also gives him a high interest in the outcome of this project. He will have a high level of influence on the direction of this project which deems him an important stakeholder.

The third stakeholder is M. Stokroos. He is the head of the DTPA lab and his stake in this BIP is to ensure the safety of the DTPA lab. Moreover, he is also responsible for the equipment within the DTPA lab and will provide the equipment necessary in order to conduct the experiments. Furthermore, he does not have a specific interest in the outcome of this research. However, he will be responsible for the provision of equipment and the proper utilization of it which will give him a considerable influence on the experimental phase of this BIP.

The fourth and final stakeholder of this BIP is C. De Persis. As chair of the Smart Manufacturing Systems (SMS) group, he will also be interested in the outcome of this BIP due to his research endeavors in smart grids.

2.4 System description

The system in which this BIP operates consists of the general mathematical model of a DGU and the control scheme proposed by trip et al. (2019). In chapter 8, the controller is applied to a two node network and in chapter 10 to a five node network and ten node network. Moreover, the control objectives current sharing and average voltage regulation are discussed.

2.4.1 Mathematical model

The mathematical model that is utilized and cited below is defined and formulated by Cucuzzella et al. (2019). The model describes a typical DC microgrid consisting of n DGUs connected by m resistive-inductive power lines as depicted in figure 2.1. The application of Kirchhoff's current (KCL) and voltage (KVL) laws yield the following dynamic equations of the i-th DGU:

$$L_{ti}\dot{I}_{ti} = -R_{ti}I_{ti} - V_i + u_i \tag{2.1}$$

$$C_{ti}\dot{V}_i = I_{ti} - I_{Li} - \sum_{j\in\mathcal{N}_i}^{n} I_{ij}, \tag{2.2}$$

where $\mathcal{N}_i$ is the set of DGUs connected to the i-th DGU by the power lines. The control input u_i represents the buck converter output voltage. Moreover, the current from DGU i to DGU j is denoted by I_{ij} and its dynamic equation is given by

$$L_{ij}\dot{I}_{ij} = (V_i - V_j) - R_{ij}I_{ij}. \tag{2.3}$$

The symbols used in (2.1), (2.2) and (2.3) are displayed in tables 2.1 and 2.2.

The overall network of DGUs and power lines is represented by a connected and undirected graph $\mathcal{G} = (\mathcal{V}, \mathcal{E})$, where the nodes, $\mathcal{V} = 1, ..., n$, represent the DGUs and the edges, $\mathcal{E} = 1, ..., m$, represent the power lines interconnecting the DGUs. The network topology is represented by its corresponding incidence matrix $\mathcal{B} \in \mathbb{R}^{nxm}$. The ends of edge k are arbitrarily labeled with a + and a , and the entries of $\mathcal{B}$ are given by

$$\mathcal{B}_{ik}\begin{cases} +1 & \text{if } i \text{ is the positive end of } k \\ -1 & \text{if } i \text{ is the negative end of } k \\ 0 & \text{otherwise} \end{cases} \tag{2.4}$$

State variable	Denotes
I_{ti}	Generated current
V_i	Load voltage
I_{ij}	Line current
Inputs	**Denotes**
u_i	Control input
I_{Li}	Current demand

Table 2.1: Description of the used symbols in (2.1), (2.2) and (2.3)

Parameter	Denotes
L_i	Filter inductance
C_i	Shunt capacitor
R_{ij}	Line resistance
L_{ij}	Line inductance
R_i	Filter resistance

Table 2.2: Description of the used symbols in (2.1), (2.2) and (2.3)

2.4.2 The DGU model

The DGU model consist of a DC voltage source, a DC-DC buck converter, a current sensor, an inductor, a resistor, a capacitor, a load resistor and a voltage sensor. The voltage sensor is located at the point of common coupling PCC. The power transmission line consists of an inductor and resistor. The described set up can be found in figure 2.1.

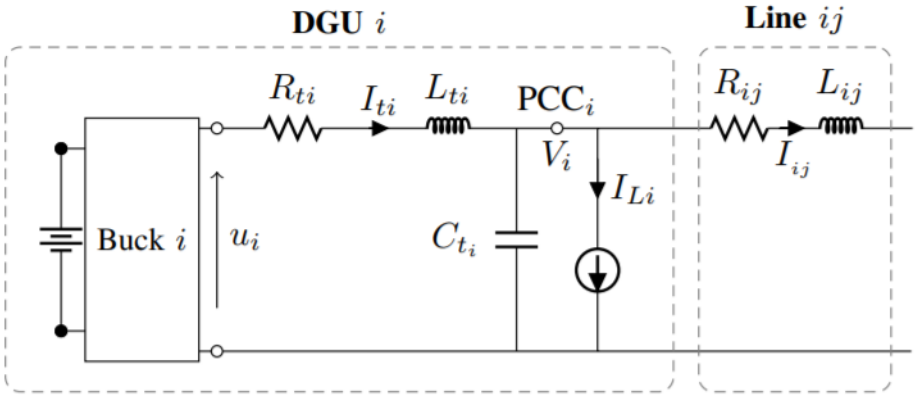

Figure 2.1: Electrical scheme of DGU i and power line k

2.4.3 Buck converter

The buck converter depicted in figure 2.1 is an important subsystem of a DGU in a DC microgrid. The buck converter is a device that is switched on and off in order to step down the input voltage of the DGU. The duty cycle is the ratio that the switch is open and closed and is related to the output voltage in equation (2.5).

$$u_i = V_{out} = V_{in}\delta \tag{2.5}$$

2.4.4 Control objectives

The two control objectives as described in chapter 1 are current sharing and voltage regulation. These two objectives are mathematically expressed in the following equations:

$$\lim_{t\to+\infty} I_t(t) = \bar{I}_t = W^{-1}\mathbb{1}i_t^* \tag{2.6}$$

$$\lim_{t\to+\infty} \mathbb{1}W^{-1}V_t(t) = \mathbb{1}^T W^{-1}\bar{V} = \mathbb{1}^T W^{-1}V^* \tag{2.7}$$

Equation (2.6) expresses the objective of current sharing where $W = \text{diag}(w_1, ..., w_n), w_i > 0$ and i_t^* is expressed as $\frac{\mathbb{1}^T I_L}{\mathbb{1}^T W^{-1}\mathbb{1}}$.

Equation (2.7) expresses the objective of voltage regulation. In addition, $V*$ denotes the desired voltage values of DGU i.

2.4.5 Control scheme

The control scheme dynamics proposed by Trip et al. (2019) are displayed in (2.8), (2.9) and (2.10). The parameters T_{θ_i}, T_{ϕ_1} and K_i permit appropriate tuning of the transient response. Moreover, γ_{ij} denotes the edge weight to a node. In addition, the control input u_i can be related to the duty cycle of a buck converter and the input voltage of the DGU. This relation is given in equation (2.5).

$$T_{\theta_i}\dot{\theta}_i = \sum_{j\in\mathcal{N}_i^{com}} \gamma_{ij}(w_i I_{ti} - w_j I_{tj}) \tag{2.8}$$

$$T_{\phi_i}\dot{\phi}_i = -\phi_i + I_{ti} \tag{2.9}$$

$$u_i = -K_i(I_{ti} - \phi_i) + w_i \sum_{j\in\mathcal{N}_i^{com}} \gamma_{ij}(\theta_i - \theta_j) + V_i^* \tag{2.10}$$

The set $\mathcal{N}_i^{com}$ is the set of nodes connected to node i via a communication network, with edge weights $\gamma_{ij} = \gamma_{ji} \in \mathbb{R}_{>}0$. Similar to the topology of the microgrid, the overall communication network is represented by a connected and undirected graph $\mathcal{G}^{com} = (\mathcal{V}^{com}, \mathcal{E}^{com})$), where $\mathcal{V}^{com} = \mathcal{V}$ and the edges, $\mathcal{E}^{com} = 1, ..., mc$, represent the communication links between the DGUs. The communication network topology is described by its corresponding incidence matrix $\mathcal{B}^{com} \in \mathbb{R}^{nxm_c}$, which is defined similarly as $\mathcal{B}$

2.5 Scope

Initially, the scope of this BIP will be limited to test the controller proposed by trip et al. (2019) within a more realistic model. The utilization of extensive simulations will be emphasized as physical experiments cannot be conducted due to the situation revolving around the COVID-19 crisis. Moreover, the two objectives of current sharing and voltage regulation will be inside the scope of this project opposed to any other kind of objectives. Two last interesting endeavors will lie in the incorporation of a nonlinear load modification and possibly the design of a non-linear consensus protocol for achieving power sharing instead of current sharing.

2.6 Problem Statement

Considering the desires of the stakeholders, the system description and the problem context, the problem statement can be defined as:
The model that is employed to test the control scheme proposed by trip et al. (2019) lacks real-life complexities which may impair the perfomance of the control scheme when applied to real-life scenarios.

3. Research Goal and Questions

In this chapter, a research goal will be formulated and also its accompanying research questions that will help to execute this research.

3.1 Research Goal

The goal of this BIP is to provide new insights in the application of the proposed control scheme by Trip et al (2019) and validate by means of simulations whether the proposed control scheme achieves the control objectives of current sharing and voltage regulation. The control scheme will also be applied to more complex models and different loads in order to verify the robustness of the control scheme under more complex circumstances. If the control scheme does not achieve voltage regulation and current sharing under the introduced circumstances, the controller will be modified and tuned in order to acquire the control objectives.

3.2 Research Questions

In order to attain the research goal stated in section 3.1 and taking the problem described in section 2 into account, the main research question can be formulated as:

What is the performance of the control scheme proposed by Trip et al. (2019) when applied to a more complex model?

The following sub-research questions have been formulated to help answer the main research question:

- *How can a more complex load be modeled?*
- *How to incorporate uncertainties, unmodeled dynamics and unknown disturbances into the model?*
- *How to modify the control scheme if it does not acquire the control objectives?*
- *How does the control scheme perform within the complex model?*

4. Design Cycle

Hevner (2007) embodies design science research as three closely related cycles of activities. These three cycles are the relevance cycle, the design cycle and the rigor cycle. These cycles are depicted in figure 4.1. In this BIP, the design cycle will be utilized. The relevance cycle initiates the design cycle by serving as an opportunity or problem as input after which the design cycle applies the knowledge provided by the rigor cycle. Furthermore, the design cycle is a constant process of (re)designing and evaluating the artefact. Moreover, if the design goals are not satisfied the cycle will be repeated until satisfactory results are achieved.

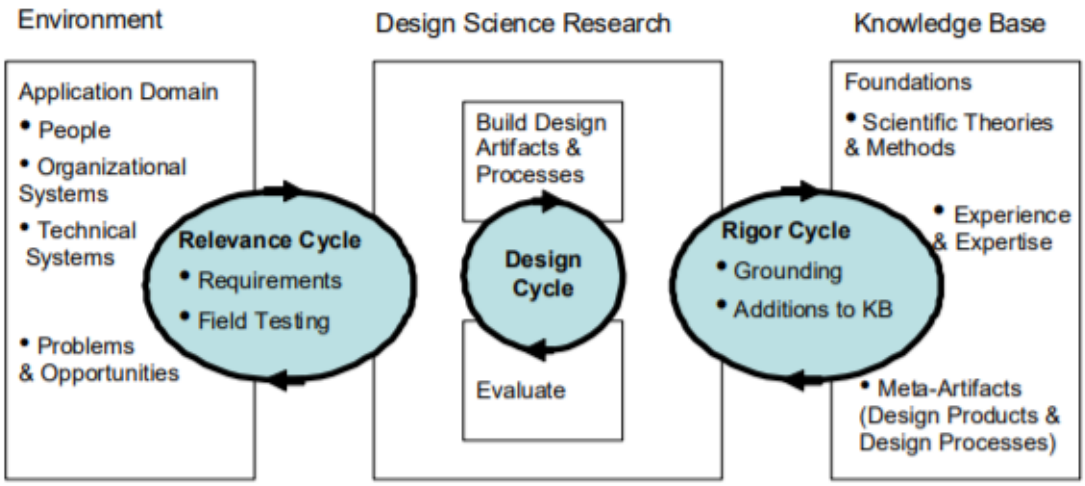

Figure 4.1: Hevner's embodiment of design science research

5. Methodology, Tools and Validation

In this chapter, the applied methodology for this BIP is explained. This will entail which steps are taken in order to produce satisfactory results in this research and which steps are to be taken. Moreover, the tools used in this BIP are listed and the validation of the outcome of this research.

5.1 Methodology

In order to test the robustness of the proposed control scheme by trip et al. (2019), the simulations with the model used in the same paper will be replicated. This replication will serve as a starting point from which complexities will be incorporated into the model after which the control scheme will be applied again in order to test the robustness of the control scheme. If the control scheme does not attain the control objectives, i.e., current sharing and voltage regulation, then the control scheme will be modified with the purpose of achieving these control objectives.

5.2 Tools and Validation

The tools that will be used to test the robustness and performance of the control scheme are Matlab, Simulink. Simulink will simulate the behaviour of the control scheme when applied to the mathematical model of the system by means of a block diagram. The simulations will validate whether the theoretical modifications to the model are justified.

6. Risk analysis

The risk is evaluated as the consequence in case of failure of the goal of this project. The primary failure at hand is that the performance of the control scheme proposed by Trip et al. (2019) cannot be validated on more complex systems. This imposes a low risk as more effort and resources can be spent on fine-tuning the control scheme. However, as this control scheme has already been proven to function on a simplified two-node model chances are considerable that the control scheme can be modified to regulate a more complex model.

7. Assumptions and Parameters

In this chapter, the assumptions that are made to bound this research are listed and the parameters that are used in the mathematical model described in section 2.4.1 are explained.

7.1 Assumptions

Several assumptions are made to set a boundary for this research. These assumptions are listed below.

- The network that is considered for the simulation is connected and undirected.
- There exists a reference voltage V_i^*, for each DGU i.
- The generated current I_i is measurable at DGU i.

7.2 Model parameters

The parameters that are assigned to the DGUs and the power lines are displayed in table 7.1. These parameters are based on the paper written by Trip et al. (2019) who managed to establish meaningful parameter ranges typically used for DC microgrids.

DGU i	1	2	3	4	5	6	7	8	9	10
R_i (Ω)	0.5	0.2	0.3	0.1	0.4	0.2	0.4	0.6	0.3	0.5
C_i (mF)	2.2	1.9	2.5	1.7	1.8	2.5	1.9	2.5	1.9	1.9
L_i (mH)	1.8	2.0	3.0	2.2	2.5	3.0	2.2	3.0	2.2	2.4
Line (i,j)	(1,2)	(2,3)	(3,4)	(4,5)	(5,6)	(6,7)	(7,8)	(8,9)	(9,10)	(1,10)
R_{ij} (Ω)	0.07	0.05	0.08	0.06	0.09	0.05	0.07	0.05	0.08	0.06
L_{ij} (μH)	2.1	2.3	2.0	1.8	1.5	2.1	2.3	2.0	1.8	1.6

Table 7.1: Parameters of each DGU and power line

8. ZIP Load Implementation

This chapter will elaborate on how the impedance load of the two node model is replaced by a ZIP load structure in order to deem the model more complex. First, the definition of a ZIP load structure is explained after which the ZIP loads will be implemented in the model. Subsequently, a load model is synthesized and simulation results are interpreted. Moreover, two load scenarios are simulated in order to evaluate the behaviour of the transient controller response.

8.1 ZIP-loads

The model described in section 2.4 utilizes a constant current load. However, In order to deem the model more complex, a ZIP load structure will be applied instead of a constant current load structure. ZIP loads consists of a constant impedance load (Z), constant current load (I) and a constant power load (P) (Cucuzzella, Kosaraju & Scherpen, 2019). To validate the performance of the controller proposed by trip et al. (2019), the simulink model has been altered to feature a ZIP load structure. This simulink model is depicted in figure 15.1 in section 15.1 and the implemented ZIP load structure is illustrated in figure 15.2 in section 15.2. Figure 15.2 illustrates the parallel connection of the ZIP loads into the model instead of the impedance load in figure 2.1.

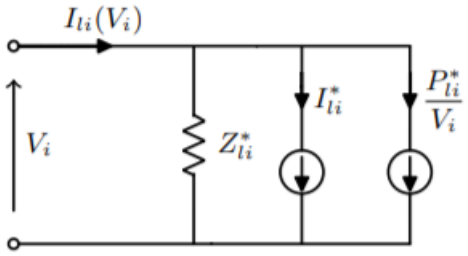

Figure 8.1: Illustration of the ZIP load into the model of figure 2.1

8.1.1 Constant Impedance Load (Z^*_{li})

The constant impedance load of the ZIP load can be expressed as a current load. This expression is given in equation 8.1 where

$$I_{li} = \frac{V_i}{Z^*_{li}} \tag{8.1}$$

8.1.2 Constant Current Load (I^*_{li})

The constant current load of the ZIP load can also be expressed as a current load. This is expression is given in equation (8.2).

$$I_{li} = I^*_{li} \tag{8.2}$$

8.1.3 Constant Power Load (P_{li}^*)

The constant power load can also be expressed as a current load. This expression is given in (8.3)

$$I_l = \frac{P_{li}^*}{V_i} \tag{8.3}$$

8.1.4 Model modification

As mentioned in section 8.1, the impedance load in 2.4 will be replaced by a ZIP load. The constant current term in equations (2.2) will be replaced by the following term:

$$I_{li}(V_i) = \frac{V_i}{Z_{li}^*} + I_{li}^* + \frac{P_{li}^*}{V_i} \tag{8.4}$$

8.1.5 Load parameters

In table 8.1 the applied ZIP loads can be found which are used to test the performance of the controller for the first scenario. The second scenario employs the same values of table 8.1 however the order of the loads is reversed in order to evaluate the transient behaviour of the controller. These values are found in table 8.2. The ZIP loads are altered in four time modes in order to validate whether the control scheme acquires the control objectives of current sharing and average voltage regulation. The ZIP load values are chosen to fall within the ranges specified by Cucuzzella, Kosaraju & Scherpen (2019). The ZIP loads change per time step in order to evaluate the behaviour of the controller as a response to change in loads. The incidence matrix and the communication matrix of the two node network are displayed in (8.5) and (8.6), respectively.

$$\mathcal{B} = \begin{pmatrix} -1 \\ 1 \end{pmatrix} \tag{8.5}$$

$$\mathcal{B}^{com} = \begin{pmatrix} -1 \\ 1 \end{pmatrix} \tag{8.6}$$

	DGU 1			DGU 2		
Time (s)	Z_{l1}^*	I_{l1}^*	P_{l1}^*	Z_{l2}^*	I_{l2}^*	P_{l2}^*
0 - 2.45	25	10	10000	12.5	15	5000
2.50 - 4.95	12.5	15	14000	25	10	3000
5.00 - 7.45	12.5	10	12000	25	15	4000
7.50 - 10.00	25	10	12000	12.5	10	4000

Table 8.1: Overview of the applied ZIP loads of scenario 1

	DGU 1			DGU 2		
Time (s)	Z^*_{l1}	I^*_{l1}	P^*_{l1}	Z^*_{l2}	I^*_{l2}	P^*_{l2}
0 - 2.45	25	10	12000	12.5	10	4000
2.50 - 4.95	12.5	10	12000	25	15	4000
5.00 - 7.45	12.5	15	14000	25	10	3000
7.50 - 10.00	25	10	10000	12.5	15	5000

Table 8.2: Overview of the applied ZIP loads of scenario 2

8.2 Simulation Results

The results of the first simulation scenario of the incorporated ZIP loads are shown in figures 8.2, 8.3 and 8.4. Subsequently, the results of the second scenario are given in figures 8.5, 8.6 and 8.7. Figures 8.2 and 8.5 represent the current generated in the DGUs whereas figures 8.3 and 8.6 represent the current flowing between the DGUs. Moreover, figures 8.4 and 8.7 represent the voltage in the DGUs. The outcomes of these simulations are interpreted in section 11.1.

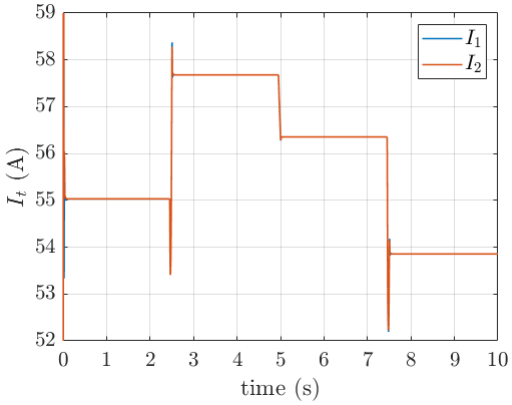

Figure 8.2: Graph of the currents in the DGUs over time

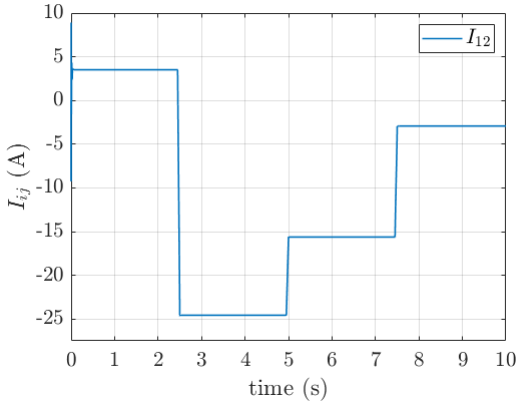

Figure 8.3: Graph of the current in the line between DGU 1 and DGU 2 over time

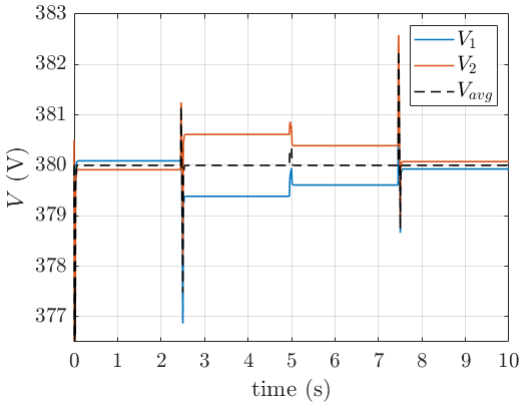

Figure 8.4: Graph of the voltages in the DGUs over time

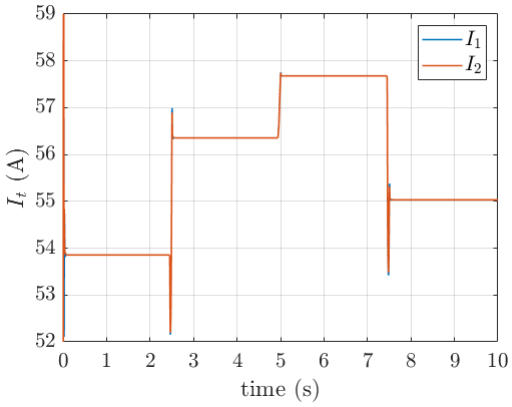

Figure 8.5: Graph of the currents in the DGUs over time

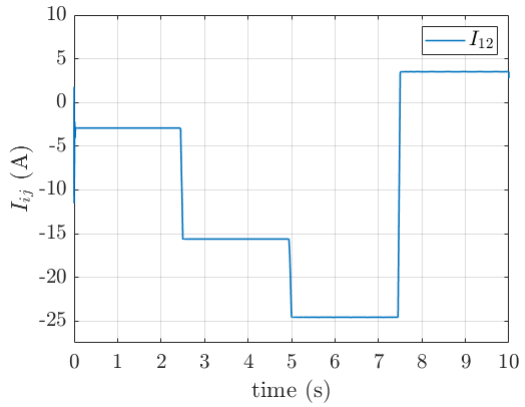

Figure 8.6: Graph of the line current between the DGUs over time

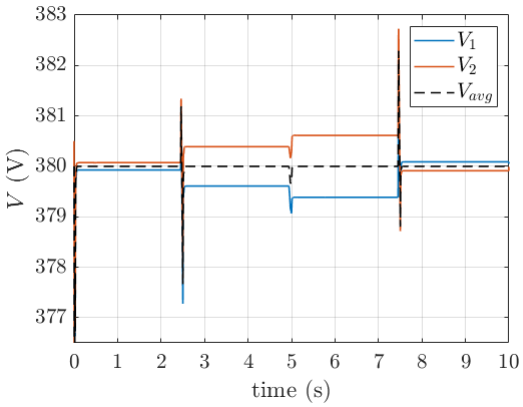

Figure 8.7: Graph of the voltages at the DGUs over time

9. Power Sharing Objective

Besides the two common control objectives, current sharing and average voltage regulation, power sharing is also a desired control objective. Power sharing is desired as it prevents local loads from overloading local DGUs which may lead to failures. Power sharing is thus crucial for the safety of a microgrid (Fan et al., 2020). In this chapter, a control objective will be formulated which features power sharing as goal. Moreover, the model will be altered such that the power sharing objective can be incorporated. Furthermore, just as in chapter 8, the two ZIP load scenarios are employed in order to evaluate the performance of the controller.

9.1 Control objective

The control objective of current sharing in section 2.4.4 equation (2.6) can be altered such that this objective is converted into the power sharing objective. This done by replacing the current term I with the expression for power which is $I * V$. Implementing this alteration will results in the following objective that promotes power sharing:

$$\lim_{t \to +\infty} I_t(t) \circ V_t(t) = \bar{P}_t = W^{-1} \mathbb{1} p_t^* \tag{9.1}$$

9.2 Model modifications

By altering the introducing the control objective of power sharing in section 9.1, the control scheme will also be slightly modified in order to attain the control objective. By replacing the current terms in equations (2.8) and (2.9) with the power terms, the equations will convert to:

$$T_{\theta_i} \dot{\theta}_i = \sum_{j \in \mathcal{N}_i^{com}} \gamma_{ij} (w_i I_{ti} V_{ti} - w_j I_{tj} V_{tj}) \tag{9.2}$$

By introducing this term in the control scheme, the objective of power sharing can be achieved. Figure 15.3 in section 15.3 depicts the Simulink model that is used for the simulations of the power shaing scenario.

9.3 Simulation results

The results of the first simulation scenario with the objective of power sharing are shown in figures 9.1, 9.2, 9.3 and 9.4. Moreover, the results of the second simulation scenario are shown in figures 9.5, 9.6, 9.7 and 9.8. The results are interpreted in section 11.2. To clarify, figures 9.1 and 9.5 represent the current in the DGUs whereas figures 9.2 and 9.6 represent the current flowing between the DGUs. Moreover, figures 9.3 and 9.7 represent the voltages in the DGUs and figures 9.4 and 9.8 represent the powers in the DGUs.

9.3.1 Scenario 1

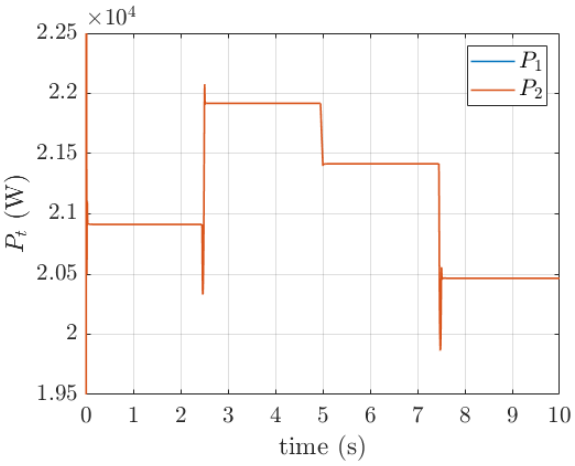

Figure 9.1: Graph of the powers in the DGUs over time

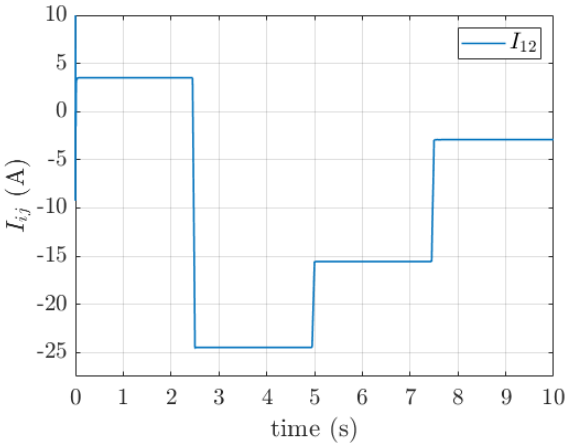

Figure 9.2: Graph of the line current between the DGUs over time

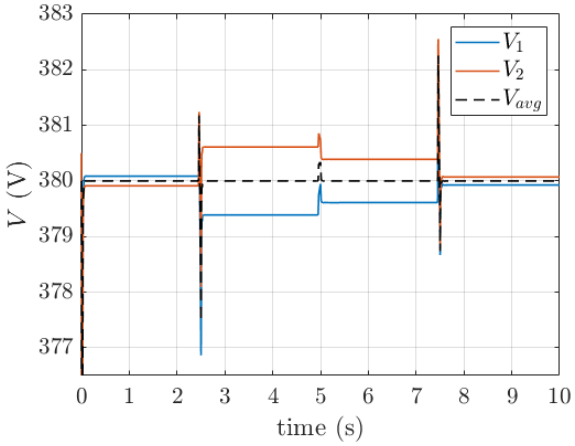

Figure 9.3: Graph of the voltages in the DGUs over time

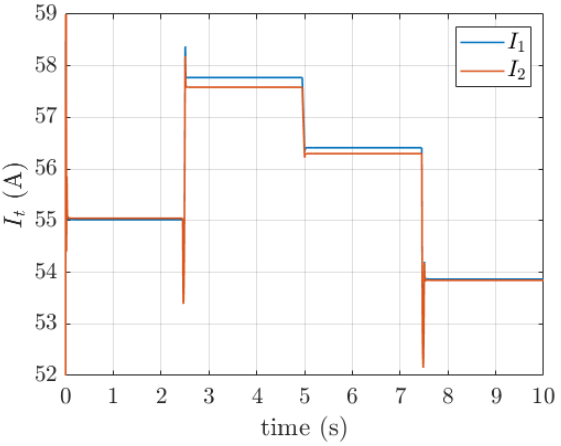

Figure 9.4: Graph of the currents in the DGUs over time

9.3.2 Scenario 2

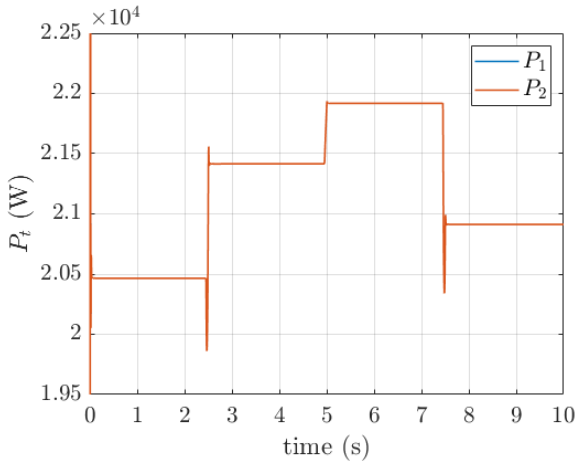

Figure 9.5: Graph of the powers in the DGUs over time

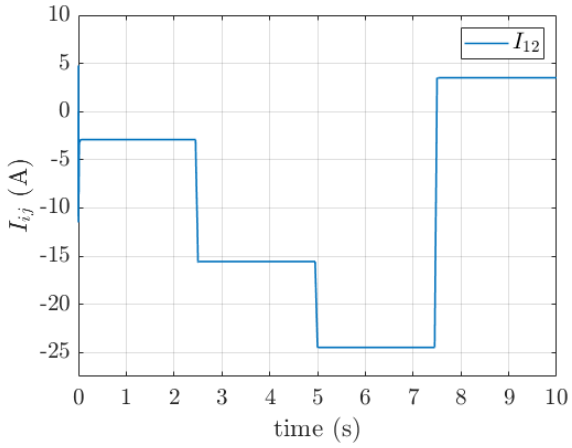

Figure 9.6: Graph of the line current between the DGUs over time

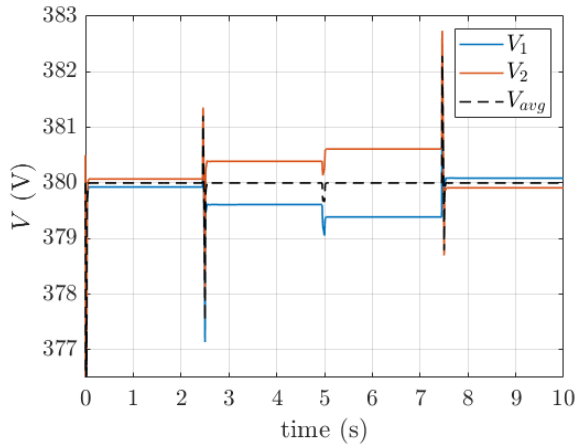

Figure 9.7: Graph of the voltages in the DGUs over time

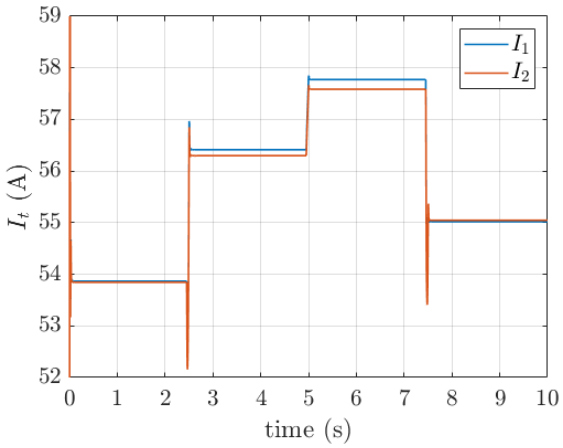

Figure 9.8: Graph of the currents in the DGUs over time

10. Upscaling of the network

In chapter 8 and 9, the controller response is evaluated while applying various ZIP loads while striving for current sharing or power sharing. These simulations have been applied to a network of two DGUs whereas in this chapter will be evaluated whether the control objectives are attained when the controller is applied to a network of five or ten DGUs including varying ZIP loads. For the first scenario the model contains 5 DGUs and 5 lines and for the second scenario the model contains 10 DGUs and 10 lines.

10.1 Five node network

The mathematical model in section 2.4.1 is converted such that a five node network exists. A visual representation of the five node network is depicted in figure 10.1. The accompanying incidence matrix and communication matrix is given in (10.1) and (10.2). The ZIP loads that are applied to each DGU can be found in table 10.1. The ZIP loads are randomly determined but do fall within realistic ranges according to Trip et al. (2019). Moreover, the reference voltage of each DGU is set at 380 Volts.

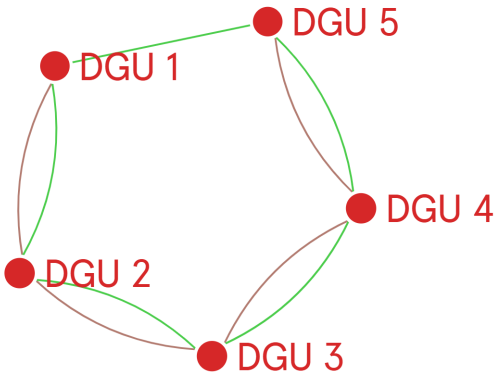

Figure 10.1: Upscaled network topology of 5 DGUs where the red edges are the communication links and the green edges are the power transmission lines.

$$\mathrm{B} = \begin{pmatrix} -1 & 0 & 0 & 0 & -1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{pmatrix} \quad (10.1) \qquad \mathrm{B}^{com} = \begin{pmatrix} -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 1 \end{pmatrix} \quad (10.2)$$

	DGU 1			DGU 2			DGU 3			DGU 4			DGU 5		
Time (s)	Z^*_{l1}	I^*_{l1}	P^*_{l1}	Z^*_{l2}	I^*_{l2}	P^*_{l2}	Z^*_{l3}	I^*_{l3}	P^*_{l3}	Z^*_{l4}	I^*_{l4}	P^*_{l4}	Z^*_{l5}	I^*_{l5}	P^*_{l5}
0 - 2.45	25	10	1000	12.5	5	5000	12	12	8000	15	15	10000	15	15	4000
2.50 - 4.95	12.5	13	2000	25	7	3000	17	15	13000	5	10	7500	25	8	8000
5.00 - 7.45	12.5	18	1000	25	12	10000	22	20	18000	10	15	1500	30	13	13000
7.50 - 10.00	25	23	4000	12.5	7	2000	27	25	14000	5	10	500	35	18	11000

Table 10.1: Overview of the applied ZIP loads of the upscaled network

10.1.1 Simulation results : Current sharing

Figures 10.2, 10.3, 10.4 and 10.5 depict the simulation results of the upscaled network of 5 nodes and 5 lines while attaining the current sharing objective. Figure 10.2 represents the currents in the DGUs whereas figure 10.3 represents the currents flowing between the DGUs. Moreover, figure 10.4 represents the voltages in the DGUs and figure 10.5 represents the powers in the DGUs. These results will be interpreted in section 11.3.1

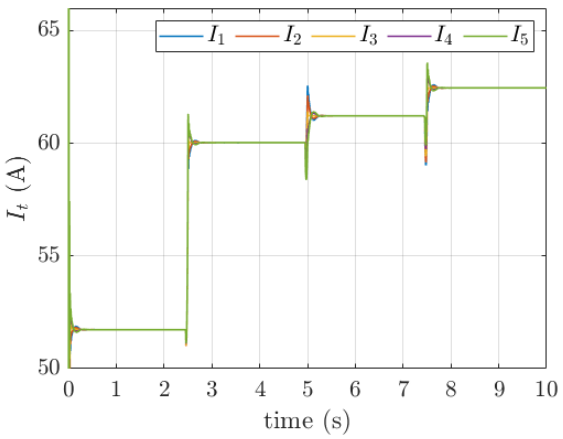

Figure 10.2: Graph of the currents in the DGUs over time

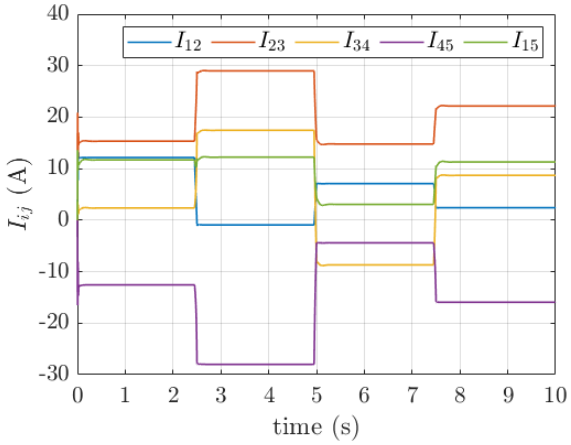

Figure 10.3: Graph of the line currents between the DGUs over time

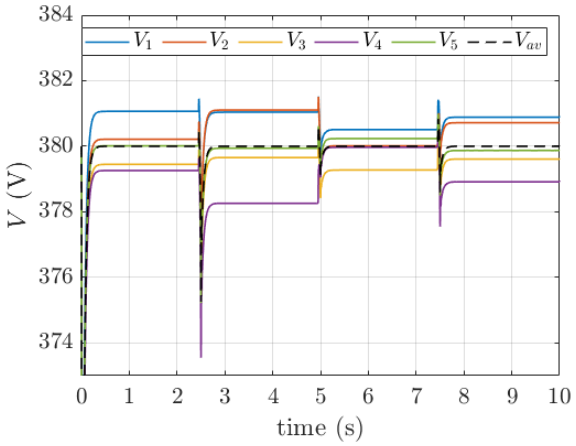

Figure 10.4: Graph of the voltages in the DGUs over time

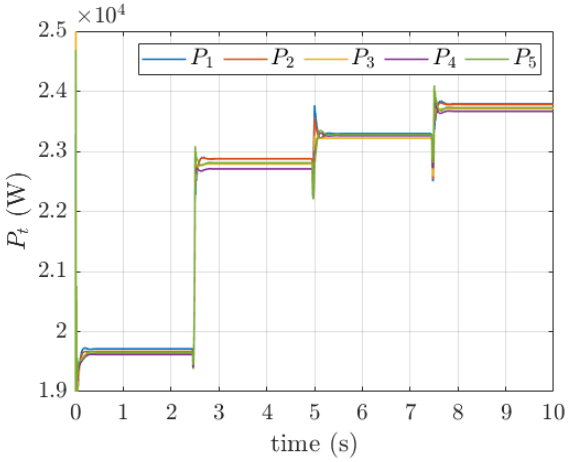

Figure 10.5: Graph of the powers in the DGUs over time

10.1.2 Simulation results : Power sharing

Figures 10.6, 10.7, 10.8 and 10.9 depict the simulation results of the upscaled network of 5 nodes and 5 lines while attaining the power sharing objective. Figure 10.6 represents the currents in the DGUs whereas figure 10.7 represents the currents flowing between the DGUs. Moreover, figure 10.8 represents the voltages in the DGUs and figure 10.9 represents the powers in the DGUs. These simulation results will be interpreted in section 11.3.1

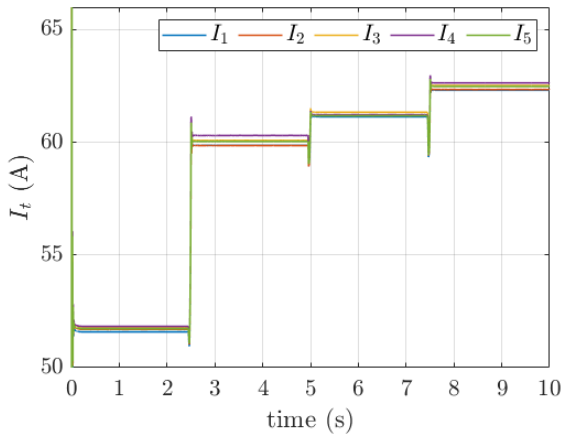

Figure 10.6: Graph of the currents in the DGUs over time

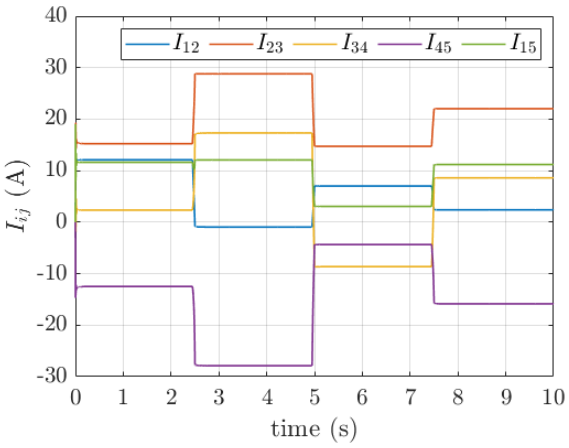

Figure 10.7: Graph of the line currents between the DGUs over time

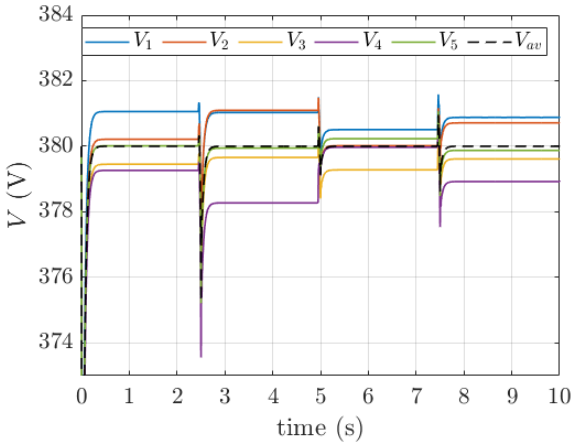

Figure 10.8: Graph of the voltages in the DGUs over time

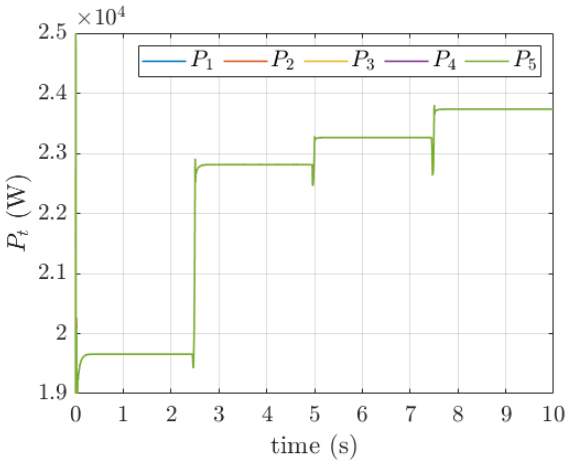

Figure 10.9: Graph of the powers in the DGUs over time

10.2 Ten node network

After testing the controller on a five node network, the network is upscaled to a ten node network. A visual representation of the ten node network is depicted in figure 10.10. The accompanying incidence matrix and communication matrix is given in (10.3) and (10.4). The ZIP loads that are applied to each DGU are dislayed in table 10.2. The ZIP loads are randomly determined but do fall within realistic ranges according to paper Trip et al. (2019). Moreover, the reference voltage of each DGU is set at 380 Volts.

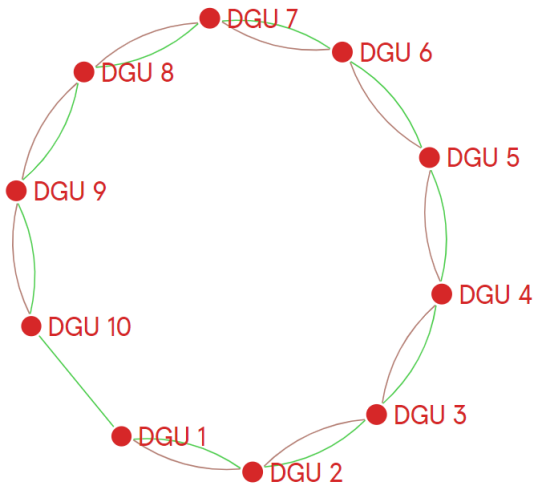

Figure 10.10: Upscaled network topology of 10 DGUs where the red edges are the communication links and the green edges are the power transmission lines.

$$\mathrm{B} = \begin{pmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0; \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix} \quad (10.3)$$

$$\mathrm{B}^{com} = \begin{pmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \quad (10.4)$$

	DGU 1			DGU 2			DGU 3			DGU 4			DGU 5		
Time (s)	Z^*_{l1}	I^*_{l1}	P^*_{l1}	Z^*_{l2}	I^*_{l2}	P^*_{l2}	Z^*_{l3}	I^*_{l3}	P^*_{l3}	Z^*_{l4}	I^*_{l4}	P^*_{l4}	Z^*_{l5}	I^*_{l5}	P^*_{l5}
0 - 2.45	25	13	10000	12.5	15	8000	17.5	12	6000	20	20	10000	15	15	5000
2.50 - 4.95	12.5	18	11000	25	20	6000	22.5	17	11000	10	25	7500	25	20	9000
5.00 - 7.45	12.5	23	9000	25	15	7000	27.5	22	16000	15	20	2500	30	25	14000
7.50 - 10.00	25	28	11000	12.5	10	2000	32.5	27	20000	10	15	500	25	30	16000
	DGU 6			DGU 7			DGU 8			DGU 9			DGU 10		
Time (s)	Z^*_{l6}	I^*_{l6}	P^*_{l6}	Z^*_{l7}	I^*_{l7}	P^*_{l7}	Z^*_{l8}	I^*_{l8}	P^*_{l8}	Z^*_{l9}	I^*_{l9}	P^*_{l9}	Z^*_{l10}	I^*_{l10}	P^*_{l10}
0 - 2.45	10	18	9000	15	14	10000	5	12	5000	20	15	8000	5	17	2000
2.50 - 4.95	22.5	23	13000	27.5	19	8000	10	17	10000	10	20	5500	15	22	6000
5.00 - 7.45	27.5	28	11000	27.5	14	9000	5	22	15000	15	15	2500	10	27	11000
7.50 - 10.00	17.5	33	13000	15	9	1000	10	27	19000	10	10	500	15	32	13000

Table 10.2: Overview of the applied ZIP loads of the upscaled network

10.2.1 Simulation results : Current sharing

Figures 10.11, 10.12, 10.13 and 10.14 depict the simulation results of the upscaled network of 5 nodes and 5 lines while attaining the current sharing objective. Figure 10.11 represents the currents in the DGUs whereas figure 10.12 represents the currents flowing between the DGUs. Moreover, figure 10.13 represents the voltages in the DGUs and figure 10.14 represents the powers in the DGUs. These results will be interpreted in section 11.3.2

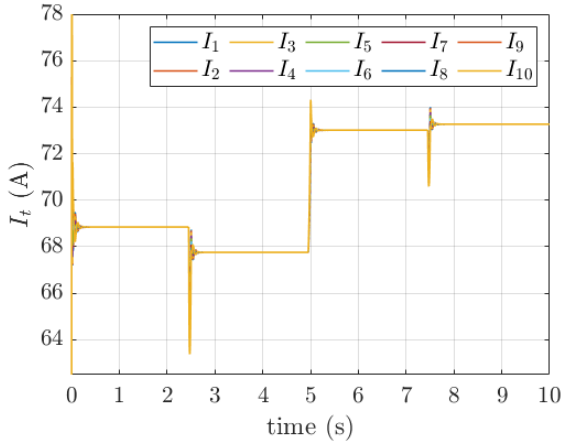

Figure 10.11: Graph of the currents in the DGUs over time

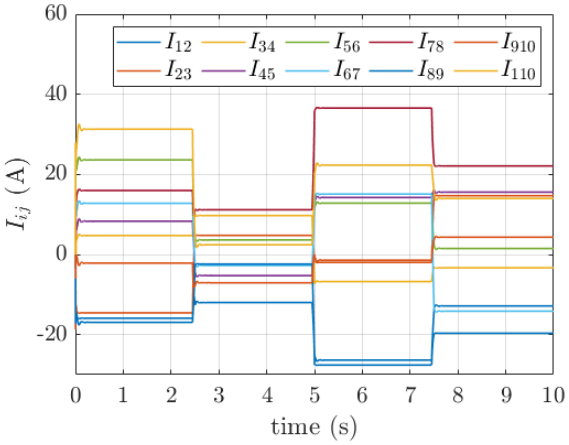

Figure 10.12: Graph of the line currents between the DGUs over time

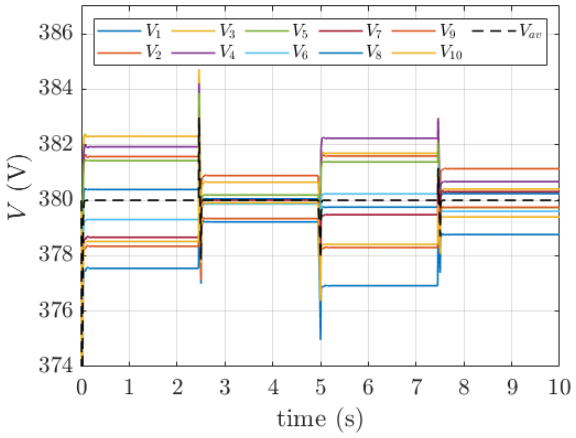

Figure 10.13: Graph of the voltages in the DGUs over time

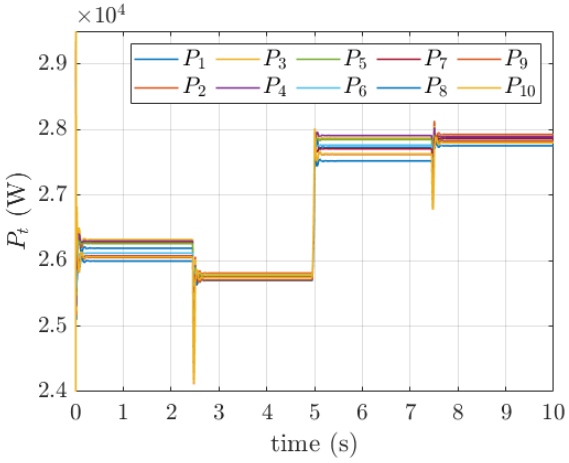

Figure 10.14: Graph of the powers in the DGUs over time

10.2.2 Simulation results : power sharing

Figures 10.15, 10.16, 10.17 and 10.18 depict the simulation results of the upscaled network of 5 nodes and 5 lines while attaining the power sharing objective. Figure 10.15 represents the currents in the DGUs whereas figure 10.16 represents the currents flowing between the DGUs. Moreover, figure 10.17 represents the voltages in the DGUs and figure 10.18 represents the powers in the DGUs. These simulation results will be interpreted in section 11.3.2

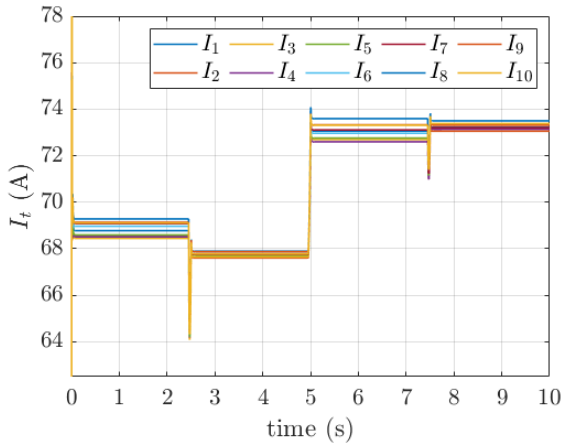

Figure 10.15: Graph of the currents in the DGUs over time

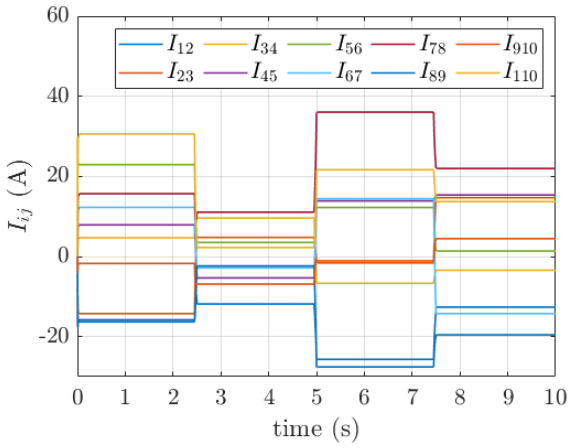

Figure 10.16: Graph of the line currents between the DGUs over time

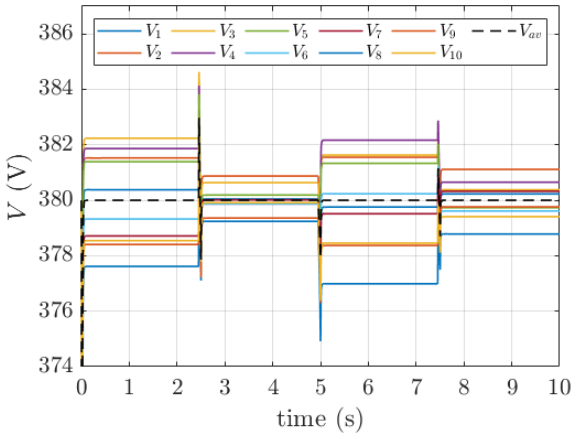

Figure 10.17: Graph of the voltages in the DGUs over time

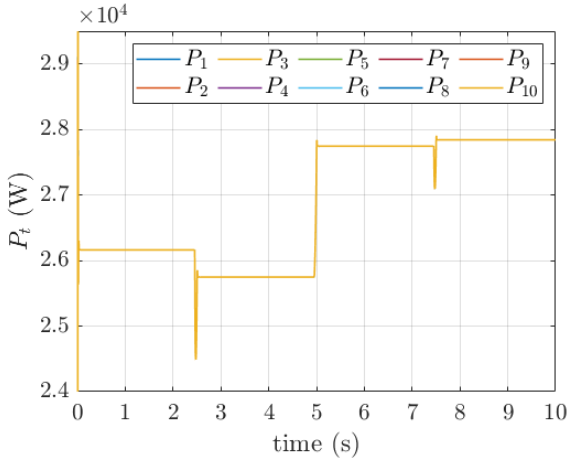

Figure 10.18: Graph of the powers in the DGUs over time

11. Results

In this chapter, the simulation results of sections 8, 9 and 10 are interpreted. In section 8, ZIP loads are implemented in the model after which the control scheme is tested under varying ZIP loads. In section 9, the control scheme is altered in order to attain the objective of power sharing instead of current sharing and tested under varying ZIP loads. In section 10, the model has been upscaled to contain 5 and 10 DGUs while applying the objectives of current sharing and power sharing under varying ZIP loads.

11.1 ZIP loads

11.1.1 First scenario

In figure 8.2, the currents in DGU 1 and 2 can be seen. This figure illustrates that the current generated in DGU 1 and DGU 2 are equal to each other. Moreover, figure 8.3 illustrates that current is flowing from one DGU to another. If the line current is positive, current is flowing from DGU 2 into DGU 1 and if the line current is negative, current is flowing from DGU 1 into DGU 2. According to (2.6), it can be concluded that the objective of current sharing is achieved.

Figure 8.4 illustrates the voltages at the PCC of each DGU over time. It shows that the voltages over each DGU are not equal to the reference voltage of $380V$ but the average of each DGU is equal to the reference voltage. From this figure, it can be concluded that the objective of average voltage regulation is also achieved since the average voltage of the graph is equal to the reference voltage which is set at $380V$. This is also in accordance with (2.7). Moreover, voltage peaks are seen at the time instances where the controller responds to the change in loads. To conclude, it becomes apparent that when a DGU is supplying current its PCC voltage is higher than the average voltage and when it is receiving it is lower than the average voltage.

11.1.2 Second scenario

In figure 8.5, the currents in DGU 1 and 2 can be seen. This figure illustrates that the current generated in DGU 1 and DGU 2 are equal to each other. Moreover, figure 8.6 illustrates that current is flowing from one DGU to another. If the line current is positive, current is flowing from DGU 2 into DGU 1 and if the line current is negative, current is flowing from DGU 1 into DGU 2. According to (2.6), it can be concluded that the objective of current sharing is achieved.

Figure 8.7 illustrates the voltages at the PCC of each DGU over time. It shows just as in scenario 1 that the voltages over each DGU are not equal to the reference voltage of $380V$ but that the average of each DGU is equal to the reference voltage. From this figure, it can also be concluded that the objective of average voltage regulation is also achieved since the average voltage of the graph is equal to the reference voltage which is thus set at $380V$. This is also in accordance with (2.7). Moreover, also during this scenario voltage peaks are seen at the time instances where the controller responds to the change in loads. When comparing both scenarios it becomes evident that the voltage spike during a change in load

is inversely related to the change of current in the DGUs. For example, at time 5.0 the currents generated in the nodes rises whereas the voltage graph exhibits a small voltage drop.

11.2 Power sharing objective

In section 9, the control scheme has been altered in order to attain the objective of power sharing. The two ZIP load scenarios in section 8.1.5 are also applied to this simulation scenario in order to interpret the behaviour of the controller.

11.2.1 First scenario

In table 8.1, the varying ZIP loads are displayed that are used in this simulation. In figures 9.4 and 9.1, the current and power generated in DGU 1 and DGU 2 can be found. Figure 9.4 illustrates that the powers generated in the DGUs are equal to each other whereas figure 9.1 illustrates that current sharing is not achieved in this case. Moreover, figure 9.2 illustrates the current flowing between DGU 1 and DGU 2, implying current is shared between them. From these figures it can be concluded that the objective of power sharing instead of current sharing is achieved according to (9.1).

Furthermore, figure 9.3 illustrates the voltages at the PCC of each DGU over time. The graph shows peaks on the time instances where the load is changed which is due to the system adjusting itself to the new loads. In addition, greater differences between DGU currents imply greater peaks in the DGU voltage. Moreover, when comparing figure 9.4 and 9.3 it can be concluded that negative voltage peaks indicate a positive change in currents and a positive voltage peak indicates a negative change in DGU current. Moreover, it can indeed be verified that the power in the DGU is equal to the current in the DGUs multiplied by the DGU voltages.

11.2.2 Second scenario

In table 8.2, the varying ZIP loads are displayed that are used in for this simulation scenario. In figures 9.5 and 9.8, the current and power generated in DGU 1 and DGU 2 can be found. Figure 9.8 illustrates that the powers generated in the DGUs are equal to each other whereas figure 9.5 illustrates that current sharing is not achieved in this case. Moreover, figure 9.6 illustrates the current flowing between DGU 1 and DGU 2, implying current is shared between them. From these figures it can be concluded that the objective of power sharing instead of current sharing is achieved according to (9.1).

Furthermore, figure 9.7 illustrates the voltages at the PCC of each DGU over time. The graph shows peaks on the time instances where the load is changed which is due to the system adjusting itself to the new loads like in scenario 1 but opposite instead. When comparing figure 9.5 and 9.7 it can also be concluded from this scenario that negative voltage peaks indicate a positive change in currents and a positive voltage peak indicates a negative change in DGU current.

11.3 Upscaled network

In chapter 10, the network of DGUs and power lines is upscaled in order to feature 5 DGUs and 5 power lines and 10 DGUs and 10 lines. The upscaled networks and their accompanying incidence and communication matrices are displayed in sections 10.1 and 10.2. Moreover, the applied ZIP loads for the five node network are displayed in table 10.1 and for the ten node network in table 10.2.

11.3.1 Five node network

Current sharing

Figures 10.2 and 10.3 illustrate the current generated in the DGUs and the current flowing between them. Since the currents generated in the DGUs are equal to each other, the control objective of current sharing is attained whereas power sharing is not. Furthermore, average voltage regulation is also achieved according to figure 10.4

Power sharing

Figures 10.9 and 10.7 illustrate the power generated in the DGUs and the current flowing between them. From figure 10.9 it can be concluded that power sharing is achieved whereas current sharing is not. Furthermore, average voltage regulation is also achieved according to figure 10.8.

11.3.2 Ten node network

Current sharing

Figures 10.11 and 10.12 illustrate the current generated in the DGUs and the current flowing between DGUs. Since the currents generated in the DGUs are equal to each other, the control objective of current sharing is attained whereas power sharing is not. Furthermore, average voltage regulation is achieved according to figure 10.13.

Power sharing

Figures 10.18 and 10.16 illustrate the power generated in the DGUs and the current flowing between them. From figure 10.18 it can be concluded that power sharing is achieved whereas current sharing is not. Furthermore, average voltage regulation is also achieved according to figure 10.17.

12. Discussion

After implementing the ZIP loads in chapter 8, the controller showed robustness against more complex load models. However, these loads are constant and further investigation into variable loads should be done in order to further validate the performance of the controller. Consequently, In chapter 9, the control objective of power sharing was introduced which the controller also attained. Furthermore, the controller was applied to larger network topologies of five and ten DGUs. However, in order to validate the performance of the controller even more, greater networks should be simulated. To conclude, the controller showed good performance during all the tested scenarios. In addition, physical experiments should be conducted to bridge the gap between the simulations and the physical world.

For future research, the response of the distributed control scheme proposed by Trip et al. 2019 could be further improved by designing a tuning algorithm that alters the controller parameters according to the scenario that is applied at that time. Furthermore, variable or even non-linear loads would also contribute to the performance of the control scheme. To conclude, extensive plug and play scenarios where certain communication links, DGUs or power transmission lines fail may deliver promising results.

13. Conclusion

In this Bachelor Integration Project, the performance of the novel distributed control scheme proposed by trip et al. (2019) has been evaluated by means of three different scenarios in order to validate its performance. These scenarios are: the implementation of ZIP loads into the model, the introduction of the nonlinear power sharing objective and the upscaling of the network topology. By building the model and the controller in Simulink, simulations are executed in order to evaluate the performance of the distributed control scheme. By applying the more general ZIP loads instead of the constant current load, the model was made more complex. The controller attained the control objectives of current sharing and voltage regulation under the applied ZIP loads indicating adequate performance. Furthermore, the control objective of power sharing has been introduced while maintaining the ZIP loads. The control also attained this objective with good performance. At last, the network topology was upscaled to contain 5 or 10 DGUs while also being equipped with the ZIP loads. The controller also attained the control of objective of current sharing and power sharing in these scenarios proving its robustness against larger networks. Therefore, it can be concluded that the application of the distributed control scheme designed by trip et al. (2019) can be regarded as a solution for controlling DC microgrid in terms of current sharing, power sharing and average voltage regulation.

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15. Appendix

15.1 System overview

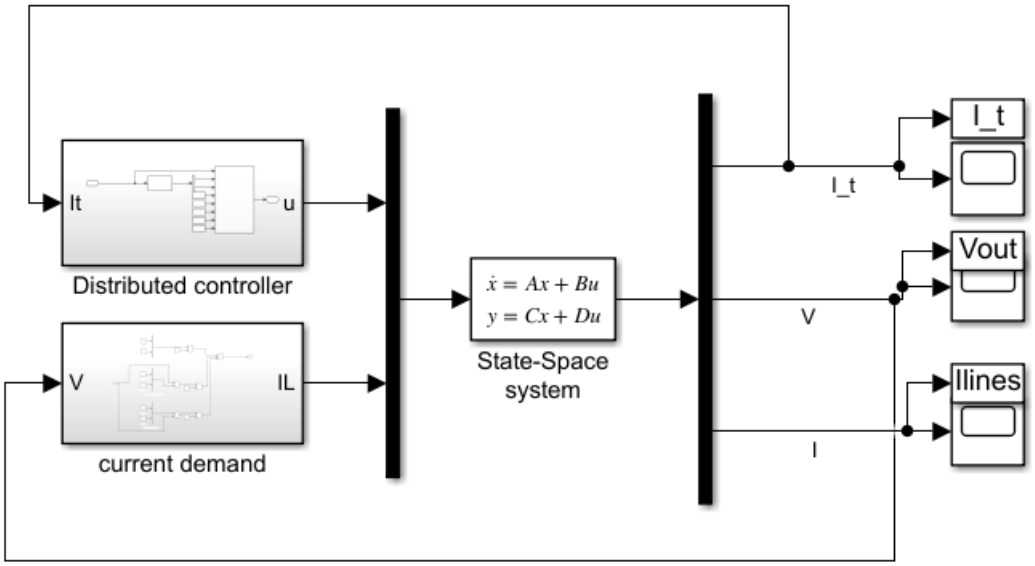

Figure 15.1: An overview of the model used in Simulink

15.2 ZIP-load structure

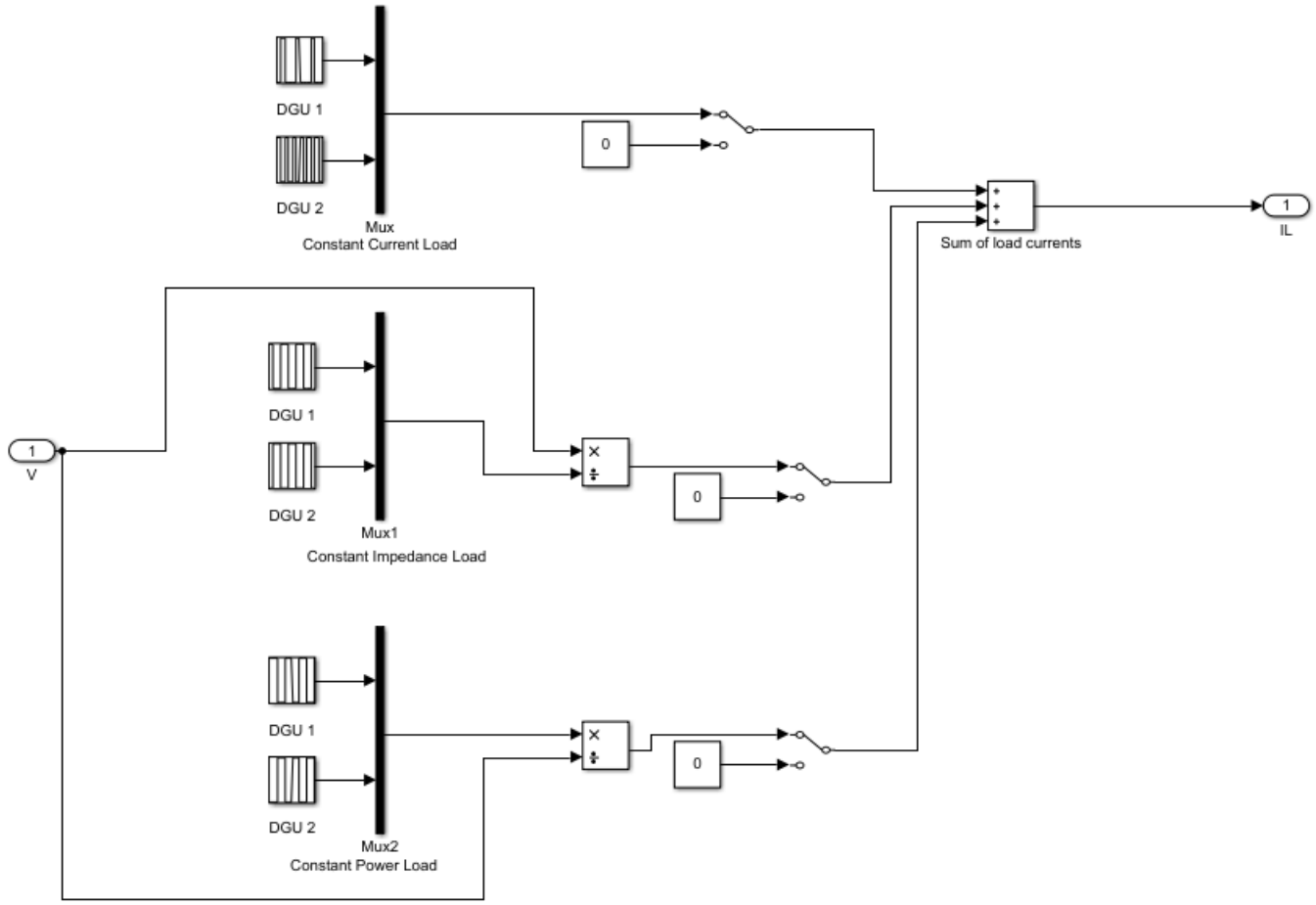

Figure 15.2: A visualization of the ZIP-loads into the Simulink model displayed in figure 15.1

15.3 Distributed controller structure

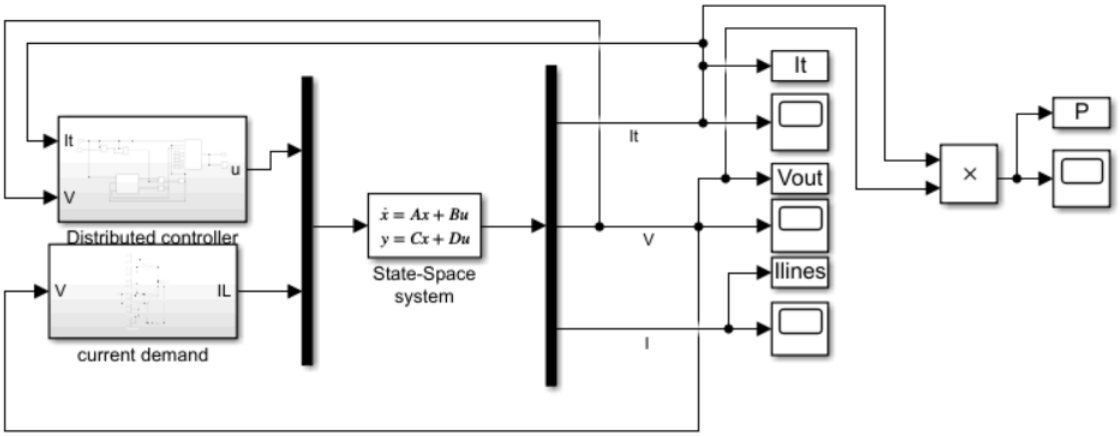

Figure 15.3: The distributed controller in the Simulink model