University of Groningen

Final Bachelor Degree Project

Properties and Neuromorphic Applications of Co/Nb:STO based Memristors

Computing Beyond von Neumann

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Abstract

The Role of Co/Nb-doped $SrTiO_3$ in Neuromorphic Computing

Neuromorphic computing aims to fabricate memory devices capable of mimicking the structure of neurons and synaptic connections in the brain. This approach allows for the co-localization of memory and information processing functionalities, overcoming the efficiency limitations of traditional computing associated with the von Neumann bottleneck and the slowdown of Moore's Law. The objective of this research was to fabricate and study the electrical properties of Cobalt and Niobium-doped Strontium Titanate (Co/Nb:$SrTiO_3$) junctions with interface-based memristive properties, and to discuss their role as embedded-memory systems in the context of neuromorphic computing. To this end, the devices were fabricated using electron beam lithography techniques and electrically characterized using the Keysight B1500A Semiconductor Device Analyze. The results show that the fabricated Co/Nb:$SrTiO_3$ devices exhibit low device-to-device variation, the ability to enhance their capabilities when miniaturized, non-binary memory states, and the capacity to modulate their conductance through current potentiation and depression. All these conditions are highly beneficial for neuromorphic applications and the development of biological sensors. However, certain limitations related to response speed and destructive readout of states require further investigation.

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Chapter 1 Introduction

1.1 Background

The von Neumann architecture has proven to be highly significant as the main paradigm of traditional computing since its conceptualization in the mid-20th century [21]. This structure was designed with the purpose of storing both data and program instructions within the same memory space [26]. In this way, both types of information could be written in binary code, allowing the computer to process them efficiently without the need for manual hardware modifications. The simplicity, speed, and versatility of this architecture have led to its widespread adoption in all commercial computers from its initial implementation to the present day.

Nevertheless, the constant demand for the evolution and improvement of computing devices has highlighted the inherent inefficiencies of this type of architecture. In conventional computers, the components responsible for memory storage are physically separated from the central processing unit (CPU), which is in charge of interpreting, processing, and executing instructions encoded in software programs [7]. The fact that these two functions are virtually separated allows for data to be fetched and processed only in a sequential manner, requiring a mechanism capable of transferring information from memory to the CPU. This is achieved through buses, which provide a transmission channel to facilitate data transfer, but this comes at the cost of increased energy consumption. Moreover, processing speed is significantly lower compared to the rate at which data can be transferred from memory. This limits the overall throughput of the device, which could potentially deliver higher performance than it does due to the constraints imposed by its architecture [9], [22].

These limitations in energy and time efficiency are known as the von Neumann bottleneck, representing one of the main challenges to overcome in the context of modern computing. Additionally, the exponential reduction in the size of electronic components, as described by Moore's Law, is beginning to reach its limits. Several microprocessor manufacturers have stated that the miniaturization of CMOS-based transistors in a cost-effective manner is already slowing down, which means that performance improvements driven by size reduction will also significantly decline in the coming years [6].

In light of this situation, there is a growing need to develop a new computational paradigm capable of overcoming the limitations associated with the von Neumann bottleneck and the physical constraints of electronic component size. In this regard, neuromorphic computing emerges as one of the most promising options for the future of computing. This novel approach aims to replicate the operational principles of the human brain in terms of information storage, cognition, and processing. The structure of the brain provides memory functions through synaptic connections formed by an extensive neural network, while neurons are responsible for processing. In this way, both functions are co-located, allowing humans to manage large amounts of information in parallel, rapidly and with extremely low energy consumption [2], [27]).

Artificial neuromorphic systems aim to simulate neural networks with synaptic interconnections using memory devices and processors. In this context, new materials with potentially optimal properties are being investigated for their possible application in brain-inspired computing systems. Among these, memristors have emerged as particularly promising due to their unique characteristics, making them increasingly important components in neuromorphic architectures. In this research project, the properties of Nb-doped $SrTiO_3$ (Nb:STO), a doped oxide perovskite, are explored. To this end, various devices composed of Co/Nb:STO were tested, and their potential computational applications were discussed.

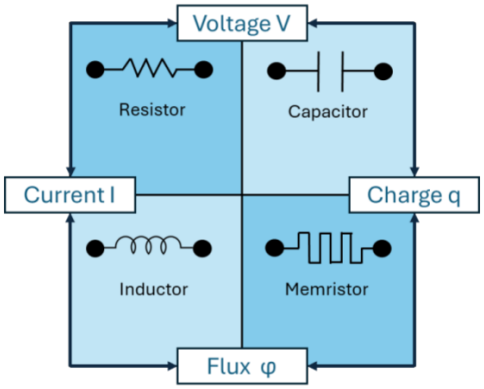


Figure 1.1.1: The four fundamental circuit elements

1.2 Memristors

Classical electronics is fundamentally built upon three basic passive components: the resistor (1827), the capacitor (1745), and the inductor (1831). Each of these elements is defined by its ability to relate the four fundamental electrical quantities: charge, current, voltage, and magnetic field [33]. These relationships are illustrated in Figure 1.1.1.

However, this definition is controversial because it was stated without experimental corroboration. Instead, since their first physical realization by HP Labs in 2007 [14], memristors are characterized by their ability to exhibit nonlinear resistance depending on the polarity, magnitude, and duration of the applied voltage. Based on these parameters, memristors can display different behaviors in terms of their opposition to electric current, alternating between various resistance states in a process known as resistive switching. The presence of these distinct states becomes evident in the typical I/V characteristic of memristors, where a pinched hysterectic current loop appears, featuring two distinct branches associated with each resistance state (see Figure 1.2.1) [5].

Although the exact physical phenomena involved in the resistive switching processes of memristors remain unknown, two main types can be distinguished based on the origin of the resistance state changes: unipolar and bipolar switching.

Thermal excitation plays a major role in the resistance state changes of non-conducting memristors with unipolar resistive switching, which are typically composed of two metal electrodes separated by a dielectric material [18]. Due to soft voltage breakdowns of the dielectric, small fragments of metal can be released and penetrate into the insulating material. This leads to the formation of conductive filaments that bridge both electrodes, thereby increasing the overall permittivity of the memristor. Through local Joule heating, oxygen ion migration, and Mott transitions, the formation of these filaments is facilitated, allowing the device to reach a lower resistance state (LRS). Once the LRS is set, the high resistance state (HRS) can be reset by destroying the conductive filaments, returning the device to more stable, lower thermal conditions. Thus, the resistance switching in unipolar memristors is reversible, although it has been observed that the resistance values do not return to those of the material's pristine state.

On the other hand, bipolar resistive switching occurs in oxide memristors connected to a metal electrode [5]. In this case, the primary factor influencing resistance state changes is the polarity of the applied voltage. These changes originate from local modifications in the interfacial layer structure between the two materials, which involve oxygen vacancy migration, major carrier transport, and, most importantly, the trapping and

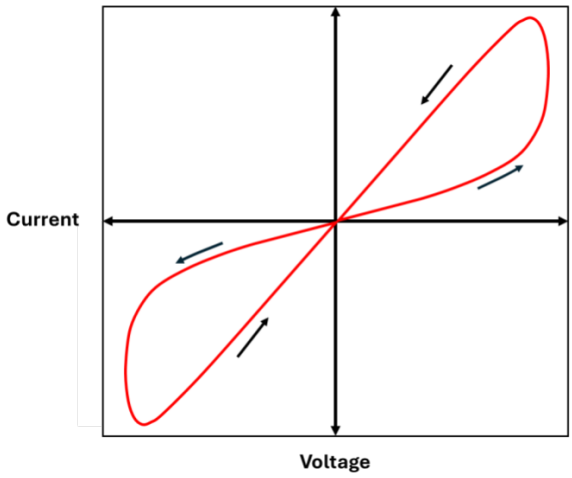


Figure 1.2.1: Typical I/V characteristics of a memristor

detrapping of charges. All of these mechanisms are driven by electrical effects, which alter the potential barrier opposing current flow and can either facilitate (LRS) or hinder (HRS) the passage of current through the interface.

In this thesis, the memristive behavior of Co/Nb:STO is examined. Its structure is defined by the combination of a metal (Co) and a semiconducting oxide perovskite (Nb:STO). Consequently, the dominant mechanism behind the resistance state transitions in this device is bipolar resistive switching, resulting from structural changes at the formed interface. The growing interest in this material for neuromorphic computing is justified by its ability to simulate synaptic plasticity through memristive switching, enabling local information storage and updating in a manner analogous to the functioning of synaptic weights.

Moreover, Nb:STO supports in-memory computing and helps overcome the von Neumann bottleneck, as it can both store data in different resistance states and perform computation (such as matrix-vector multiplication) within the same physical location. However, a detailed understanding of the physical phenomena involved in resistance state changes in this type of memristor remains crucial for drawing conclusions about its properties and potential applications. This remains the most significant challenge in memristor research.

1.3 Nb-doped $SrTiO_3$

Oxide perovskites are materials that exhibit a general crystalline structure consistent with the chemical formula ABO_3, where A represents an alkali or alkaline earth metal, and B refers to a transition metal [3]. Regarding the spatial arrangement of these elements within the simple cubic lattice of perovskites, the B-site cation is located at the center of the cube (0, 0, 0), while the A-site cations are positioned at each of the cube's corners (1/2, 1/2, 1/2). Oxygen atoms occupy the centers of the cube faces (1/2, 1/2, 0).

The various particles that make up the general structure of oxide perovskites each play a specific role that influences the overall properties of the bulk material [37]. The A-site element acts as a large-radius cation, donating electrons and contributing to the thermodynamic stability of the structure. The B-site cations, which have smaller ionic radii, are responsible for regulating electrochemical reactions. However, the critical magnetic and electrical conductivity properties of these materials originate from the presence of oxygen within the lattice structure, as it forms the bonds between B-site atoms of adjacent lattices. This is because the modulation of the band structure in oxide perovskites largely depends on the orbital hybridization state present in the B–O–B bonds.

The material $SrTiO_3$ (STO) exhibits an almost ideal stoichiometry at room temperature, with a face-centered

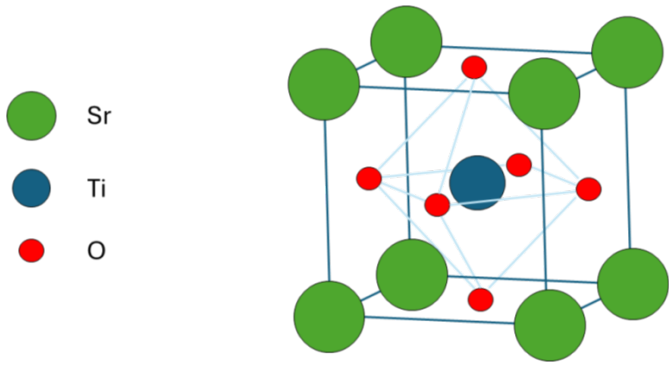


Figure 1.3.1: Three dimensional cubic lattice of $SrTiO_3$

simple cubic oxide perovskite structure. The lattice constant of bulk STO is 3.928 Å, its indirect band gap is 3.27 eV, and its electron affinity is 3.9 eV) [29]. Additionally, its high dielectric constant defines its insulating behavior under normal environmental conditions, reflecting a polar nature and low electrical conductivity in the presence of an electric field.

However, recent studies have shown that the dielectric constant of STO (ε_r) is highly dependent on variations in temperature and electric field strength [31]. This is due to phase transitions to lower symmetry configurations, which promote oxygen non-stoichiometry and alter the electrical properties of STO. The relationship between these quantities is described by the Barrett formula [15]:

$$\varepsilon_r(T,E) = \frac{b(T)\varepsilon_0}{\sqrt{a(T+E^2)}}, \tag{1.3.1}$$

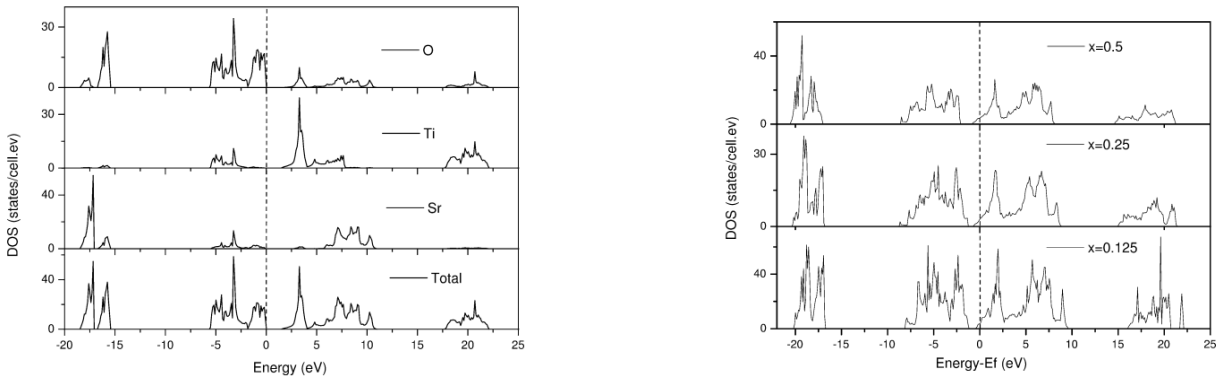
where ε_0 is the vacuum permittivity, and $b(T) = (1.3710^7 + 4.2910^7)(\frac{T}{100})$ and $a(T) = a(T) = b(T)/\varepsilon_r(T,0)\frac{b(T)}{\varepsilon_r(T,0)}$. The dielectric permittivity of the material under zero electrical field is given by:

$$\varepsilon_r(T,0) = \frac{1635\varepsilon_0}{coth(\frac{44.1}{T}) - 0.937}. \tag{1.3.2}$$

The formula predicts a decrease in the dielectric constant of $SrTiO_3$ with increasing temperature. It aligns well with experimental results under moderate electric field conditions, where the dielectric permittivity saturates due to quantum fluctuations. However, under high electric field conditions, experimental measurements deviate from the relationship described by the Barrett formula [24].

All these properties, combined with its high melting point, low dielectric loss, low leakage current, and high Seebeck coefficient, have generated significant interest in this material [36]. $SrTiO_3$ is regarded as a universal substrate for epitaxially growing other oxides, as well as an active component in oxide heterostructures, demonstrating strong potential for applications in data storage and neuromorphic computing.

For this research, the oxide-based memristor is fabricated on a thin film of Nb-doped $SrTiO_3$ substrate, which alters the original stoichiometry responsible for the insulating properties of pristine STO. Niobium atoms partially substitute the titanium cations located at the B-sites of the crystal lattice, resulting in a



(a) DOS of $SrTiO_3$ **(b)** DOS of Nb:$SrTiO_3$

Figure 1.3.2: Comparison of the Density of States of $SrTiO_3$ and Nb:$SrTiO_3$ for different doping concentrations [36].

composition of $SrTi_{1-x}Nb_xO_3$. While Ti^{4+} cations contribute four electrons to the overall structure of the strontium-based perovskite, Nb^{5+} cations act as n-type doping agents, donating five electrons. This creates an artificial electronic imbalance, which is compensated by introducing one free electron into the conduction band for each Nb^{5+} ion added. With a sufficiently high dopant concentration, STO can exhibit behavior characteristic of an n-type semiconductor, where the Fermi level is shifted toward the conduction band.

Previous studies conducted by the Spintronics of Functional Materials research group have demonstrated some of the properties of Nb:STO that justify the growing interest in this material for computational applications [15], [11], [10], [30]. Unlike conventional semiconductors, the carrier concentration in Nb:STO remains nearly constant despite variations in temperature. The high dielectric permittivity of STO, even at very low temperatures, explains niobium's ability to remain ionized under these conditions, since the binding energy is inversely proportional to the square of the permittivity. This relationship is expressed by the following formula:

$$E_D = -13.6eV(\frac{m_e^*}{m_e})(\frac{1}{\varepsilon_{r^2}}), \tag{1.3.3}$$

where m_e^* represents the effective mass of the electrons and m_e denotes the mass of a free electron. The binding energy is minimal under very low temperature conditions, which means that Nb behaves as a shallow donor, requiring little energy for its ionization in such conditions. This favors the absence of freeze-out and results in a carrier concentration that is independent of temperature [4].

In contrast, the mobility of carriers in Nb:STO increases significantly as the temperature decreases. Furthermore, if the Nb doping concentration is sufficiently high, the oxide heterostructure can become a degenerate semiconductor capable of exhibiting metallic behavior. When these two parameters are properly exploited, it is possible to induce a superconducting transition, which highlights the remarkable versatility of Nb:STO and the wide range of functionalities it can offer in various applications [32].

1.4 Scope and Structure

The purpose of this research is to investigate the properties of Co/Nb:STO and evaluate its potential as a key material in the development of neuromorphic computing devices. In particular, the study explores the effects of device miniaturization down to 300 nm, on its I/V characterization, as well as device-to-device variability, endurance, retention characteristics, and transient behavior. Additionally, a theoretical model is proposed to account for the physical mechanisms underlying the resistance state changes observed in Co/Nb:STO.

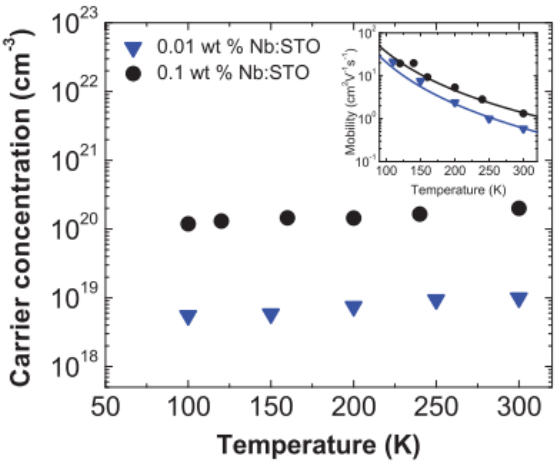


Figure 1.3.3: Temperature dependence of carrier concentration and mobility for 0.01 and 0.1 wt % Nb doped $SrTiO_3$ in the temperature range from 100 K to 300 K [30].

To this end, the theoretical principles related to the memristive behavior of the material are presented in Chapter 2. The fabrication process of Co/Nb:STO, carried out at the Nanolab Groningen facilities, is described in detail in Chapter 3, along with the methods employed for the electronic characterization of these devices. Chapter 4 presents the experimental results and their subsequent discussion. Finally, Chapter 5 summarizes the conclusions drawn from the analysis of the results.

Chapter 2 Theoretical Background

Once the metal/n-type semiconductor contacts are formed in the Co/Nb:STO memristor, the characteristic potential barrier of such heterojunctions is established. The higher work function of cobalt (5 eV) [12]compared to that of the semiconductor (4.2 eV) [25] results in the formation of a Schottky contact, which accounts for the electrical characteristics of the device. This section discusses the formation process of the Schottky barrier, its variations under voltage bias, the mechanisms involved in carrier transport through the barrier, and the resistive switching theory underlying the memristive behavior of Co/Nb:STO [34], [19].

2.1 Schottky Barrier Formation

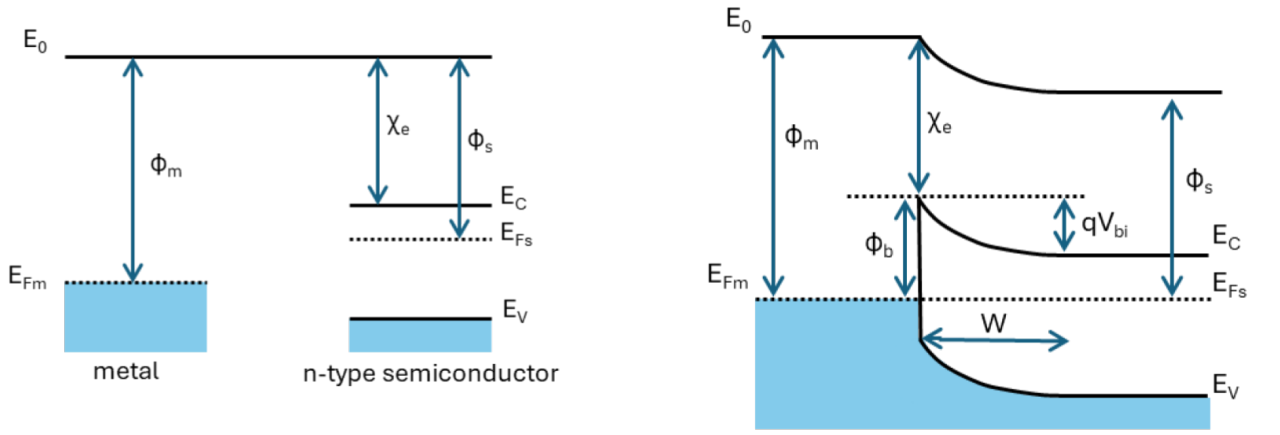
Before the materials come into contact, the energy band profiles of each are configured as shown in the diagram in Figure 2.1.1a. The Fermi energy corresponds to the highest energy level at which the probability of finding an electron is fifty percent at absolute zero temperature (0 K). All energy levels below this point are fully occupied by carriers, while those above remain empty. The work function values are specific to each material and determine the position of their respective Fermi levels. In this case, the work function of Co is greater than that of Nb:STO, meaning that the Fermi level of the metal initially lies lower than that of the semiconductor, fulfilling a fundamental condition for the formation of a Schottky barrier in such contacts. Furthermore, the position of the Fermi level in the semiconductor relative to the conduction and valence bands depends on the carrier concentration. Since we are dealing with an n-type semiconductor, the concentration of free conduction electrons in the conduction band is higher, which explains the Fermi level being located near the conduction band.

Once contact between both materials is established, the Fermi levels tend to align in order to reach thermodynamic equilibrium, which alters the overall band profile, as shown in the Figure 2.1.1b. This energy level shift is caused by the migration of majority carriers across the junction. Electrons from the semiconductor, having a higher electrochemical potential, naturally flow toward lower potential states in the metal. However, since the metal side has an extremely high electron density, its Fermi level remains essentially unchanged when a small number of electrons are added or removed. Therefore, the equilibrium is reached primarily through the adjustment of the semiconductor's Fermi level.

As electrons leave the semiconductor, they leave behind positively charged fixed dopants, which generate an electric field at the junction interface. This newly formed field opposes the initial electron flow, creating a depletion region near the semiconductor interface that reduces the mobility of the majority carriers. As a result, the conduction and valence bands of the semiconductor bend upward near the interface, and a potential barrier is formed that limits electron flow toward the metal. This potential difference is known as the Schottky barrier.

The height of the Schottky barrier at equilibrium ($e\phi_b$), relative to the equilibrium Fermi level, depends on the metal's work function and the electron affinity of the semiconductor, which defines the energy required to release an electron from the conduction band. This characterization of the Schottky barrier opposes the movement of majority carriers from the semiconductor and is described by the Schottky-Mott relation:

$$e\phi_b = e\phi_m - e\chi_s, \tag{2.1.1}$$



(a) Before junction

(b) After junction DOS of $Nb:SrTiO_3$

Figure 2.1.1: Energy band diagram of a metal and an n-type semiconductor junction before and after contact.

where ϕ_m is the workfunction of the metal, χ_s is the electron affinity of the semiconductor, and e the elementary charge.

On the other hand, the built-in potential (V_{bi}) resulting from the shift in the Fermi levels is determined by the difference between the work functions of the two materials and is associated with the change in the semiconductor's Fermi level from its initial position during alignment. This potential represents the effective barrier that electrons originating from the semiconductor experience as they traverse the interface toward the metal side.

$$eV_{bi} = e\phi_m - e\phi_s, \tag{2.1.2}$$

where ϕ_s is the workfunction of the semiconductor.

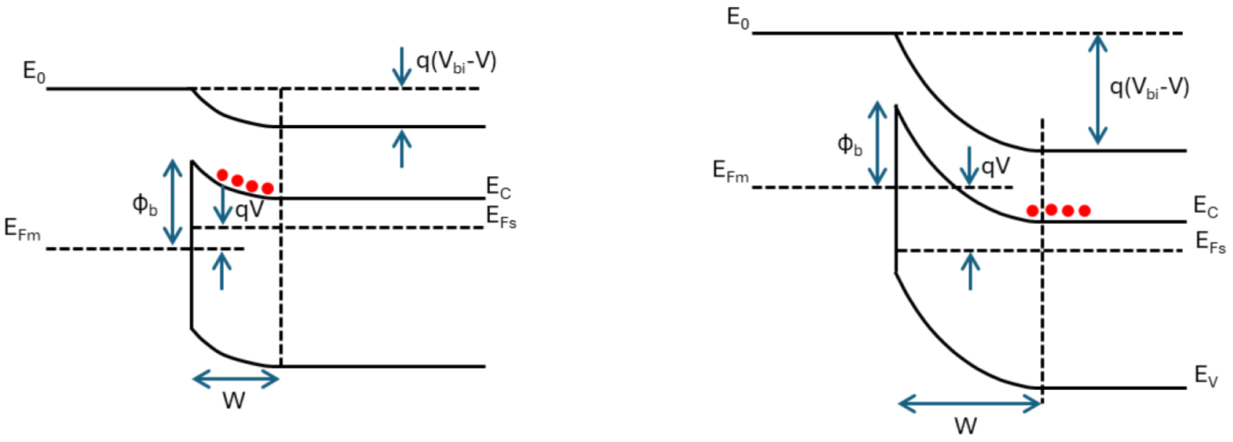
In such cases, the potential barrier associated with the built-in potential is generally lower than the Schottky barrier. This difference, along with the unequal electron concentrations on each side of the metal/semiconductor junction, enables the system to reach thermodynamic equilibrium. The depletion region also plays a crucial role in this balance; its width depends on the dielectric permittivity of the semiconductor, the donor concentration, and the built-in voltage.

$$W = \left(\frac{2\varepsilon(V_{bi} - V)}{eN_d} \right)^{1/2}, \tag{2.1.3}$$

where N_d is the donor concentration.

2.2 Schottky Barrier Under Bias

Both the width of the depletion region and the value of the built-in effective potential barrier, as described in equations 2.1.2 and 2.1.3, can be modified by applying an external voltage. Depending on the polarity of this voltage, different structural changes can be induced in the energy band profile of the heterojunction, which may enhance the flow of current across the interface in a specific direction. In this context, two distinct cases can be identified: forward bias and reverse bias.



(a) Forward Bias

(b) Reverse Bias

Figure 2.2.1: Energy band diagram of a Schottky contact under forward and reverse bias.

When a negative bias V is applied to the semiconductor side of a Schottky junction and a positive bias to the metal side, the applied voltage corresponds to the forward bias regime. In this case, all the energy levels of the semiconductor, including its Fermi level, are shifted upward, and become higher with respect to the Fermi level of the metal. According to equation 2.1.3, the width of the depletion region is reduced compared to its configuration at equilibrium. Additionally, since the work function of the semiconductor also decreases, the effective potential barrier (ϕ_b^{eff}) associated with the built-in potential is reduced relative to its height in the equilibrium state, and takes the following form:

$$\phi_b^{\text{eff}} = \phi_b - V. \tag{2.2.1}$$

All of this results in an increase in the forward current from the semiconductor to the metal, as the depletion region and the effective potential barrier offer less resistance.

On the other hand, the reverse regime is achieved by applying a negative bias to the metal side and a positive bias to the semiconductor side. In this way, the Fermi Level of the semiconductor and its energy bands become lower relative to the Fermi Level of the metal. Under these conditions, equation 2.1.3 predicts an increase in the depletion region of the Schottky contact, pushing the conduction band electrons further away from the interface. Due to the downward shift of the Fermi Level, the effective potential barrier increases significantly, further hindering current flow in the forward direction. The height of the new potential barrier is:

$$\phi_b^{\text{eff}} = \phi_b - V, \tag{2.2.2}$$

where V now gets negative values and the effective potential barrier is increased.

However, as the Fermi level of the semiconductor decreases, the Schottky barrier becomes steeper and thinner. When the energy of the conduction band becomes sufficiently lower compared to the Fermi energy of the metal, the probability of electrons tunneling through the potential barrier increases, thereby enhancing the current in the reverse direction.

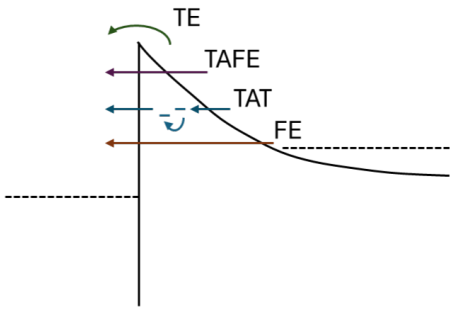


Figure 2.2.2: Diagram of the carrier transport mechanisms

2.3 Carrier Transport

When a potential difference is applied across the Schottky contact, the structural changes in the band profile discussed in the previous section explain the rectifying behavior of this type of heterojunctions, allowing current to flow in a specific direction. Depending on the polarity of the voltage bias, current can flow either from the semiconductor to the metal in a forward bias scheme, or from the metal to the semiconductor in a reverse bias regime.
The electric current arises from the movement of carriers overcoming the Schottky barrier across the interface, which is governed by the mechanisms of Thermionic Emission and Tunneling as shown in Figure 2.2.2.

2.3.1 Thermionic Emission

Thermionic emission refers to the movement of charge carriers over the Schottky barrier due to their own thermal energy. Only those electrons with sufficient energy to overcome the potential barrier are able to move from one side of the junction to the other through this mechanism. Assuming that the Schottky barrier height is significantly higher than the thermal energy under ambient conditions ($\mathrm{k}_B\mathrm{T}$), and that thermal equilibrium at the interface remains unchanged despite the net current flow, the current density in the forward direction from the semiconductor to the metal is given by the Thermionic Emission Equation:

$$J_{s\to m} = A^* T^2 \exp\left(-\frac{e\phi_b}{kT}\right) \exp\left(\frac{eV}{kT}\right), \tag{2.3.1}$$

where J is the current density, k_B is the Boltzmann constant, and T the temperature. A^* is defined as the Richardson-Dushman constant and represents a material-dependent parameter related to the transmission rate due to thermionic emission. The expression for this constant is:

$$A^* = \frac{4\pi e m_e^* k^2}{h^3}, \tag{2.3.2}$$

where, m_e^* corresponds to the effective mass of the electrons, and h is the Planck constant. In the case of Nb:STO, the value of the Richardson constant is 156 $Acm^{-2}K^{-2}$.

In the expression for the current density in the forward direction, the applied voltage is taken into account, as the effective potential barrier for carriers on the semiconductor side can be modified under bias. However,

the potential barrier opposing the flow of charge in the reverse direction from the metal to the semiconductor is voltage-independent, since the Fermi level of the metal remains fixed. Therefore, the current density in the reverse direction can be obtained from Equation 2.3.1 by setting V = 0, resulting in:

$$J_{m\to s} = -A^* T^2 \exp\left(-\frac{e\phi_b}{kT}\right). \tag{2.3.3}$$

By summing the contributions in both directions, the net current density due to thermionic emission is given by:

$$J_{TE} = A^* T^2 \exp\left(-\frac{e\phi_b}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right) - 1\right], \tag{2.3.4}$$

where an ideality factor n is included. This factor equals one in the case of ideal thermionic emission. However, if defects are present in the heterojunction or if other mechanisms are involved in carrier transport across the interface, n will take values greater than 1. These additional transport mechanisms are typically associated with tunneling processes.

2.3.2 Tunneling

Tunneling encompasses all carrier transport mechanisms in which electrons are able to pass through an energy potential barrier via this quantum phenomenon. These processes allow electrons to cross from one side of the interface to the other, even when they lack the energy required to overcome the potential barrier in a classical manner as is the case in thermionic emission. When electrons with minimal energies near the Fermi level tunnel through the barrier, the mechanism is referred to as Field Emission. However, the tunneling phenomenon can also be facilitated by the thermal excitation of these electrons to higher energy levels, where the effective potential barrier becomes narrower and the likelihood of crossing via Thermally Assisted Field Emission increases. Both Field Emission mechanisms are strongly quantum in nature and are highly sensitive to changes in doping concentration and temperature, which significantly influence the potential barrier profile.

A comprehensive description of the current density across the Schottky barrier, which includes tunneling contributions from field emission and thermally assisted field emission, is provided by the Padovani and Stratton model, whose expression takes the form:

$$J_{\mathrm{T}} = \frac{q^3 E^2}{8\pi h \phi_b} \exp\left(-\frac{8\pi\sqrt{2m^*}\phi_b^{3/2}}{3qhE}\right), \tag{2.3.5}$$

where, h refers to the Planck constant, E is the electric field strength, and q is the charge. This model assumes specific conditions of low temperature and high doping, highlighting the complexity of developing a mathematical expression that accurately describes the tunneling effect across the barrier and remains broadly applicable.
Equation 2.3.5 incorporates both tunneling mechanisms discussed; however, the current density associated with each can be defined separately. In the case of field emission transport, the expression is given by:

$$J_{FE} = \frac{A^{**} T\pi}{c_1 k \sin(\pi c_1 kT)} \exp\left[\frac{e(\phi_b - V)}{E_{00}}\right] \quad \text{with} \quad c_1 \equiv \frac{1}{2E_{00}} \log\left[\frac{4(\phi_b - V)}{-\xi}\right]. \tag{2.3.6}$$

The expression for the fraction of current density associated with thermally assisted field emission is:

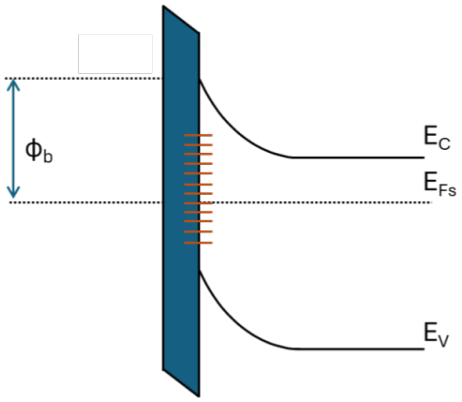


Figure 2.3.1: Interfacial layer and trapping states in non-ideal Schottky contact.

$$J_{TAFE} = \frac{A^{**}T\sqrt{\pi E_{00}e(\phi_b - \xi - V)}}{k\cosh(E_{00}/kT)} \exp\left[\frac{-e\xi}{kT} - \frac{e(\phi_b - \xi)}{E_0}\right] \exp\left(\frac{eV}{E_0}\right), \tag{2.3.7}$$

where $E_0 \equiv E_{00}\coth\left(\frac{E_{00}}{kT}\right)$.

In order to determine which of the discussed carrier transport mechanisms is dominant under specific temperature and doping conditions, the characteristic energy parameter E_{00} is defined. Its expression is:

$$E_{00} = \frac{e\hbar}{2}\sqrt{\frac{N_d}{m_e^*\epsilon_r}} \tag{2.3.8}$$

where $\hbar$ is the reduced Planck constant. By comparing this energy parameter with the average thermal energy available to electrons at a given temperature, expressed as k_BT, it is possible to determine which of the three transport mechanisms contributes most significantly to carrier transport. If E_{00} is much smaller than k_BT ($E_{00} < k_BT$), simple field emission is the dominant process. Conversely, if E_{00} is much greater than k_BT ($E_{00} > k_BT$), thermally assisted field emission becomes the prevailing mechanism. If E_{00} is approximately equal to k_BT ($E_{00} \simeq k_BT$), then thermionic emission is the primary transport mechanism across the barrier, taking precedence over tunneling.

However, this parameter only accounts for direct band-to-band transport mechanisms. In the Schottky junction formed by oxide perovskites, such as the interface between Co and Nb:STO, another highly relevant transport process involves energy states present at the interface. This phenomenon is known as Trap Assisted Tunneling, and it plays a crucial role in the switching and distinction between the two characteristic resistance states in memristive materials.

2.3.3 Resistive Switching by Trap Assisted Tunneling

In the derivations obtained in previous sections, the formation of an ideal Schottky contact was considered, where materials come into contact in a perfect vacuum and are free of defects and impurities. Although this approach allows for the correct prediction of variations in the Schottky barrier profile and the approximate current behavior, numerous non-ideal agents modify these derivations. These irregularities are key to understanding the operation of Co/Nb:STO contacts.

During the fabrication process of Co/Nb:STO memristors, it's crucial to consider numerous impurities related to the surface energy of the semiconductor material and its characteristics. First, oxide perovskites

very commonly show a high level of oxidation on their surface. This can generate a very thin interfacial layer between the metal-semiconductor junction with insulating properties. This new feature in the non-ideal Schottky contact modifies its energy band profile as shown in Figure 2.3.1.

The presence of this insulating layer causes an additional voltage drop of the built-in potential across it. As a result, there's a deviation from the ideal Schottky-Mott limit, where the Schottky barrier is determined solely by the metal's work function and remains constant. In this case, the effective Schottky barrier that charges experience becomes bias-dependent and can be altered.

Additionally, Nb:STO has numerous oxygen dangling bonds on its surface. The presence of these incomplete surface terminations during the fabrication of the heterojunctions creates a series of interface states capable of trapping charges moving from side to side. This transport mechanism, where carriers can tunnel between both sides of the Schottky contact through these trapping states, is called Trap-Assisted Tunneling. Although the density of interface trap states depends on the cleaning, preparation, and fabrication processes, their formation is mainly due to the stoichiometric properties of the Nb:STO material, representing a structural consequence in the development of these memristive devices.

The occupation of trapping states at the interface by electrons is governed by the Fermi-Dirac distribution for fermions. Thus, since all energy levels located below the Fermi Level are fully occupied, the same rule applies to the trapping states. Consequently, in the Co/Nb:STO Schottky junction, the trapping and detrapping of carriers at the interface states largely depend on the Fermi Level's position, which can be modulated by applying a voltage bias.

When a forward bias is established from equilibrium, the semiconductor's quasi-Fermi level moves closer to the conduction band, increasing the probability that electrons moving from the semiconductor to the metal will be trapped at the interface. The trapped carriers cannot contribute to the generated current, leading to a high resistance state (HRS). Conversely, when the voltage polarity is switched and the forward bias is reduced to equilibrium, the Fermi level returns to its initial position. During this process, the charges previously trapped at the interface begin to release and reach the metal side, enhancing the resulting current and switching to a low resistance state (LRS). If the voltage continues to decrease and a reverse bias is applied, the semiconductor's Fermi level will continue to drop, approaching the valence band. The number of available interface states under these conditions remains very high, facilitating the transport of carriers from the metal to the semiconductor via trap-assisted tunneling. This, combined with the reduced width of the Schottky barrier, results in low resistance, and the LRS is maintained. Finally, if the voltage polarity is reversed again, the Fermi level will start to rise from the valence band and return to its equilibrium state, favoring the occupation of the states present at the interface. This reduces the number of available states for trap-assisted tunneling, thereby increasing the resistance to current flow in the reverse direction. The HRS is thus re-established.

This voltage-controlled modulation of the trapping states' occupation provides the foundation for the memristive behavior of Co/Nb:STO, in which two well-defined resistance states can be interchanged through bipolar resistive switching mechanisms. The voltage values at which the High Resistance State (HRS) is switched to a Low Resistance State (LRS) are referred to as SET voltages. Conversely, the voltage values at which the LRS is switched back to the HRS are known as RESET voltages. Although this model makes it possible to explain the electrical properties of the device under test, it remains a basic conceptualization of the complex physical processes involved. Yet, it remains useful for the development of this research work.

Chapter 3 Methodology

The memristive properties of Co/Nb:STO are largely attributed to the crystal structure of the materials and to the inherent imperfections present on their surfaces. Therefore, it is crucial to design a precise and rigorous fabrication process that enables the creation of functional devices capable of exhibiting the desired response during their electrical characterization. This section outlines the steps carried out in the cleanroom for the fabrication of the Co/Nb:STO contacts, as well as the methods employed during their testing using the Keysight B1500A Device Analyzer [1].

3.1 Device Fabrication

3.1.1 Sample Preparation

TiO_2 Single Terminated Surface

The substrate of the fabricated device consists of Nb-doped $SrTiO_3$ with a donor concentration of 0.01 wt% Nb. Depending on the crystal structure of oxide perovskites, it is possible to observe the surface of $SrTiO_3$ entirely covered by terminations of a single type, corresponding to a thin oxidation layer formed either by SrO or TiO_2. However, the crystal structure of the material provided by the supplier exhibits a mixed-terminated layer, composed of a combination of both types of terminations mentioned above. Although this structure provides greater thermodynamic stability, a single termination on the surface of the perovskite enables the construction of (111)-oriented $SrTiO_3$ with more functional physical properties and more homogeneous interfaces [28]. Since a single TiO_2-terminated layer features greater energetic stability, the surface structure of Nb:STO was modified through a controlled selective chemical wet etching process, taking advantage of the different etching rates of the Sr and Ti terminations [20].

First, the substrate is cleaned using successive ultrasonic baths filled with acetone, ethanol, and isopropanol. Cleaning occurs when the sound waves agitate the solvent-based liquid, causing cavitation or bubbling of the impurities and contaminants present on the surface. The resulting molecular explosions generate enough force to dislodge dirt and other contaminants from the surface of the immersed substrate. Once the solvent baths are completed, the substrate is again submerged and ultrasonicated in deionized (DI) water for 30 minutes to complete the cleaning process. In this way, the SrO terminations are hydroxylated, leading to the formation of $Sr(OH)_2$.

$$SrO + H_2O \rightarrow Sr(OH)_2$$

In order to remove the $Sr(OH)_2$ and obtain a TiO_2-terminated surface, the substrate is etched with buffered HF acid for 30 seconds.

$$Sr(OH)_2 + BHF \rightarrow Sr^{2+} + 4\,F^- + 2\,H_3O^-$$

Once the process is completed, the sample is ultrasonicated in DI water one final time, cleaned with ethanol, and dried with N_2.

Thermal Annealing

Thermal annealing consists of removing any remaining cleaning agents previously used by controlling the temperature and adjusting the oxygen pressure. Additionally, the crystalline lattice of Nb:STO is restruc-

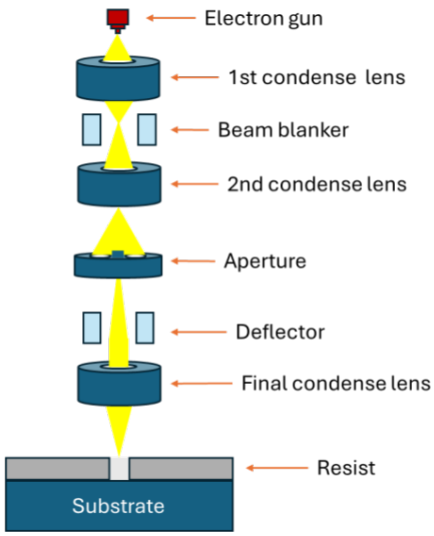


Figure 3.1.1: Typical structure of the optical column of an Electron Beam Lithography machine.

tured due to the diffusion and rearrangement of particles at the surface, which leads to a reduction in surface energy. For this purpose, the substrate is annealed at 960°C under an O_2 flow of 300 *cc* per minute. The duration of the process depends on the thickness of the substrate.

As a result of the annealing process, the surface of the material exhibits reduced roughness and more pronounced height variations, corresponding to well-defined stepped terraces.

Electron Beam Lithography

The fabrication of the Schottky contacts is based on the deposition of Co onto the Nb:STO substrate. To achieve this, the desired pattern is transferred using Electron Beam Lithography (EBL), a maskless fabrication technique used to write nanostructures by means of a focused beam of electrons (e-beam) directed at a resist-coated substrate. The resist material on top of the substrate is electron-sensitive, meaning its chemical composition and solubility can be altered through exposure to the electron beam. In this way, regions with different exposure levels can be selectively dissolved during the development process, as they become more or less soluble depending on the type of resist used and the intensity of the high-frequency e-beam. The electron beam can be focused to below 10 nm, making this technique not diffraction-limited and enabling fabrication with a high level of precision and accuracy [16].

The lithographic process is carried out using the Raith e-Line Plus system, which includes a column equipped with an electron gun capable of generating an electron beam with energies ranging from 20 eV to 30 keV ([16]). The system also incorporates various optical components such as lenses, aligners, and deflection coils, which control the position, alignment, and focusing of the e-beam. Additionally, a beam blanker is included to switch the e-beam on and off, enabling the transfer of the desired pattern onto the material without the need for masks.
The sample is placed on a mechanical stage, allowing for easy positioning under the e-beam. Figure 3.1.1 presents a general diagram of the column in an EBL system. All these components can be controlled computationally during the lithographic process, which must be conducted under high-vacuum conditions to prevent electron diffraction by air particles. The optimal pressure to achieve reliable results is approximately 510^{-7} mbar.

The high precision and accuracy of the EBL technique can be attributed to the high energy of the e-beam. In this experiment, the emitted electrons are accelerated to an energy of 10 keV. Using the de Broglie wavelength formula, $\lambda = \sqrt{(h/2mE)}$, the electron beam corresponds to a wavelength of 7.0810^{-3} nm, an

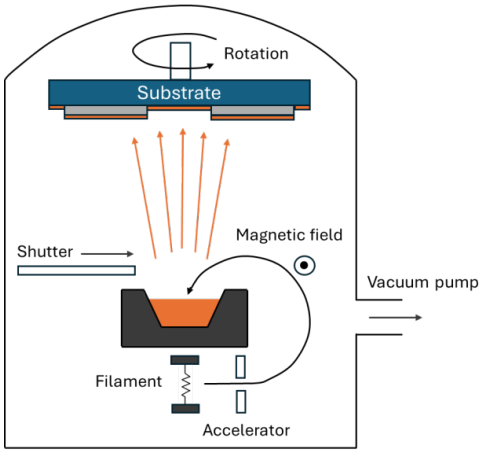


Figure 3.1.2: General setup of an electron beam evaporation machine.

extremely low value compared to other state-of-the-art lithographic techniques such as Extreme Ultraviolet Lithography (EUV) **??**.

As a result, the smallest possible feature size is not diffraction-limited; instead, the minimum beam spot size and the specific experimental procedure become the most critical factors. Furthermore, the photoresist material introduces an additional variable, as its composition can influence the number of scattering events, potentially reducing the overall resolution.

Electron Beam Evaporation

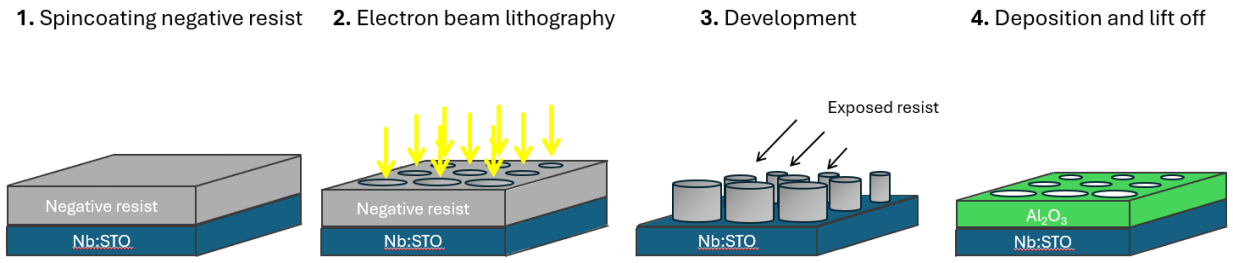
The deposition process of the material onto the sample is carried out via electron beam deposition, using the Temescal Thin Film Coater 2000 (TFC-2000) system. This physical vapor deposition technique enables the heating of materials with extremely high boiling points by means of a focused beam of high-energy electrons, properly directed using a magnetic field. The target material is placed in a water-cooled crucible inside a vacuum coating chamber. The substrate is positioned just above the source, allowing the evaporated particles to flow upward and adhere to its surface under high-temperature and low-pressure conditions.

The electron beam is rastered over a wider area of the target material rather than focusing on a single point, thereby avoiding localized overheating. To prevent undesired or accidental deposition on the sample, shutters are placed between the substrate and the source. These shutters function as gates that open only when the deposition rate, monitored by sensors integrated into the system, reaches a stable and constant value. The general layout of the components in the electron beam deposition system is shown in Figure 3.1.2. For optimal deposition without irregularities or defects, the process must be carried out under high vacuum conditions, typically around 1×10^{-6} mbar.

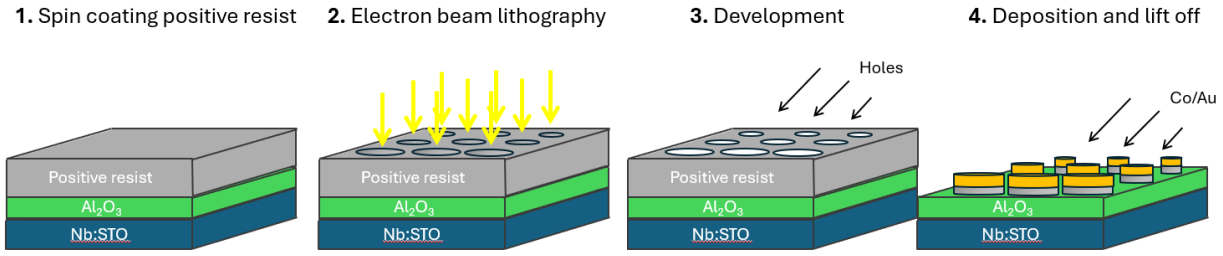
3.1.2 Experimental Procedure

Once the sample has been prepared, the fabrication of the Co/Nb:STO device consists of two lithographic processes using EBL, each followed by its respective development, deposition, and lift-off phases. Both steps are schematically illustrated in Figure 3.1.3.

The first EBL step (3.1.3a), involves transferring circular patterns of various sizes onto the substrate, in preparation for the subsequent deposition of insulating AlOx across the entire surface—except in those patterned circles, which are intended to form the metal–semiconductor contacts. These heterojunctions are created during the second EBL step, which includes the deposition of Co and Au exclusively within the circles left uncovered by the AlOx layer as a result of the previous step.



(a) First lithographic step



(b) Second lithographic step

Figure 3.1.3: Steps of the fabrication process of Co/Nb:$SrTiO_3$ memristive contacts.

Before initiating the first lithographic process itself, the annealed and single-terminated Nb:STO substrate must be carefully cleaned, and the negative e-beam resist AZ nLOF 2020 must be spin-coated onto its surface. The coating technique is designed to ensure a uniform distribution of the resist material over the substrate by means of a constant rotational speed of 3000 rpm for 1 minute. Once the spin-coating step is complete, the substrate must be soft-baked at 110 C to eliminate any residual solvent and enhance the adhesion between materials.

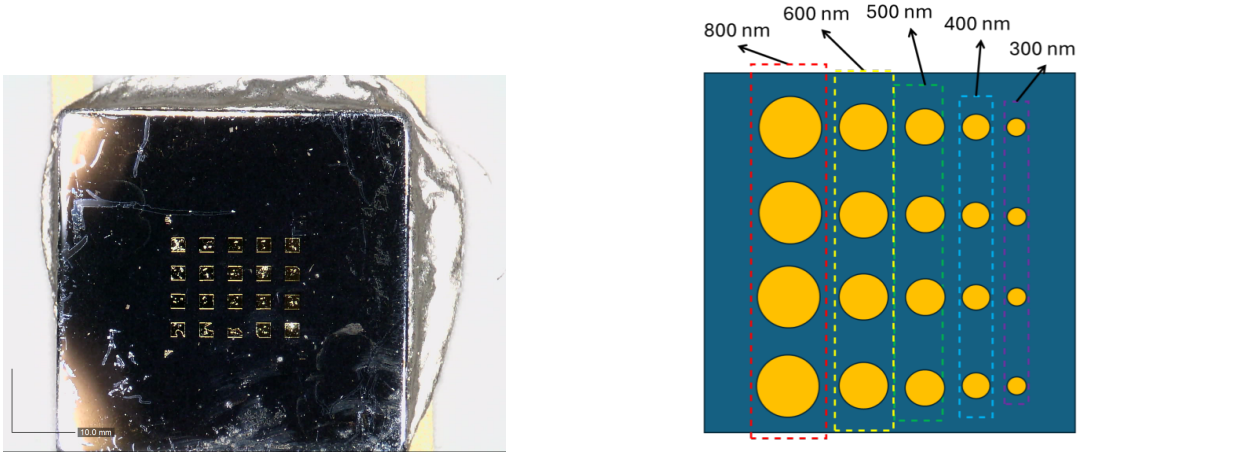
The desired initial pattern for the first lithographic step consists of a 44×5 array of circles left uncovered by the resist, arranged such that each column corresponds to a specific, predefined circle radius. The radii of the circles from the first to the fifth column are: 800 nm, 600 nm, 500 nm, 400 nm, and 300 nm, respectively. This pattern is illustrated in Figure 3.1.4b and is digitally defined in the Electron Beam Lithography (EBL) system.

Before starting the electron beam exposure, parameters such as focus, stigmation, and aperture positioning must be computationally optimized. Depending on the column to be written, variables such as aperture distance, electron beam current, and dose per unit area must be adjusted to suit each specific case. For the smaller circles, the dose per area must be increased in order to overcome relevant physical and material limitations at this scale, such as the proximity effect and resist contrast, among others [23] [13]. The exposure time for this first lithographic process was 30 minutes.

After exposure, the material is developed to make the designed pattern visible. This is achieved by immersing the sample in AZ MIF developer for 90 seconds, followed by rinsing in deionized (DI) water for 2 minutes. Since a negative e-beam resist was used, the areas that were exposed to the electron beam undergo a crosslinking reaction, becoming more insoluble and thus remaining adhered to the substrate after development. In contrast, the unexposed circular regions retain their original structure and dissolve more readily during the development process, thereby revealing the underlying substrate surface.

Next, a thin 50 nm insulating layer of AlO_x is deposited onto the patterned sample using the electron beam evaporation machine, TFC-2000. The sample must be placed inside the system's load lock, and a pressure of approximately 5×10^{-6} mbar is established within the chamber. The deposition of AlO_x is carried out at a rate of 1 $\mathring{A}/s$.

Once the deposition is complete, the lift-off process of the resist material is carried out by immersing the



(a) Fabricated device

(b) Diagram of the fabricated device with Co/Nb:$SrTiO_3$ contacts

Figure 3.1.4: Disposition of the fabricated devices in the measuring chip.

sample in an NMP (1-methyl-2-pyrrolidone) solution preheated to $80C$ for 15 minutes. Then, the sample is ultrasonicated at maximum power for 99 minutes to remove any remaining solvent or resist residues. In this way, the first lithographic step of the fabrication process is completed, resulting in an Nb:STO substrate fully covered by AlO_x except for circular areas of varying diameters where the substrate surface remains exposed. Under this configuration, the circles are now electrically isolated from each other and from the rest of the substrate.

In the second step of the fabrication process, the EBL technique is employed in the same manner to construct the metal–semiconductor contacts of the final device within the spaces provided by the previously designed and isolated circular openings. For this purpose, the Nb:STO substrate with the deposited AlO_x layer is spin-coated again, this time with a positive e-beam resist. The resist used is PMMA 950K 4%, which is spin-coated at 4000 rpm for 1 minute. The sample is then soft-baked at 180 C for 90 seconds.

The exposure is once again carried out using the EBL system, although in this case the process lasts for 1 hour. Subsequently, the e-beam resist is developed by immersing the sample in an MIBK:IPA solution for 60 seconds, followed by immersion in deionized (DI) water for the same duration. Since the resist material is positive, the exposed areas undergo chain scission, making them more soluble in the developer solution compared to the unexposed regions.

Finally, the second step is completed with the sequential deposition of thin layers consisting of 20 nm of Co and 120 nm of Au, one on top of the other, respectively. The deposition is carried out using the TFC-2000 system, where Co is deposited at a rate of 1 $\AA/s$, while the Au layer is deposited at a rate of 3 $\AA/s$. In this step, the sample is immersed in cold acetone for several days to facilitate the lift-off process. Afterwards, gentle ultrasonication is applied to the substrate to remove any remaining metal flakes.

In this way, the fabrication process is completed, resulting in an array of circular Schottky contacts of varying sizes formed by Co/Nb:STO. These contacts are electrically isolated from one another due to the presence of the AlO_x layer. The Au layer deposited on top of the contacts serves to prevent the oxidation of Co, as gold is

an inert metal with low chemical reactivity. Figure 3.1.4a shows an image of the fabricated device after being mounted onto a chip carrier using a conductive silver paste.

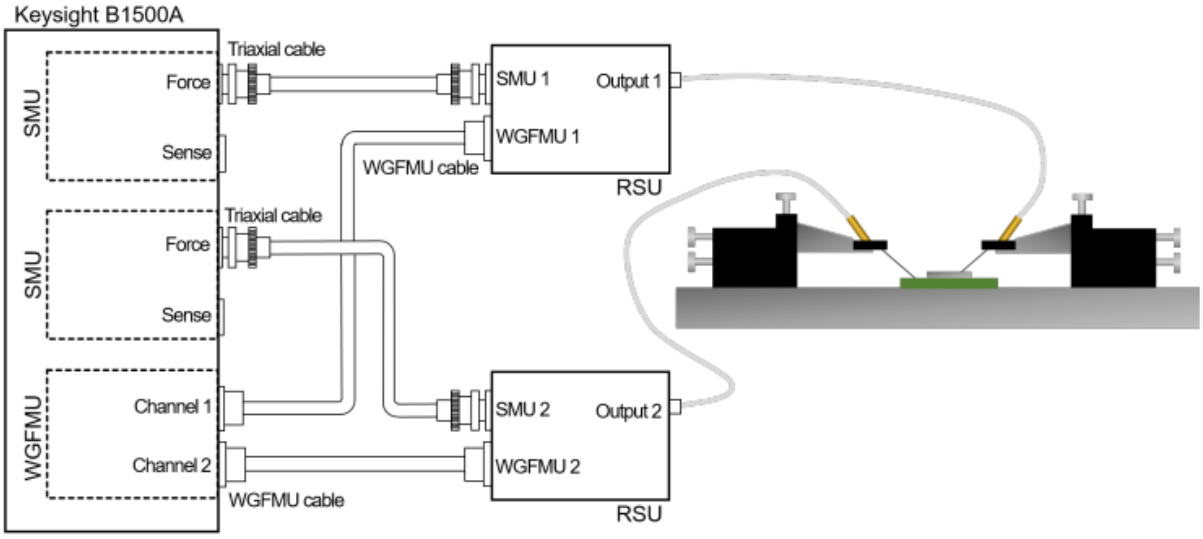


Figure 3.1.5: Experimental setup for the electrical characterization of samples using the B1500A Keysight Analyzer [10]

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3.2 Electrical Characterization

Measurements of the electrical properties are fundamental for analyzing the behavior of the tested memristive device. The results obtained regarding the electrical characterization in this research were acquired using the Keysight B1500A Semiconductor Device Analyzer. The experimental setup for this process is shown in Figure 3.1.5 [10].

The Keysight B1500A Semiconductor Device Analyzer consists of a computer connected via various rear ports to up to 10 supported modules designed for specific measurements. The computer has integrated EasyEXPERT group+ software, which allows for selecting and configuring different measurement modes. The modes used for electrical characterization in this research are described in more detail in Appendix A, including: I/V Sweep, I/V-t Sample, I/V List Sample, and Pulsed wave generator measurements.

The most basic electrical measurements are performed using Source/Monitor Units (SMUs), which are connected to their respective modules. An SMU compactly integrates a current source, a power supply, an ammeter, and a voltmeter, allowing for rapid switching between these resources without manual hardware changes. These units are used in the most basic measurement modes, related to classic tests like I/V Sweep, I/V-t Sample, and I/V List Sample, where it's necessary to control a wide variety of parameters. The maximum measurement and sourcing power for voltage and current is 200 V and 1 A, respectively, with a resolution down to 0.5 μV and 0.1 pA. Additionally, these units can produce voltage and current pulses in the 50 μs range, as well as time-dependent measurements with a speed of 100 μs.

The Waveform Generator/Fast Measuring Unit (WGFMU) module offers greater speed and precision in both supplying and measuring processes, enabling more advanced characterizations, including fast-pulsed and high-speed transient analysis. The waveform configuration supports pulses as short as 100 ns, and it's also possible to simultaneously measure current and voltage with a 5 ns sampling rate. This mode of operation is essential for analyzing the properties and applications of the devices under test in relation to their capabilities as memory units.

Two cables or probes are connected to each of these modules and are brought into contact with the device. One of the probes must be placed on the silver paste present on the chip carrier, while the other is carefully positioned directly on each of the Co/Nb:STO devices with the aid of a Dino-Lite digital camera with a 5-megapixel resolution.

Chapter 4 Results and Discussion

In order to analyze the properties of the fabricated Co/Nb:STO devices, several I–V curves were obtained, reflecting the relationship between the voltage applied to the device and the resulting output current. These measurements were performed for all devices and analytically compared with one another. Additionally, the behavior of the devices under different voltage pulses was examined, allowing for discussion of the response speed, transient characteristics, and previously unexplored depression and potentiation properties, which offer promising potential for various applications.

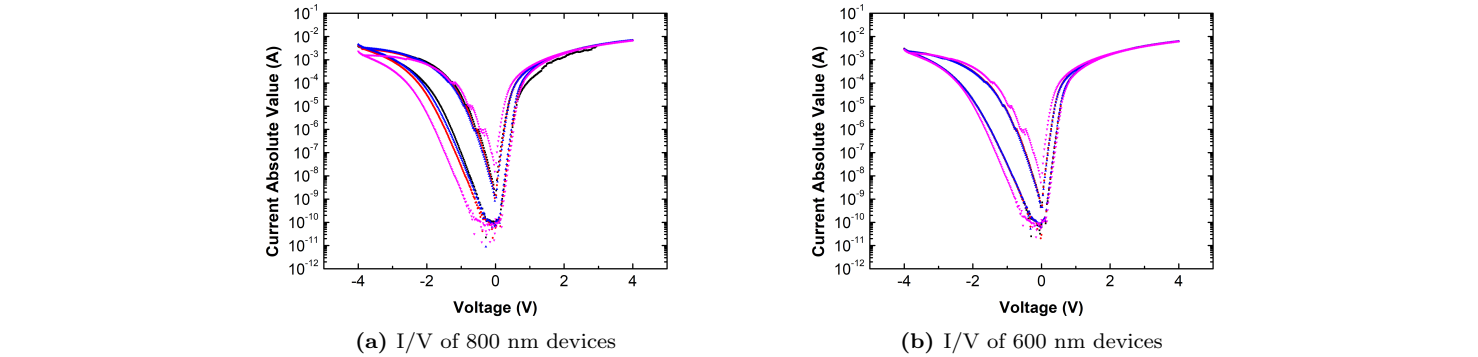
4.1 Current-Voltage Characteristics

Multiple I–V measurements were performed on devices of identical size to compare the variability in their behavior and to identify any defective units with fabrication-related issues. Figure 4.1.1 displays several plots of the I–V characteristics from different devices of the same dimensions, where voltage sweeps were applied with an initial RESET voltage of -4 V and a SET voltage of 4 V. The terms SET and RESET voltages refer to the voltage values at which a polarity reversal of the applied potential induces the transition from the High Resistance State (HRS) to the Low Resistance State (LRS), and vice versa, respectively. This mechanism is known as bipolar resistive switching, which has been introduced already in Section 2.3.3.

Most devices exhibit a clear hysteretic behavior, characterized by two well-defined current branches at the same voltage value in both the forward and reverse bias regimes. The upper branch, associated with higher current levels, corresponds to the LRS, whereas the lower branch represents the HRS. This behavior confirms that the fabrication process was largely successful, effectively demonstrating the memristive properties of Co/Nb:STO. Only two of the smallest devices, shown in plot 4.1.1e deviate from this trend.

The gap between the current lines of each state is referred to as the dynamic range, which is more pronounced under reverse bias than under forward bias. However, both branches tend to saturate near the SET and RESET voltage values, where the two states converge and become indistinguishable. The fact that the dynamic range is narrower in forward bias compared to reverse bias can be explained by the different dominant carrier transport mechanisms in each regime, as well as the influence of trapping states on the overall current density. In forward bias, the primary transport mechanism is thermionic emission of carriers with sufficient energy to “jump” over the effective potential barrier, which is significantly reduced. Under these conditions, the likelihood of various tunneling processes is diminished, and their contribution to the current density toward the metal side is negligible. Consequently, trapping-assisted tunneling plays a secondary role under forward bias, reducing the differences between the LRS and HRS and limiting the memristive properties. In contrast, under reverse bias, carrier tunneling processes become highly relevant, as the potential barrier at the interface becomes thinner. As a result, trapping-assisted tunneling contributes more substantially to the overall current density toward the semiconductor, enhancing the differences between the LRS and HRS and increasing the dynamic range in the reverse bias regime.

Some LRS curves under reverse bias show a sudden step-like increase in current, corresponding to a change in its order of magnitude, as well as a crossing point and overshoot between the LRS and HRS branches within the same regime. These features have been attributed to limitations of the Keysight B1500A measurement system and have therefore been excluded from the analysis of Co/Nb:STO properties.



(a) I/V of 800 nm devices

(b) I/V of 600 nm devices

(c) I/V of 500 nm devices

(d) I/V of 400 nm devices

(e) I/V of 300 nm devices

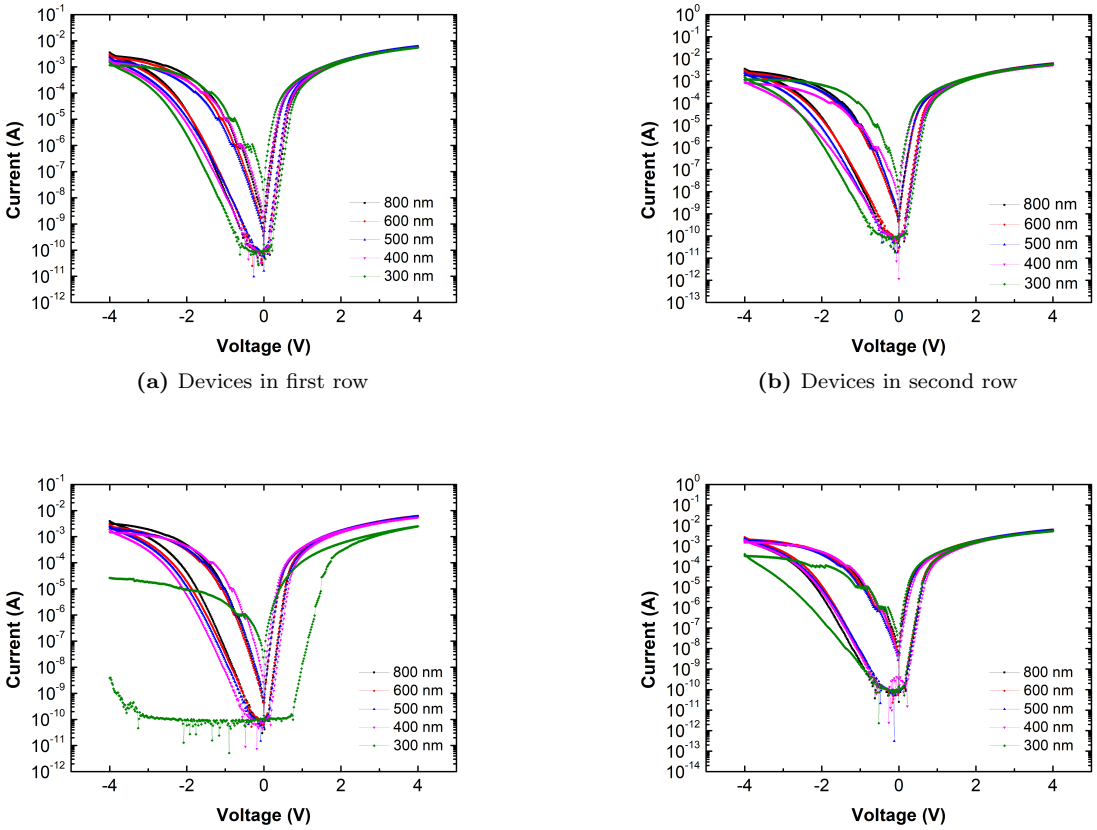
Figure 4.1.1: Current-voltage characteristics of several equal-sized devices.

Although minor differences are inevitable due to the inherent difficulty of fabricating perfectly identical contacts, the device-to-device variation is relatively low, as the I–V curves in each plot tend to overlap closely. This is a highly favorable feature, as it reflects the consistency, reliability, and predictability of these devices. These are some key characteristics for both practical applications and accurate modeling. Moreover, the variations among devices of the same size tend to decrease with miniaturization, suggesting an enhancement of the material's properties at smaller scales. Similar observations presented in the following sections support this claim, highlighting the high spatial and energy efficiency of Co/Nb:STO.

4.2 Device Scaling Effects

With the aim of analyzing the consequences of reducing device size, I–V curves were obtained using voltage sweeps with a RESET voltage of -4 V and a RESET voltage of 4 V. Figure 4.2.1 shows the size variation across a series of devices. The contact radius ranges from 800 nm down to 300 nm, the latter corresponding to the smallest Co/Nb:STO device ever fabricated at the Zernike Institute for Advanced Materials.

A clear increase in the dynamic range between the LRS and HRS was observed as device size decreased. This widening of the window is primarily attributed to the edge effect, which depends on the perimeter-area ratio [10]. This effect consists of the appearance of different properties on the surface of materials compared to the rest of the bulk, due to high surface energy. Therefore, the electrical characteristics of nanostructures near their edges can differ from the rest of the material. With respect to the electric field, the edge effect can result in a higher concentration of field strength on the surface, which is the basis for resistive switching behavior. In the case of smaller devices, the consequences of the edge effect become more evident, leading to a stronger differentiation between resistance states and thereby enhancing the memristive behavior and overall applicability of the material.



(a) Devices in first row

(b) Devices in second row

(c) Devices in third row

(d) Devices in forth row

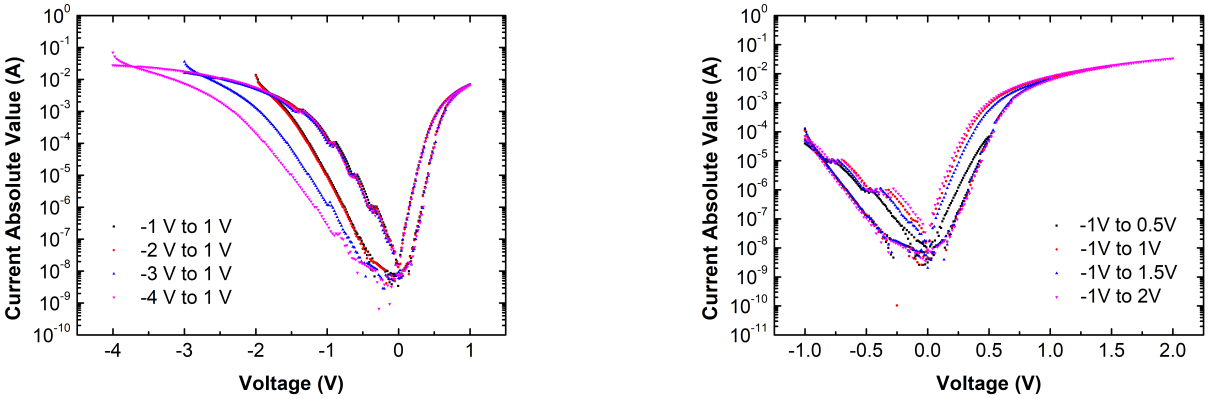
Figure 4.2.1: Current-voltage characteristics of devices with different sizes from 800 nm to 300 nm

Under reverse bias, the variation in the dynamic range is particularly pronounced, since the dominant carrier transport mechanism consists of several tunneling processes whose efficiency strongly depends on electric filed strength. In contrast, under forward bias, the dynamic range exhibits more subtle variation, since trapping and detrapping of the interface states is not the main contribution to the current changes. In this regime, the main transport mechanism is thermionic emission of electrons over the Schottky potential barrier. This process is largely size-independent, and while tunneling contributes to the forward current density, its role is comparatively minor, making the influence of varying trapping state densities less significant.

4.3 RESET and SET Voltage Variations

In Figure 4.3.1, the I–V characteristics of a single device are shown after performing several voltage sweeps in which the SET and RESET voltage values are varied.

In plot 4.3.1b, the SET voltage is fixed at 1 V, while the RESET voltage is varied from -1 V to -4 V. In this case, the hysteresis loop under forward bias remains unchanged. However, in the reverse bias regime, the loop expands to match the increasing voltage range, progressively extending further to the left. Although the LRS and HRS branches do not overlap, they do converge in all cases. The current lines associated with the LRS under reverse bias overlap perfectly across all voltage ranges, exhibiting the same slope variation and differing only in their extension along the voltage axis. In contrast, the HRS current lines in the reverse bias regime vary with the applied RESET voltage, showing no overlap while maintaining similar slopes. This behavior indicates a multilevel nature of the memristor under test, as intermediate resistance states between



(a) Reverse voltage variation

(b) Forward voltage variation

Figure 4.3.1: Current-voltage characteristics of a device under voltage sweeps with different ranges.

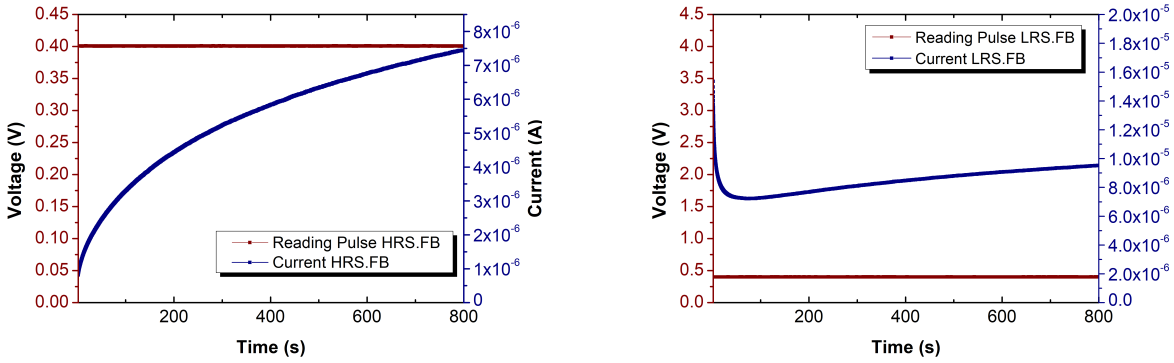
the LRS and HRS can be accessed in the reverse bias regime. By modulating the RESET voltage range, this property can be enhanced, offering significant advantages for non-binary computational memory, particularly for multi-level cells (MLCs), which can respond with mid-step memory values and store more than a single bit of information [8].

On the other hand, plot 4.3.1a displays the I–V characteristics of the same device when the RESET voltage is fixed at -2 V, and the SET voltage is varied within a range from 0.5 V to 2 V. Under these conditions, the different loops in the reverse bias do not undergo significant changes, while the branches under forward bias extend further to the right. The current lines with lower values, associated with the HRS under forward bias, overlap with one another and become indistinguishable except for their extension along the voltage axis. However, the lines corresponding to the LRS in the forward bias show slightly different slopes and are marginally separated from each other, unlocking intermediate states too. Unlike the modulation of the RESET voltage range, the current gap between the intermediate lines within the memory window is smaller in this case, which would hinder non-binary memory applications, although it could still be feasible with proper device design.

These differences in the variation of states when altering the RESET versus the SET voltage are related to the overlap of the current lines at the limits of the voltage domain in each case. While the LRS and HRS lines under reverse bias modulation converge at different points, the lines corresponding to both states during forward bias modulation tend to overlap and converge at the same point. This phenomenon can be explained by the movement of the semiconductor's Fermi level and the occupation or release of interfacial trapping states, whose number is finite and limited. Once the maximum number of trapping states has been either occupied or released under forward and reverse bias respectively, the resulting current behavior becomes comparable to that observed under a constant voltage, with the Fermi level remaining fixed. This is because the number of available trapping states remains constant in both situations. Therefore, the current line behavior at the domain extremes in each plot resembles the transient current response of each state to a constant voltage pulse, as will be shown in Section 4.4. Ultimately, the overlap between the LRS and HRS lines under forward bias modulation arises from the nearly identical time-dependent resistance values of both states when the number of occupied trapping states reaches its maximum and becomes stable. In contrast, the LRS and HRS lines under reverse bias modulation do not overlap and diverge rapidly after converging, as the time-dependent resistance variations between these states are significantly different.

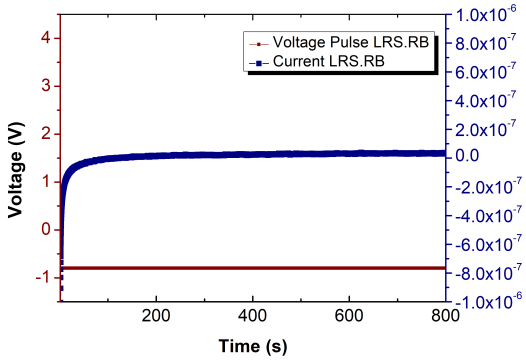
4.4 Resistance Changing Rate at Constant Voltage Pulses

Based on the curved traces observed in the I–V sweeps in Section 4.3, along with additional measurements carried out using the I/V List Mode and I/V-t Sampling modes of the Keysight Semiconductor Device

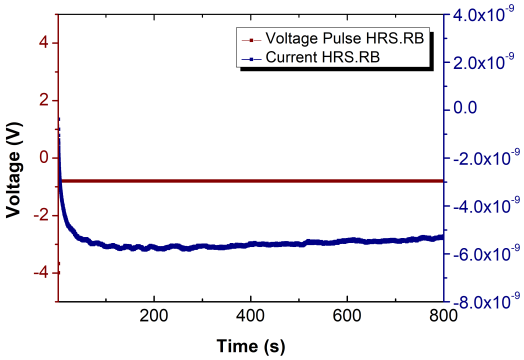


(a) HRS of forward bias

(b) LRS of forward bias



(c) LRS of reverse bias



(d) HRS of reverse bias

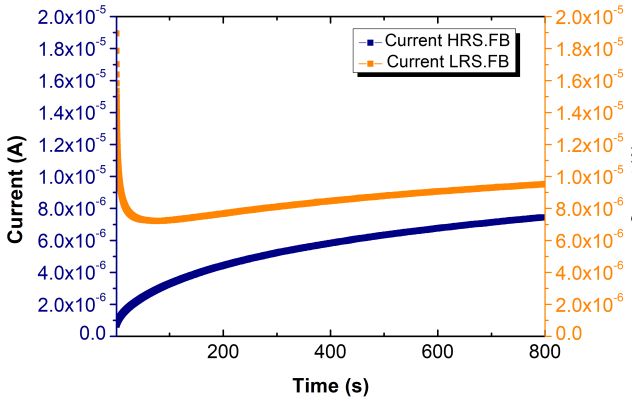
Figure 4.4.1: Resulting current at constant reading voltage pulses for each state

Analyzer (see Appendix B.1), it was inferred that the resistance of the Co/Nb:STO devices at constant voltage evolves differently over time depending on the memristive state. To investigate the time dependence on resistance across all memristive states, a series of custom voltage pulses were designed and applied using the WGFMU mode of the Keysight system. These pulses enable selective access to each resistance state while continuously monitoring the output current at a constant applied voltage.

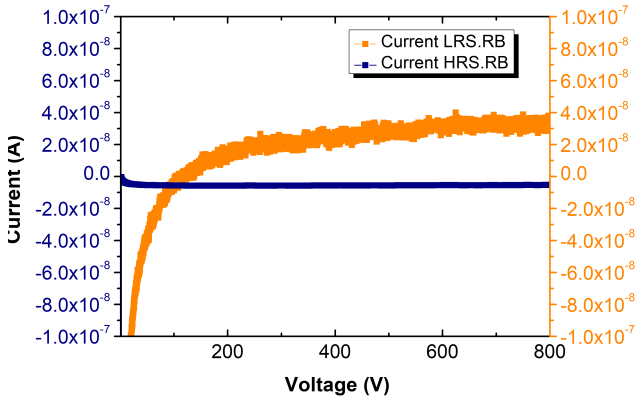
The voltage pulse sequences for each state are shown in Appendix B.1.2. Figure 4.4.1 presents the corresponding current responses for the HRS and LRS under forward bias (B.1.2a and B.1.2b), as well as for the LRS and HRS under reverse bias (B.1.2c and B.1.2d). The voltage pulse sequences applied in each case are, respectively: 0 V → 0.4 V, 0 V → 2 V → 0.4 V, 0 V → 2 V → -0.8 V, and 0 V → 2 V → -2 V → -0.8 V. Although similar measurements have been performed in previous works by the Spintronics of Functional Materials research group, the pulse durations have been extended in the present study to enhance the quality and depth of the results, allowing for a more thorough discussion [10].

The resulting current under a constant voltage pulse in the HRS under forward bias tends to increase slightly over time, indicating a gradual decrease in resistance (plot B.1.2a). In contrast, the transient current in LRS under forward bias initially exhibits a sudden drop, corresponding to a sharp increase in resistance (plot B.1.2b). However, the current soon begins to increase gradually again, reflecting a progressive decrease in resistance. The slope of the current increase in this phase of the LRS is remarkably similar to that observed in the HRS. Plot 4.4.2a shows both cases on the same graph, where it can be seen that the two curves do not converge but rather run almost parallel to each other.

These voltage pulses aim to simulate the reading process required in memory applications, where a constant voltage must be maintained for a certain duration until the measurement and analysis of the device's output



(a) HRS and LRS current lines in forward bias during constant reading voltage pulses.



(b) HRS and LRS current lines in reverse bias during constant reading voltage pulses.

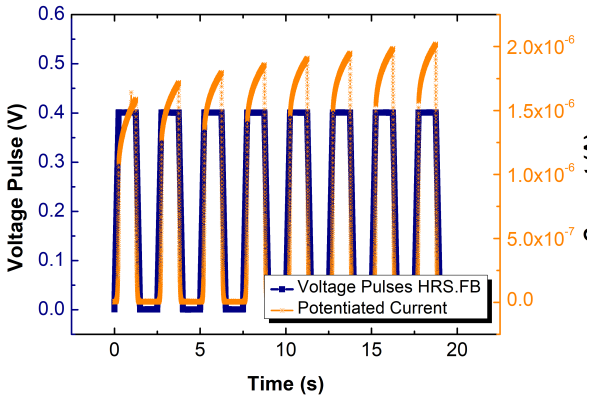
Figure 4.4.2: Comparison of currents from HRS and LRS of forward and reverse under constant reading voltage pulses.

current are completed. For this purpose, it is crucial that the curves associated with the LRS and HRS do not intersect or come too close, as this would significantly hinder the distinction between the two states. The memristive device tested under forward bias exhibits relatively optimal behavior in this regard. Although the LRS current values initially decrease sharply and approach those of the HRS, a previously described change in trend occurs around the 20-second mark, after which the curves for both states begin to increase with a similar slope. The fact that the minimum current value in the LRS remains higher than the maximum current value in the HRS, and that the curves do not converge for extended periods, are two strong indicators supporting the suitability of the Co/Nb:STO memristive device under forward bias for memory-related applications.

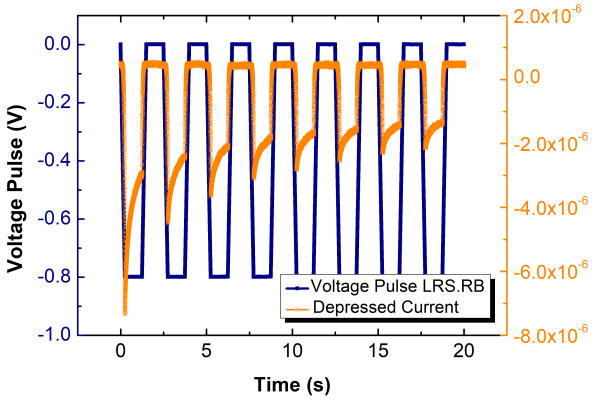
Under reverse bias, the output current of the LRS during constant voltage exhibits an initial abrupt decrease, where the absolute value of the current drops until it reaches 0 Å (plot B.1.2c). It is important to note that the current in this bias regime is negative, meaning that the resistance is lower when the absolute value of the negative current is higher. The variation in resistance is so pronounced that the LRS current even reaches positive values, suggesting a reversal in the direction of current flow. The transient current of the HRS, in contrast, displays completely opposite behavior (plot B.1.2d. Initially, the absolute magnitude of the current increases slightly on the order of 10 A, but quickly stabilizes and becomes constant. As a result, the resistance variation over time in the HRS under reverse bias is virtually negligible.

In plot 4.4.2b, the LRS and HRS curves under reverse bias are shown together, allowing for a clearer comparison of their differences. In this case, the stark contrast between the resistance variations of each state following the constant voltage pulses leads to a very noticeable convergence between the two curves. As a result, it becomes increasingly difficult to distinguish between the two possible resistance states. This significantly reduces the effective time window available for reliably analyzing the memristor's response under reverse bias, ultimately limiting the device's performance in practical applications where precise state detection is essential.

Regarding the physical principles underlying these transient characteristics, under constant voltage the Fermi level of the material remains fixed either at a higher or lower position, corresponding to the forward or reverse bias regimes, respectively. Since the Fermi level remains stable, this implies that the number of available trapping states at the interface should also remain constant over time, and therefore, the total current density would be expected to remain steady. Only at the onset of the voltage pulse might a change in resistance occur, due to the typical short delay between the shift in the Fermi level and the subsequent filling or emptying of the trapping states at the interface. However, the experimental results indicate not only distinct resistance variations over time for each state, but also that these effects are sustained over extended periods. This suggests the presence of multiple localized phenomena related to charge motion at the interface that alter



(a) Potentation behaviour of the current after several pulses in the HRS of reverse bias.



(b) Depressive behaviour of the current after several pulses in the LRS of reverse bias.

Figure 4.4.3: Potentation and depression characteristics due to numerous identical voltage pulses.

the Schottky barrier profile, although they have not been fully identified yet.

4.5 Potentiation and Depression Behaviour

In the previous section, it was concluded that the current associated with the HRS under forward bias tends to increase over time at constant voltage, whereas the opposite effect occurs in the LRS under reverse bias, where the current decreases. Using the WGFMU mode, a series of identical, repeated rectangular voltage pulses were applied, accessing each of the aforementioned states and measuring the current generated by the device under test. The aim of this experiment is to determine whether a behavior similar to the previously analyzed transient characteristics can be reproduced through this approach, effectively simulating the effect of multiple, successive stimuli.

In graph 4.4.3a, the repeated voltage pulses and the resulting current in the HRS under forward bias are plotted. A single pulse consists of the sweep $0\,\mathrm{V} \rightarrow 0.4\,\mathrm{V} \rightarrow 0\,\mathrm{V}$, where the $0.4\,\mathrm{V}$ level is held constant for a duration of several seconds. In this way, the transient behavior of the HRS at constant voltage is reflected during these voltage peaks, corresponding to the current increase phases observed in the graph. The repeated application of the same voltage pulse leads to a gradual increase in the overall current from one pulse to the next, producing a distinctive and previously unreported current potentiation phenomenon in Co/Nb:STO memristive devices.

The second case is illustrated in plot 4.4.3b, where the repeated voltage pulses used to access the LRS under reverse bias and the resulting current are shown. The overall voltage waveform consists of successive identical single pulses, following the sweep $0\,\mathrm{V} \rightarrow -0.8\,\mathrm{V} \rightarrow 0\,\mathrm{V}$. As in the previous case, the $-0.8\,\mathrm{V}$ level is held constant for several seconds, allowing the transient behavior of the LRS under constant reverse bias to manifest. This accounts for the observed decrease in current during each voltage peak. Moreover, the repeated application of these voltage pulses results in a progressive reduction in the absolute magnitude of the current from pulse to pulse, corresponding to a current depression process.

This transient phenomenon has also been observed in voltage pulses with widths ranging from milliseconds down to nanoseconds. Figure 4.5.1 presents the results obtained in the millisecond regime after applying repeated voltage sweeps of the form $0\,\mathrm{V} \rightarrow -0.8\,\mathrm{V} \rightarrow 0\,\mathrm{V}$ to the memristive device, accessing the LRS under reverse bias. As expected, the decreasing trend of the current during each single pulse persists. However, the overall current only exhibits a clear depression during the initial pulses; in subsequent pulses, the current values stabilize roughly around a constant level. This behavior appears to be influenced by a secondary effect occurring when the $0\,\mathrm{V}$ segment is held between pulses, which partially counteracts the depressive effect

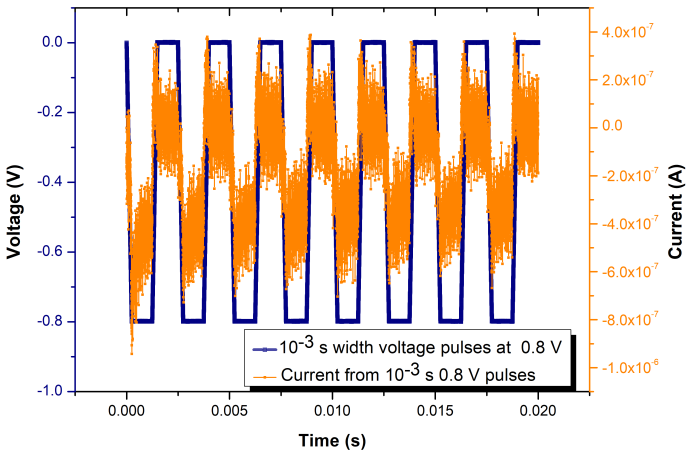


Figure 4.5.1: Depressive behabiour in the milisecond time range

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induced by the –0.8 V segments. Although the underlying mechanism is not yet fully understood, there is reason to believe that it could be mitigated by either reducing the time width of the 0 V segment in each pulse or adjusting the voltage sweep range. Such modifications could enhance the current depression characteristics in the millisecond regime.

The potentiation and depression patterns become difficult to distinguish in the microsecond and nanosecond time regimes, which may suggest that Co/Nb:STO devices do not exhibit a rapid response to very short stimuli (see Appendix B.2). However, this interpretation is subject to certain limitations related to the measurement system itself. These include challenges in determining the appropriate current range and inadequacies in the shape of the voltage pulses when operating at such short timescales. Therefore, this conclusion regarding the speed of the devices under test is not definitive. The complexity of the electrical characterization method, particularly when using the WGFMU mode of the Keysight Semiconductor Device Analyzer, suggests that the measurement apparatus may lack the sensitivity or precision required to capture accurate results in these fast regimes.

4.6 Discussion

In the context of neuromorphic computing, there are numerous essential requirements for new materials and devices designed to lead this emerging computational paradigm. First and foremost, devices must retain their previously established state even when the power is turned off. This property, known as non-volatile memory, enables the permanent preservation of desired information until it is intentionally erased or overwritten. Additionally, devices must operate effectively under low power conditions, demonstrating high energy efficiency by minimizing the energy consumption necessary for proper function.

Another critical factor is the operational speed of the device, which refers to the time required for state transitions and the exhibition of a consistent response. The faster the device, the better its performance. Regarding durability and reliability, the device's behavior should not undergo significant changes during prolonged and intensive use, involving numerous write and read cycles. High stability between cycles and minimal variation in results compared to other devices must be observed.

Finally, it is crucial that device dimensions be easily scalable, allowing significant size reduction without adversely affecting any of their properties. All these conditions are indispensable for developing memory components capable of emulating the characteristics of neurons and their interconnections, highlighting the

remarkable efficiency and complexity of the human brain [17]. By leveraging devices with these features arranged in networks analogous to neural systems, it would be possible to overcome the von Neumann bottleneck by co-locating memory and processing functions, which is the ultimate goal of the present research.

Through the analysis of the results obtained during this research, the electronic characterization of the Co/Nb:STO memristive devices has been successfully conducted. Based on this, it can be inferred that the properties of the studied contacts meet most of the requirements necessary to satisfy the demands imposed by neuromorphic computing.

All devices under study have demonstrated minimal device-to-device variation, indicating only slight differences in the behavior of the samples. The dynamic range exhibits no significant changes between similar devices. Furthermore, studies conducted within the Spintronics of Functional Materials research group have confirmed their remarkable durability, with numerous write and read cycles performed without observing substantial alterations in the I/V curves [10]. Consequently, these contacts are extremely reliable and long-lasting, greatly facilitating the processes of research, development, and their joint implementation.

The memory states in the Co/Nb:STO contacts are closely linked to distinct resistance states, where the current conductance varies and these changes can be readily distinguished through the I/V curves. Accessing each state requires only polarity changes in the applied voltage, which induce modifications in the number of available trapping states contributing to the resulting current. The devices' dynamic range, which consists of the gap between the current lines corresponding to each resistance state, is clearly observable even at relatively low voltage values. This enables differentiation between states with minimal energy expenditure, by applying voltages in the range below 1 V up to 4 V. As long as no polarity change occurs, the devices maintain the previously written resistance state indefinitely, satisfying the non-volatile memory requirements of neuromorphic computing.

Beyond simply meeting the requirements for neuromorphic functions, the fabricated Co/Nb:STO memristive devices have demonstrated highly beneficial performance characteristics. Maintaining memristive properties when contacts are miniaturized is crucial for enhancing energy and spatial efficiency. In this regard, the devices studied not only retain their properties but also show improved characteristics after scaling processes. Smaller contacts induce a greater difference between the output currents of each state in the I/V curves, making them easier to distinguish and allowing for more flexible algorithm design in recognition processes.

Upon applying various voltage ranges, it's been confirmed that it's possible to distinguish not only between two resistance states in the I/V characteristics of Co/Nb:STO, but also to unlock functional intermediate states in the reverse bias regime. The presence of more than two distinct states is extremely valuable as it allows for storing more information in a single memory unit compared to binary cells. Considering this property, storing more than 1 bit per cell is feasible, increasing information density and improving the efficiency of certain processes. However, state recognition phases become more complex and slower, making this a particularly useful option for specific processing tasks.

Another aspect to consider is the tunability of the conductance. The potentiation and depression properties of these devices are a fundamental concept of great utility within the context of neuromorphic computing. Neurons in the human brain possess an ability to adapt to their environment, modifying their response based on the nature, intensity, and recurrence of detected stimuli. Based on these parameters, the synaptic connections between neurons can be inhibited or potentiated, which is a fundamental mechanism in memory and learning processes. This characteristic is known as synaptic plasticity, and it can potentially be replicated in Co/Nb:STO devices with the correct design and activation of depression and potentiation behavior.

Furthermore, this novel property may be useful for functionalities beyond computational memory. Nociceptors are receptors capable of detecting harmful stimuli in the human body and sending signals to the brain for interpretation. Damaging contact or injury corresponds to a voltage input, which the nociceptor detects. If the stimulus magnitude doesn't exceed a certain threshold voltage, the contact isn't considered harmful, and no response is generated. Conversely, if the contact detected by the nociceptor surpasses the established threshold voltage value, the receptor will generate a current signal as a response, which will be

sent to the brain for processing and appropriate action. Depending on the force and frequency of the contact, the nociceptor has the ability to modulate the signal to activate different body actions. Co/Nb:STO diffusive memristor devices can be configured to exhibit behavior similar to nociceptors, where the potentiation and depression of the signal are important for enabling adaptive processes to stimuli. Additionally, biological pain receptors are capable of reacting to pulses in the millisecond range. The tested memristive devices also offer responses to voltage pulses generated within this time range, although results concerning the microsecond and nanosecond ranges are not yet conclusive. This potential application of Co/Nb:STO is currently under research by the Spintronics of Functional Materials research group at the University of Groningen [35].

Despite the promising aspects, certain behaviors of the Co/Nb:STO nanostructures are unfavorable and currently prevent their immediate application as neuromorphic components. These issues necessitate more rigorous study. Firstly, current reading simulations performed with constant voltage pulses have been satisfactory under forward bias. However, it's been shown that in the reverse bias regime, the transient currents of both states tend to converge rapidly during constant voltage application. This phenomenon, known as destructive readout of memory states, makes it impossible to distinguish between the output currents from each state for extended periods. In this case, the states in the reverse bias region cannot be clearly differentiated, which means no information bit can be reliably associated with them. This is a very counterproductive finding, especially since the lines generated by reverse bias voltages in the I/V curves previously showed enhanced characteristics compared to forward bias, such as a larger gap between the current states.

Regarding the device's response speed, the various voltage pulses applied to the devices have produced relatively adequate patterns in the order of 100 microseconds (µs). This result is comparable to the processing speed of the human brain, which can detect stimuli within a similar timeframe. Nevertheless, some traditional memory devices, as well as other components currently under investigation as embedded-memory cells, have demonstrated extremely fast speeds in the order of microseconds and nanoseconds [17].

4.7 Experimental and Theoretical Limitations

The Co/Nb:STO contacts appear to exhibit a behavioral pattern within these ranges, but significant limitations in both the measurement apparatus and the experimental methodology have impacted these results, preventing clear conclusions. This highlights the presence of several limiting factors that have hindered the experimental process and, to some extent, reduced the scope of this work.

Firstly, the B1500A Keysight Semiconductor Analyzer lacked the necessary connections to perform detailed measurements regarding the device capacitance as a function of different resistance states. Furthermore, using this measurement system makes it challenging to configure voltage pulses and obtain results for reaction times shorter than 100 µs. Therefore, for future experiments, it is suggested acquiring the relevant connections to obtain capacitance data. Additionally, we recommend using the Keithley 2400 Source Meter as an alternative measurement apparatus and verifying if it's possible to conduct measurements in lower time ranges.

Lastly, all results, discussions, and conclusions presented in this work have been based on the consequences of variations in the trapping states at the interface of the Schottky contacts on the overall current density (see Section 2.3.3). It's important to recognize that while this theory is highly useful for conceptually understanding the fundamentals behind the memristive properties of Co/Nb:STO, it serves only as a mere approximation of reality. Numerous real physical phenomena have not yet been investigated in detail by the scientific community and were not considered in this research. This represents an intrinsic limitation that prevents a detailed argumentation of all results based on fundamental physical principles.

Chapter 5 Conclusion

Currently, both conventional and advanced computational devices integrate the von Neumann architecture in their hardware, where memory storage units and processing units are physically separated. As a result of this arrangement, there are a series of inherent limitations that reduce the energy and time efficiency of the device. This phenomenon is known as the von Neumann bottleneck, and it is mainly caused by the energy consumption during the transmission of information between memory and the CPU, as well as by the mismatch in operating speed between these two functional units. Furthermore, the technological impossibility of fabricating smaller transistors and electronic components without increasing their operating energy leads to a standstill of this traditional computational paradigm in terms of efficiency.

Therefore, there is widespread interest within the scientific community in developing new paradigms beyond the von Neumann architecture, which would allow its limitations to be overcome and drive the next phase of exponential growth in the computing market. One of the most widely supported potential solutions is neuromorphic computing, which aims to artificially design devices with a structure similar to that found in the human brain. This architecture is based on the co-localization of memory and processing functions within a single module, simulating the behavior of neurons and the synaptic connections between them.

The aim of this research work has been to study the characteristics of different Co/Nb-doped $SrTiO_3$ interface-based memristive devices in the context of neuromorphic computing, discussing their potential application as embedded-memory units capable of replicating neuronal architecture. For this purpose, several Co/Nb-doped $SrTiO_3$ contacts of different diameters (ranging from 800 nm to 300 nm) were fabricated using a two-step lithographic process based on Electron Beam Lithography. In addition, the devices were electronically characterized using the B1500A Keysight Semiconductor Device Analyzer, focusing primarily on the scalability of the memristive devices, their device-to-device variability, and the physical mechanisms behind their behavior.

After analyzing the obtained results, a series of interesting and potentially useful properties of the Co/Nb-doped $SrTiO_3$ devices have been discovered in relation to neuromorphic computing. First, the current–voltage characteristics of all tested samples have shown typical memristive behavior, distinguishing a Low Resistance State (LRS) and a High Resistance State (HRS) under both forward and reverse bias. Access to each of these states is achieved by alternating the polarity of the applied voltage. The current–voltage curves among devices of the same size show minimal variation, demonstrating low device-to-device variability. It has also been verified that, through the miniaturization of the contacts, their memristive properties can be enhanced, displaying a greater dynamic range between states. By varying the voltage range, the existence of intermediate states between LRS and HRS has been identified, enabling increased memory density by designing multi-bit cells. Simulations of the readout process using voltage pulses have revealed non-destructive reading properties in the forward bias regime. Finally, potentiation and depression behavior of the current has been observed after applying appropriate voltage pulse configurations.

All these discovered properties represent fundamental requirements to artificially simulate the operation of human neurons, including high durability and reliability, easy scalability, low energy consumption, and synaptic plasticity to modulate conductivity. Therefore, it can be stated that Co/Nb-doped $SrTiO_3$ holds strong potential to become a leading material for memory applications in neuromorphic computing. Additionally, the potentiation and depression characteristics expand the technological reach of Co/Nb-doped $SrTiO_3$, making it potentially useful for functions such as biological sensing in response to mechanical stimuli. This new approach is currently being investigated by the Spintronics of Functional Materials research group at the

University of Groningen, focusing on the use of these devices as artificial nociceptors.

Nevertheless, there are certain limitations that must be taken into account and which require further investigation in order to reach a more definitive conclusion. Primarily, the results show a destructive reading pattern in the reverse bias regime, which would considerably hinder the distinction between states. The proper functioning of the Co/Nb-doped $SrTiO_3$ devices has also been demonstrated under stimuli in the 100 microsecond range, but more results are needed for faster pulses. Finally, the resistive switching theory presented in this thesis serves as a highly realistic conceptual approach capable of explaining most of the results physically. Unfortunately, there are certain behaviors related to resistance variation under constant voltages that cannot be explained through the theory of trapping/detrapping of interfacial states, indicating that unknown physical principles may be at play in Co/Nb-doped $SrTiO_3$, which cannot be addressed within the scope of this Final Bachelor Degree Project.

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The successful completion of this Bachelor's Thesis would not have been possible without the collaboration and support of many people, to whom I am deeply grateful. I would therefore like to take this opportunity to acknowledge them and offer the recognition they truly deserve.

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My passion for physics was first sparked by someone very special to me, Héctor, a telecommunications engineer at the University of Vigo. At the time, he was my private tutor, and we developed a meaningful friendship. His way of teaching mathematics and physics fascinated me, igniting a deep interest in the field. I look back on that time with great fondness, and I am deeply grateful for the advice he gave me and the time he dedicated to me, since those are the reasons I am now completing my university studies.

Lastly, and most importantly, I know I will never be able to fully express my gratitude for the constant support and dedication of my parents and my family. Thanks to them, I've had the opportunity to follow my dream and finish my degree with great joy. I hope they feel as proud of me as I am of them. They have supported me through both good and difficult times, something I feel immensely privileged for and value above all. To conclude, I simply want to express how much I love them, and how important they are in my life.

Bibliography

[1] I. Bhaduri, *Area-dependent resistive switching in memristive co/nb-doped srtio$_3$ schottky junctions*, Bachelor's thesis, Accessed via private link, Jul. 2021. [Online]. Available: https://mail.google.com/mail/u/0/?tab=rm&ogbl#starred/FMfcgzQbfBtlrcRSqKhBZhkPmsTWtXnB?projector=1.

[2] G. W. Burr, R. M. Shelby, A. Sebastian, *et al.*, "Neuromorphic Computing Using Non-Volatile Memory," *Advances in Physics: X*, vol. 2, no. 1, pp. 89–124, Dec. 2016, ISSN: 2374-6149. DOI: 10.1080/23746149.2016.1259585.

[3] E. Charles, S. Mahapatra, B. Salim, *et al.*, "Metal Oxide Memristors and Their Applications: A Review," *Solid-State Electronics*, vol. 203, p. 108 646, 2023. DOI: 10.1016/j.sse.2023.108646. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378775323005414.

[4] T. van Dalfsen and J. van Dam, *The applicability of srtio$_3$ in memristive devices: A preliminary investigation*, Bachelor Thesis, Accessed: 2025-06-21, 2013. [Online]. Available: https://essay.utwente.nl/65060/1/The%20applicability%20of%20SrTiO3%20in%20memristive%20devices%2C%20a%20preliminary%20investigation.pdf.

[5] J. Domaradzki, D. Wojcieszak, T. Kotwica, and E. Mańkowska, "Memristors: A Short Review on Fundamentals, Structures, Materials and Applications," *International Journal of Electronics and Telecommunications*, vol. 66, no. 2, pp. 373–381, 2020, Accessed: 2025-06-21. DOI: 10.24425/ijet.2020.131888. [Online]. Available: https://journals.pan.pl/Content/115215/PDF/51_2020.pdf.

[6] L. Eeckhout, "Is Moore's Law Slowing Down? What's Next?" *IEEE Micro*, vol. 37, no. 4, pp. 4–5, Jul. 2017, ISSN: 0272-1732. DOI: 10.1109/MM.2017.3421223.

[7] Elsevier, *Von neumann architecture*, ScienceDirect Topics, Computer Science, Accessed June 21, 2025, 2025. [Online]. Available: https://www.sciencedirect.com/topics/computer-science/von-neumann-architecture.

[8] P. Ganesh, S. Murali Krishna, and V. Ravi, "Multi-level memristor memory: Design and performance analysis," *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 8, no. 4, pp. 723–728, Feb. 2019, Accessed: 2025-06-27. [Online]. Available: https://www.researchgate.net/publication/331331547_Multi-level_memristor_memory_Design_and_performance_analysis.

[9] GeeksforGeeks, *Computer Organization–Von Neumann Architecture*, GeeksforGeeks, Last updated January 31, 2025; accessed June 21, 2025, Jan. 2025. [Online]. Available: https://www.geeksforgeeks.org/computer-organization-von-neumann-architecture/.

[10] A. S. Goossens, "Complex oxides for computing beyond von neumann," Ph.D. dissertation, University of Groningen, Oct. 2023. DOI: 10.33612/diss.766596376. [Online]. Available: https://doi.org/10.33612/diss.766596376.

[11] A. S. Goossens, M. Ahmadi, D. Gupta, I. Bhaduri, B. J. Kooi, and T. Banerjee, "Memristive memory enhancement by device miniaturization for neuromorphic computing," *Advanced Electronic Materials*, vol. 9, no. 4, 2023. DOI: 10.1002/aelm.202201111. [Online]. Available: https://doi.org/10.1002/aelm.202201111.

[12] J. F. Harrison, *Element work function (ev)*, PDF lecture notes, CEM 483 Quantum Chemistry course, Aug. 2008. [Online]. Available: https://www2.chemistry.msu.edu/faculty/harrison/cem483/work_functions.pdf.

[13] S. Hitomi, K. Michishita, H. Kawata, Y. Hirai, and M. Yasuda, "Molecular dynamics study of line edge roughness and the proximity effect in electron beam lithography," *Journal of Photopolymer Science and Technology*, vol. 28, no. 5, pp. 677–682, 2015. DOI: 10.2494/photopolymer.28.677. [Online]. Available: https://www.jstage.jst.go.jp/article/photopolymer/28/5/28_677/_pdf.

[14] HP Inc., *HP Labs Discovery Holds Potential to Fundamentally Change Computer System Design*, Accessed: 2025-06-21, Apr. 2010. [Online]. Available: https://investor.hp.com/news-events/news/news-details/2010/HP-Labs-Discovery-Holds-Potential-to-Fundamentally-Change-Computer--System-Design/default.aspx.

[15] A. M. Kamerbeek, T. Banerjee, and R. J. E. Hueting, "Electrostatic analysis of n-doped srtio$_3$ metal-insulator-semiconductor systems," *Journal of Applied Physics*, vol. 118, no. 22, p. 225 704, 2015. DOI: 10.1063/1.4936959. [Online]. Available: https://doi.org/10.1063/1.4936959.

[16] Kaunas University of Technology, *Ebl: E-beam lithography tool - raith e-line plus*, https://apcis.ktu.edu/MMI/en/site/katalogas?more=6727, Accessed: 2025-06-21, Kaunas, Lithuania, 2025.

[17] A. I. Khan, A. Keshavarzi, and S. Datta, "The future of ferroelectric field-effect transistor technology," *Nature Electronics*, vol. 3, no. 10, pp. 588–597, Oct. 2020, NSF Public Access, accessed: 2025-06-27, ISSN: 2520-1131. [Online]. Available: https://par.nsf.gov/servlets/purl/10243505.

[18] J. Kim, K. Jung, Y. Kim, *et al.*, "Switching Power Universality in Unipolar Resistive Switching Memories," *Scientific Reports*, vol. 6, 2016. DOI: 10.1038/srep23930. [Online]. Available: https://www.nature.com/articles/srep23930.

[19] C. Kittel, *Introduction to Solid State Physics*, 8th. Hoboken, NJ: John Wiley & Sons, 2005, Accessed: 2025-06-21; PDF hosted by Eötvös Loránd University, ISBN: 978-0471415268. [Online]. Available: https://metal.elte.hu/~groma/Anyagtudomany/kittel.pdf.

[20] J. E. Kleibeuker, G. Koster, W. Siemons, *et al.*, "Atomically defined rare-earth scandate crystal surfaces," *Advanced Functional Materials*, vol. 20, no. 20, pp. 3490–3496, 2010. DOI: 10.1002/adfm.201000889. [Online]. Available: https://www.utwente.nl/en/daveblank/publications/pdf-files/AdvFuncMat20(2010)3490.pdf.

[21] D. E. Knuth, "Von Neumann's First Computer Program," *ACM Computing Surveys*, vol. 2, no. 4, pp. 247–260, 1970. DOI: 10.1145/356580.356581.

[22] Levente Hajdu and Jérôme Lauret and Radomir A. Mihajlović, *Von Neumann Bottleneck (VNB)*, In *Handbook of Research on High Performance and Cloud Computing in Scientific Research and Education*, Chapter 13, Definition accessed via IGI Global dictionary, 2014. DOI: 10.4018/978-1-4666-5784-7.ch013.

[23] P. Li, "A review of proximity effect correction in electron-beam lithography," *arXiv:1509.05169 [cond-mat.mes-hall]*, 2015. [Online]. Available: https://arxiv.org/abs/1509.05169.

[24] K. Morito, Y. Iwazaki, T. Suzuki, and M. Fujimoto, "Electric field induced piezoelectric resonance in the micrometer to millimeter waveband in a thin film srtio$_3$ capacitor," *Journal of Applied Physics*, vol. 94, no. 8, pp. 5199–5205, 2003. DOI: 10.1063/1.1611268. [Online]. Available: https://doi.org/10.1063/1.1611268.

[25] B. Nagaraj, T. Wu, S. B. Ogale, T. Venkatesan, and R. Ramesh, "Interface characterization of all-perovskite oxide field effect heterostructures," *Journal of Electroceramics*, vol. 8, no. 3, pp. 233–241, 2002. DOI: 10.1023/A:1020806402413.

[26] J. von Neumann, "First Draft of a Report on the EDVAC," Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, PA, Technical Report Contract No. W-670-ORD-4926, Jun. 1945, Distributed by Herman Goldstine; first public description of the stored-program concept.

[27] B.-E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S.-M. Yoon, Eds., *Ferroelectric-Gate Field Effect Transistor Memories: Device Physics and Applications* (Topics in Applied Physics). Springer, 2020, vol. 131. DOI: 10.1007/978-981-15-1212-4.

[28] Y. Park, J. Jang, Q. Niu, and R. Ramesh, "Atomically flat single-terminated srtio$_3$ (111) surface," *Applied Physics Letters*, vol. 92, no. 15, p. 152 910, 2008, Published online May 12, 2008. DOI: 10.1063/1.365242.

[29] D. Pérez-Rodríguez, "The applicability of srtio$_3$ in memristive devices, a preliminary investigation," M.S. thesis, University of Twente, 2017. [Online]. Available: https://essay.utwente.nl/65060/1/The%20applicability%20of%20SrTiO3%20in%20memristive%20devices%2C%20a%20preliminary%20investigation.pdf.

[30] K. G. Rana, "Electron transport across complex oxide heterointerfaces," Ph.D. thesis under supervisors T. Banerjee and B. J. van Wees, Ph.D. dissertation, University of Groningen, Groningen, Netherlands, Sep. 2013. [Online]. Available: https://research.rug.nl/en/publications/electron-transport-across-complex-oxide-heterointerfaces.

[31] S. Suzuki, T. Yamamoto, H. Suzuki, K. Kawaguchi, K. Takahashi, and Y. Yoshisato, "Fabrication and characterization of bakbio$_3$/nb-doped srtio$_3$ all-oxide-type schottky junctions," *Journal of Applied Physics*, vol. 81, no. 10, pp. 6830–6836, 1997. DOI: 10.1063/1.365242.

[32] K. Takahashi, T. Susaki, and H. Y. Hwang, "Epitaxial growth and transport properties of nb-doped SrTiO_3 thin films," in *Strongly Correlated Electron Materials: Physics and Nanoengineering. Proceedings SPIE*, Presented at Optics and Photonics, vol. 5932, San Diego, California, USA: SPIE, 2005, 59321K. DOI: 10.1117/12.616888.

[33] B. Tellini, M. Bologna, K. J. Chandía, and M. Macucci, "A Capacitance-Coupled Ga_2O_3 Memristor," *International Journal of Circuit Theory and Applications*, vol. 44, no. 4, pp. 311–324, 2016. DOI: 10.1002/cta.3111.

[34] Unknown Author, *Semiconductor physics*, PDF lecture notes, Accessed: 2025-06-21; source: Seklad69 Associates, n.d. [Online]. Available: http://seklad69associates.com/seklad69associates.com/EEG_811_files/Semiconductor%20Physics.pdf.

[35] J. H. Yoon, Z. Wang, K. M. Kim, *et al.*, "An artificial nociceptor based on a diffusive memristor," *Nature Communications*, vol. 9, 2018, Accessed: 2025-06-27. DOI: 10.1038/s41467-017-02572-3. [Online]. Available: https://www.nature.com/articles/s41467-017-02572-3.

[36] X.-J. Zhou, H.-J. Grabert, W. Köster, H. Lüth, G. Füssler, and A. Weber, "Observation of quantized conductance in si-doped gaas/algaas heterostructures," *Solid State Communications*, vol. 83, no. 6, pp. 491–495, 1992. DOI: 10.1016/0038-1098(92)90094-F. [Online]. Available: https://doi.org/10.1016/0038-1098(92)90094-F.

[37] Y. Zhou and H.-S. P. Wong, "Energy-efficient vlsi design techniques for emerging nanoscale memory technologies," *Frontiers of Computer Science in China*, vol. 7, no. 1, pp. 53–65, 2013. DOI: 10.1007/s11704-013-2294-3. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1002007112001451.

Chapter A Electrical Measurements Modes

A.1 I/V Sweep Test

This mode allows for measuring the output current of the device under test after applying a continuous voltage variation within a determined range. In the Channel menu, probe 1 (connected to SMU 1) should be associated with the voltage application, while the current received by probe 2 (connected to SMU 2 and the device under test) should be measured by the computer. The relevant parameters for this mode are set in the Measurements section, whose display is shown in FigureA.1.1. Below is an explanation of the necessary configuration for performing a simple I/V Sweep measurement.

First, the direction of the output current lines is set to "double," allowing for current variations to be measured in both directions. For the devices analyzed, current range variations are more noticeable with a logarithmic scale. The range of applied voltages must be determined to limit the measurement loop. To obtain a complete current loop, including both reverse and forward responses, the RESET voltage is typically negative and the SET voltage positive. "Steps" refer to the distance between measurement points, corresponding to contiguous points of applied voltage. The higher the number of points, the smoother and more regular the obtained curve will be. Based on the voltage range and the step distance, the total number of steps is calculated automatically.

It's also possible to define a "compliance intensity," which prevents very high measured current values from exceeding this limit and potentially damaging the device.

Finally, the "holding time" refers to the waiting time before starting the I/V Sweep, affecting only the first measured point. In contrast, the "delay time" is applied at each measurement point, slowing down the process and allowing the tested device to return to equilibrium states between each step. A longer delay time will result in a more accurate current curve, though the time set in the box will be multiplied by the number of steps, considerably slowing down the overall process. Both the holding and delay times can be set to 0s for a simple I/V Sweep. When using a logarithmic scale, negative current values related to the reverse bias regime won't display correctly in the final result. To counteract this, it's necessary to include a function in the "Function" section to plot the absolute value of the measured current. This expression takes the form: a=abs(I2).

In the "Display" section, you can configure the axes, scales, and data shown in the resulting plot once an I/V Sweep measurement is completed. It's important to select parameters V1 and a as the x and y variables of the graph.

Figure A.1.2 shows a plot exemplifying an I/V Sweep with a voltage range of -4V $\rightarrow$ 4V $\rightarrow$ -4V and 20mV steps.

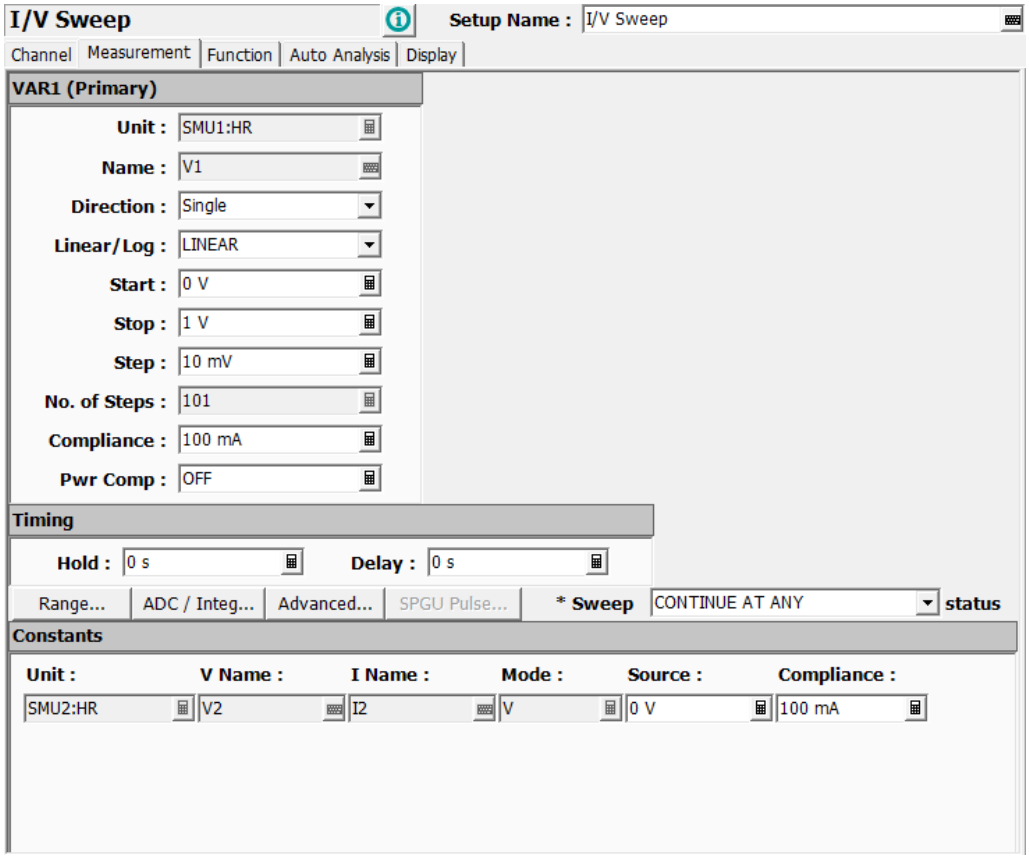


Figure A.1.1: Measurement configuration in I/V Sweep Test mode.

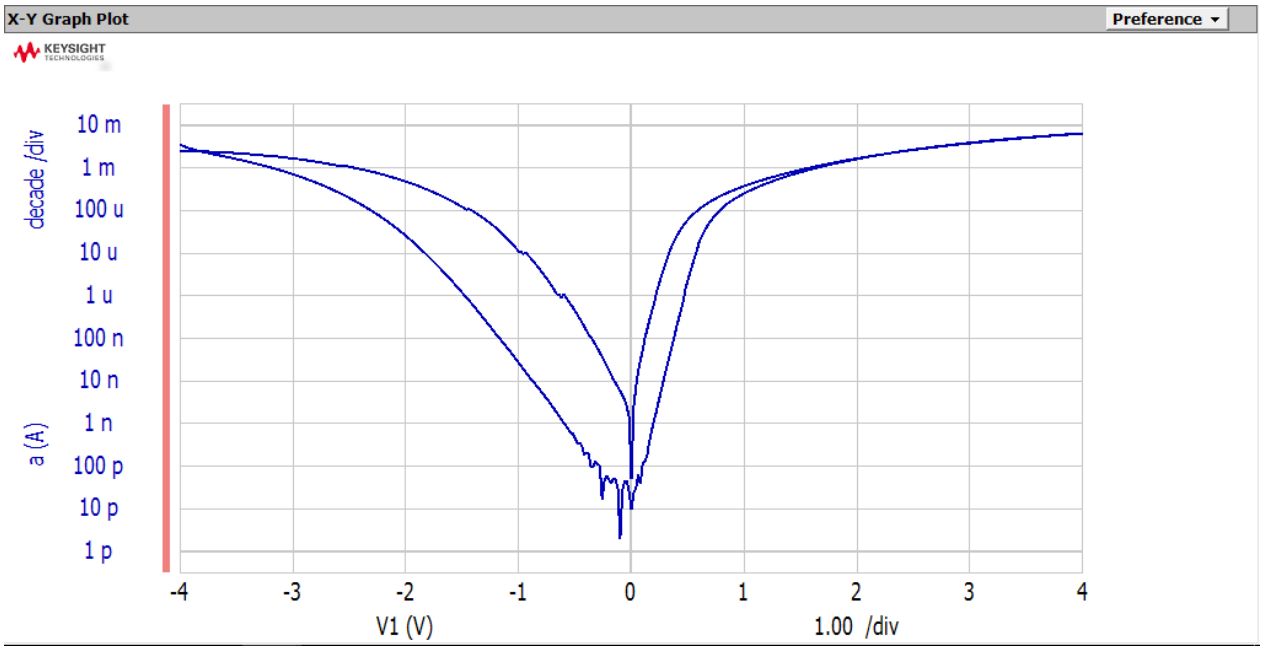


Figure A.1.2: I/V Sweep example of measurement.

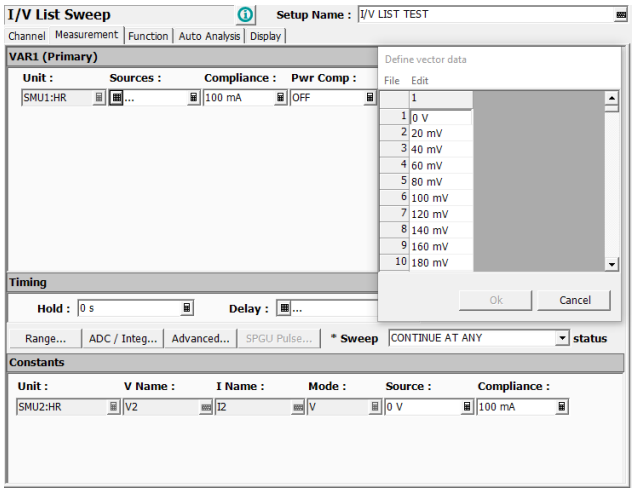
A.2 I/V List Test

Unlike the I/V Sweep mode, where measurement points are automatically set based on step distance and voltage sweep range, the I/V List setup allows for a completely customized data table. This means you can input a series of measurement points with specific applied voltages, enabling you to apply the same voltage repeatedly and modify the step distance as needed.

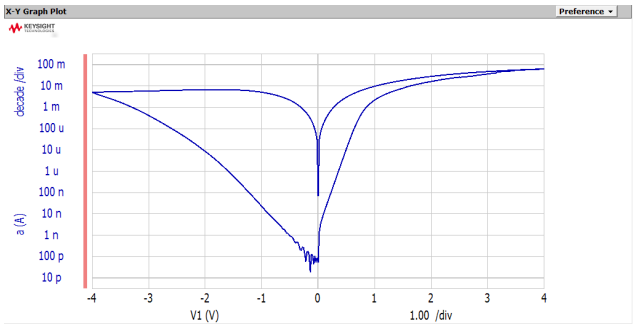
The Channel and Function sections remain the same as in I/V Sweep mode. In the Measurement section, you need to add the desired voltage list, which will constitute each point where the current is measured. The maximum number of points is 1001, and voltage values can be varied as needed. Additionally, in the Display section, you can obtain a list of the output current and its associated voltage points, in addition to the plot of the I/V curves.

This mode can yield the same results as the I/V Sweep mode. Figure A.2.1 shows the current within a voltage range of -4V → 4V → -4V. In the measuring list, voltage values associated with this range were entered with 20 mV separations, simulating the automatic setup generated in the I/V Sweep mode shown in Figure A.1.2.

Furthermore, it's possible to measure current by applying the same voltage constantly by adding the desired value multiple times to the list. Figure A.2.2 displays the I/V plot and a measuring list where a voltage of -600mV in the LRS of Reverse Bias was repeated, and the current variation at that point was measured. This allows for observing transient current directions and how quickly a device reaches an equilibrium state (completing a full loop and setting several points with 0 V). Figure A.2.3 shows a similar case for the HRS of Reverse Bias at -600mV.

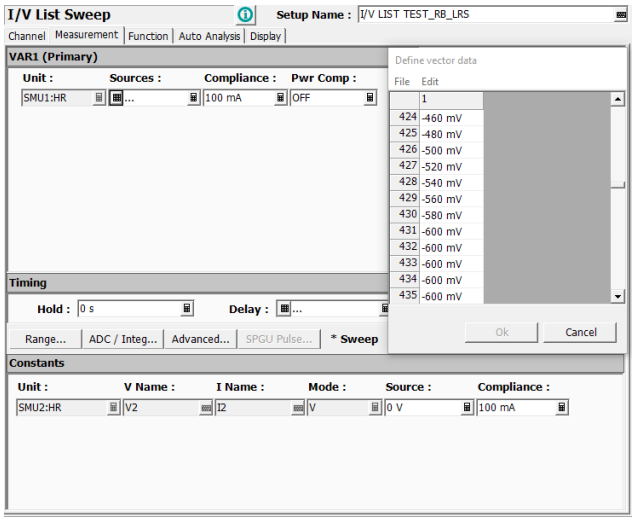


(a) Measurement configuration of I/V List Test measurement of a simple I/V Sweep.

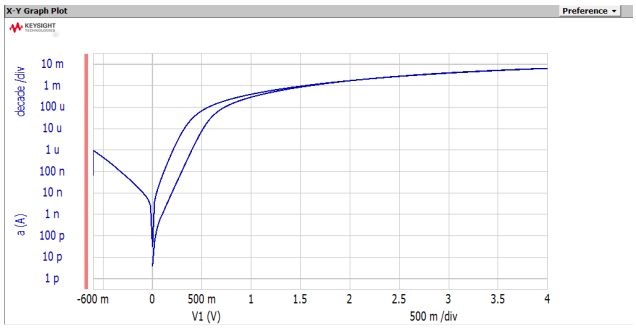


(b) I/V list measurement of a simple I/V sweep.

Figure A.2.1: I/V sweep measurement made using the I/V List Test.

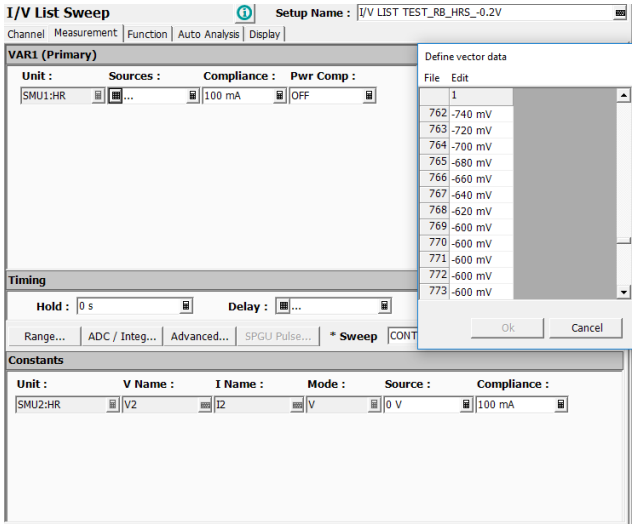


(a) Measurement configuration of I/V List Test measurement of transient current in LRS of reverse bias.

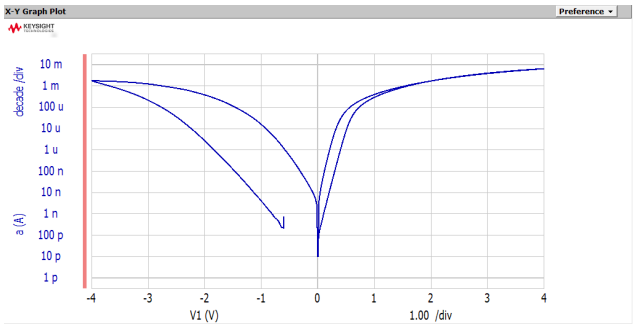


(b) Current variation at constant voltage in LRS in reverse bias.

Figure A.2.2: Example of I/V List Test measurement in LRS of reverse bias.



(a) Measurement configuration of I/V List Test measurement of transient current in HRS of reverse bias.



(b) Current variation at constant voltage in HRS in reverse bias.

Figure A.2.3: Example of I/V List Test measurement in HRS of reverse bias.

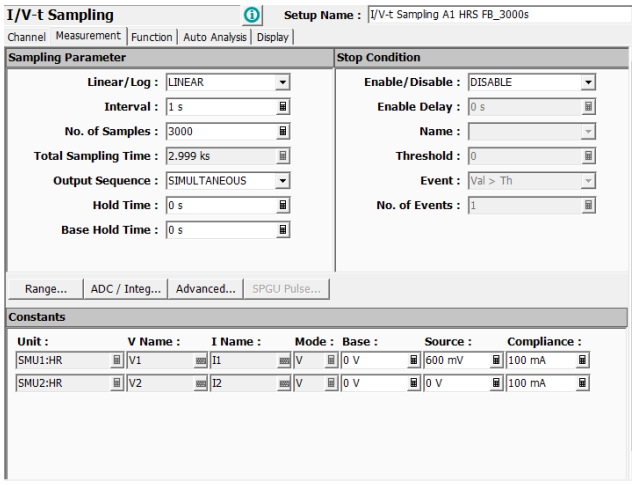
A.3 I/V-t Sample

This mode allows for measuring the output current in response to a constant voltage over time. To do this, you configure the parameters for the desired voltage and time period within the Measurement section, as shown in Figure A.3.1a.

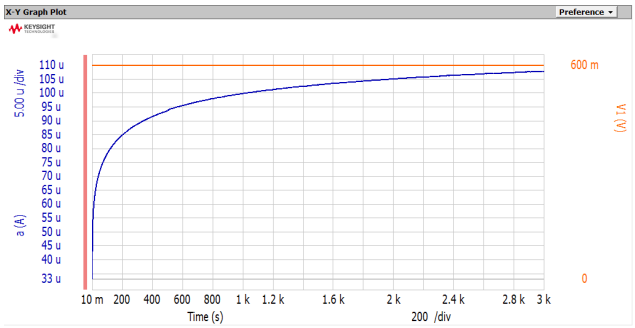
The "time interval" refers to the temporal distance between two measurement points, similar to how voltage steps functioned in previous modes. Additionally, you can set the total number of points, or "number of samples." By multiplying the interval and the number of points, the computer automatically calculates the corresponding total measurement time.

The "output sequence" lets you choose whether the voltage and current lines are displayed separately in different plots or if they should be shown simultaneously without any time delay.

The bottom window, reserved for constants, is where you establish the dependent and independent variables. To observe the effects of voltage on the current generated by the device under test, you must set a potential difference between the source and the base of the circuit, while ensuring no external current is supplied to the system. This arrangement would be inverted if you intended to analyze the effects of applying a current to the circuit on the voltage. Figure A.3.1b corresponds to the output current results after setting a constant voltage of 600mV for 3000s.



(a) Measurement configuration of I/V-t Test.



(b) Current variation over time at constant voltage in HRS in forward bias.

Figure A.3.1: Example of I/V List Test measurement in HRS of reverse bias.

A.4 WGFMU

The WGFMU allows for the highly precise and detailed generation of both voltage and current waveforms, making it essential for transient characterization. Figure A.4.1 provides an overview of the parameters that can be determined using this mode. The diagram in the top-right corner of the screen exemplifies the typical WGFMU process: a waveform is configured to supply a specific voltage pulse for a defined duration (blue line). Additionally, it shows the precise moments at which the output current measurement points are set, along with their respective intervals (green line).

A.4.1 Channel Configuration

WGFMU1 corresponds to the waveform generated by Channel 1. The image shows that this channel is responsible for measuring the voltage pulse applied to the device under test, as "Fast IV V measurement" has been selected in the OperationMode1 option. The "Initial Measurement Range" option establishes the voltage range, which must be adapted to each situation based on the maximum and minimum applied voltage values.

On the other hand, the WGFMU2 menu corresponds to the waveform measured by Channel 2. The configuration regarding the OperationMode2 in the image shows that this channel is intended to measure the output current of the device under test via the "Fast IV I measurement" option. Setting the current range is crucial for obtaining clear and sharp results without any compliance issues or noise from the devices. Possible ranges include from 1µA to 100mA. Both Channel 1 and Channel 2 can be enabled or disabled. If both are enabled, the final plot will display both the applied voltage lines and the measured output current from the device.

A.4.2 Pattern Configuration

Next, the generated waveform and the measuring events must be configured in the Pattern section. The "Waveform Channel 1" option is used to configure the shape of the voltage pulse, which is done through the list shown in Figure A.4.2a. In the first column, time values must be entered, while in the second column, the desired voltage values to be applied at each defined point are entered. In this way, each row corresponds to an inflection point in the generated waveform, denoted as $t_w(x)$. For example, in the figure, the first point $t_w(1)$ is associated with row 1, where at instant 0s, the initial pulse voltage is 0V. In the second row, $t_w(2)$ is set at instant 0.05s, where the voltage should acquire a value of 2V. Between points $t_w(1)$ and $t_w(2)$, the voltage waveform automatically transitions linearly from 0V to 2V in 0.05s. Overall, the voltage pulse generated by Waveform Channel 1 is 0V $\rightarrow$ 2V $\rightarrow$ 0.4V, where the 2V voltage is maintained for one second between $t_w(2)$ and $t_w(3)$, and the 0.4V voltage is also constant for 3 seconds between $t_w(4)$ and $t_w(5)$.

"Waveform Channel 2" refers to the duration of the voltage pulse. Figure A.4.2b shows the list that appears during the configuration of this option. In the example shown, the voltage pulse is displayed from 0s to instant 4s, which corresponds exactly to the duration of the waveform generated in Channel 1. Although this is usually the most common case, it is possible to set a display time longer than the voltage pulse. However, it is not possible to set a display time shorter than the duration of the voltage pulse established in Waveform Channel 2.

Finally, the measurement points of the output current must be modulated through the table shown in Figure A.4.3. In column 1, the starting time of each measuring event, denoted as $t_m(x)$, must be added. Measuring events consist of points and intervals, which are set in columns 2 and 3, respectively. The "number of points" refers to very small time instances where output current measurements are performed. Each of these instances is not a single measuring point; rather, each point comprises a time interval where numerous measurements are conducted for greater precision. By multiplying the number of points and the time interval established for each, the total duration of the specific measuring event is obtained. Each point of the measuring event, where multiple current measurements are performed, must display a single current value. To achieve this, column 4 is used to define time periods within each interval where all measured current values are averaged. The time cycles in column 4 must be smaller than the interval times in column 3. Columns 4 and 5 serve to set a voltage and current range during the display, although it's usually not necessary to use them as they

have already been established previously.

It is extremely important to note that the total number of points across all measuring events cannot exceed 20000. It is possible to add more rows to configure more measuring events, but their initial temporal instants cannot overlap. In the case of Figure A.4.3, the measuring event in row 1 has 4000 points and intervals of 0.001s, corresponding to a total duration of 4 seconds. If a second measuring event were to be added in row 2, its initial instant established in column 1 must be greater than or equal to $t_m(2) = 4s$. Additionally, the sum of the total points of measuring events 1 and 2 could not exceed 20000. The total duration of all measuring events cannot exceed the display time added in the Waveform Channel 2 window. The lowest values that can be added in in column 3 and 4, referring to the interval and averaging time, are 10^{-8} s and 10^{-9}s.

Failure to meet any of these conditions will result in an error message, while a correct configuration of all parameters can lead to the plot shown in Figure A.4.4.

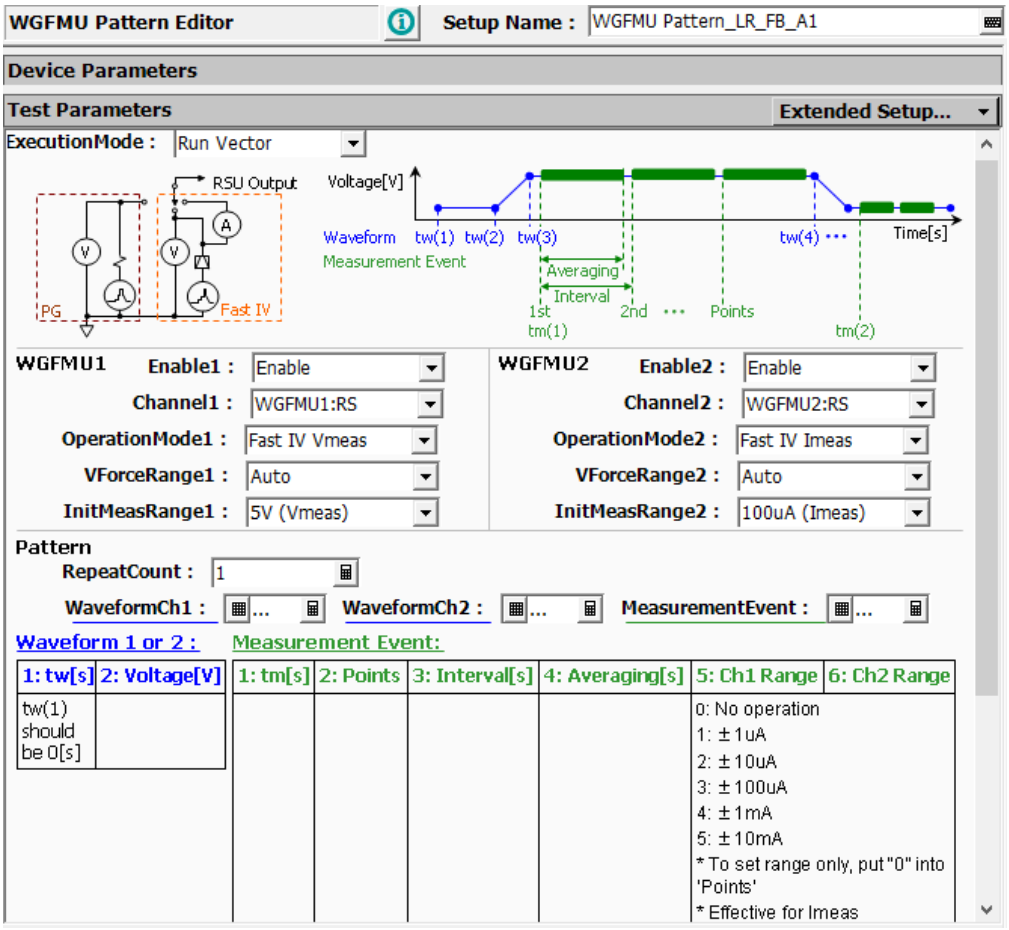
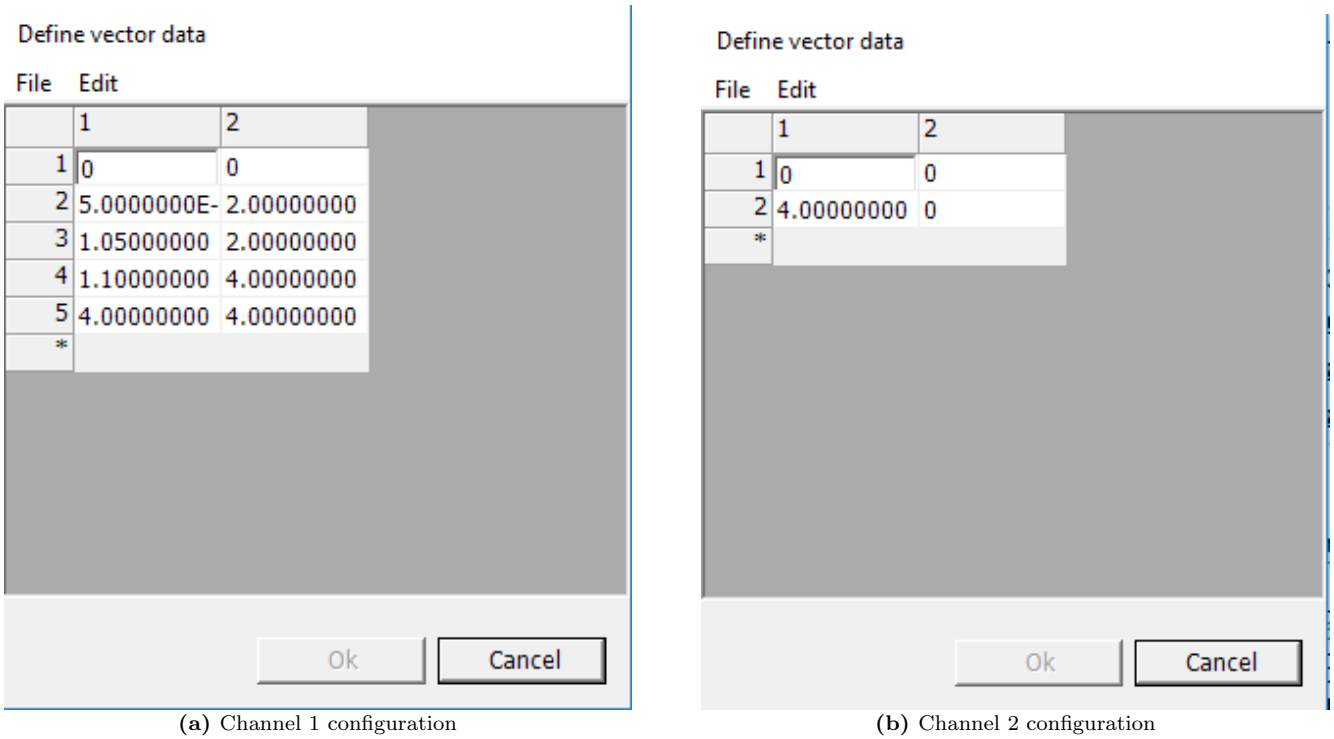


Figure A.4.1: Measurement configuration in WGFMU mode.



(a) Channel 1 configuration **(b)** Channel 2 configuration

Figure A.4.2: Waveform channels configuration

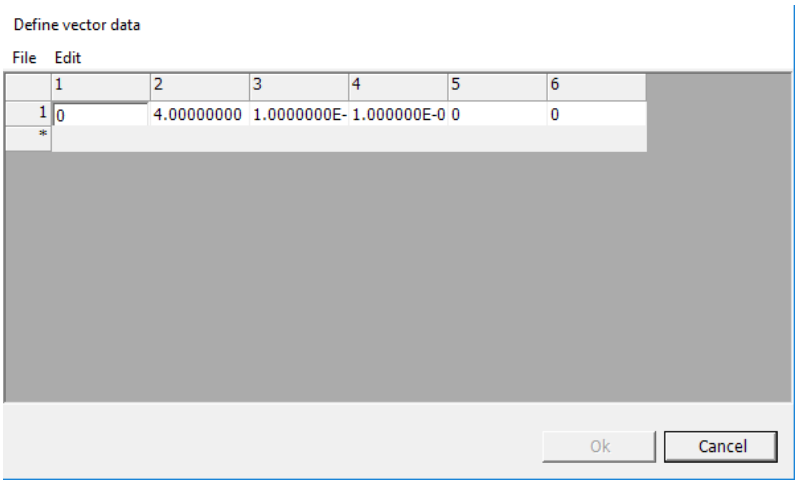


Figure A.4.3: Measuring events configuration.

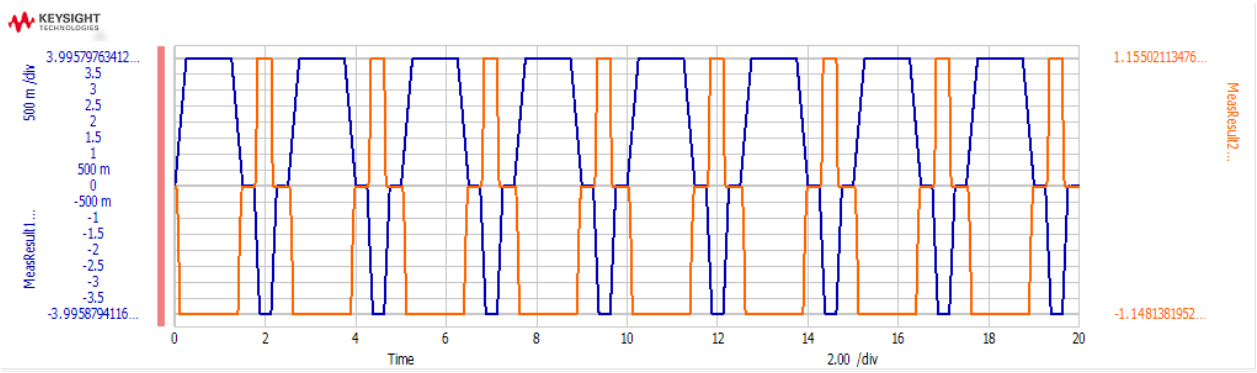
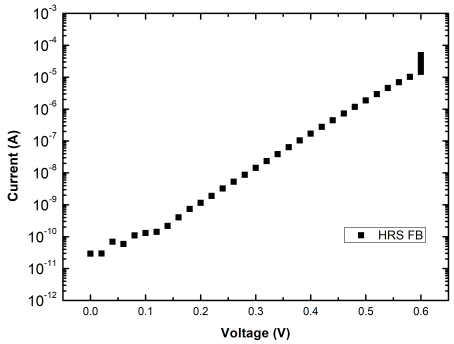


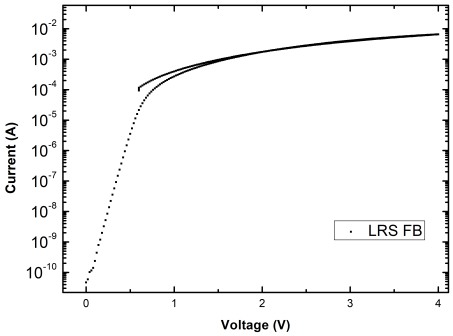
Figure A.4.4: Writing voltage pulse and output current measured with the WGFMU mode.

Chapter B Supplementary Plots

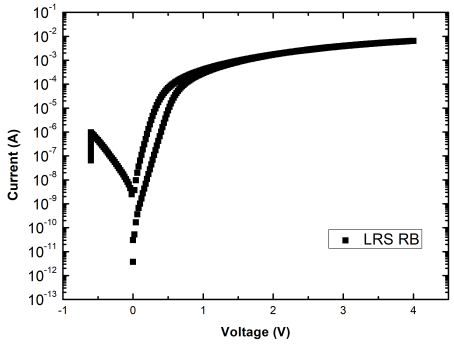
B.1 Resistance Time Dependence at Constant Voltage Pulses



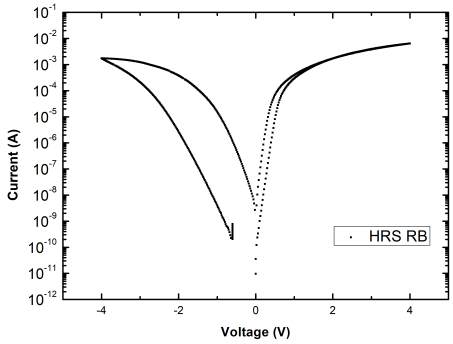
(a) HRS of forward bias



(b) LRS of forward bias

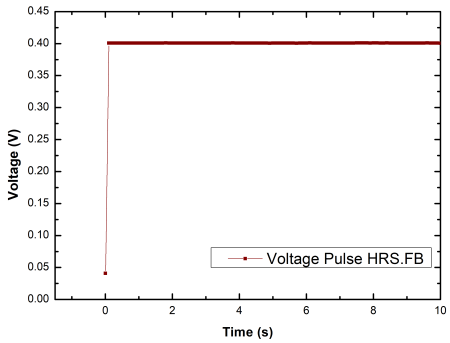


(c) LRS of reverse bias

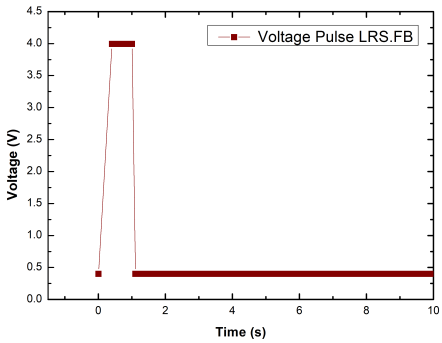


(d) HRS of reverse bias

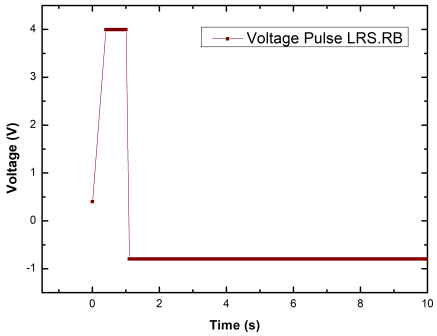
Figure B.1.1: Resistance changes in the current at constant voltage in every state using the I/V List Test.



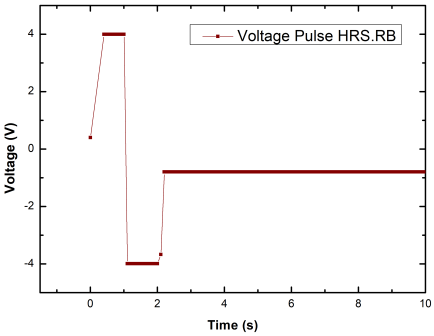
(a) Writing voltage pulse to access the HRS in forward bias.



(b) Writing voltage pulse to access the LRS in forward bias.



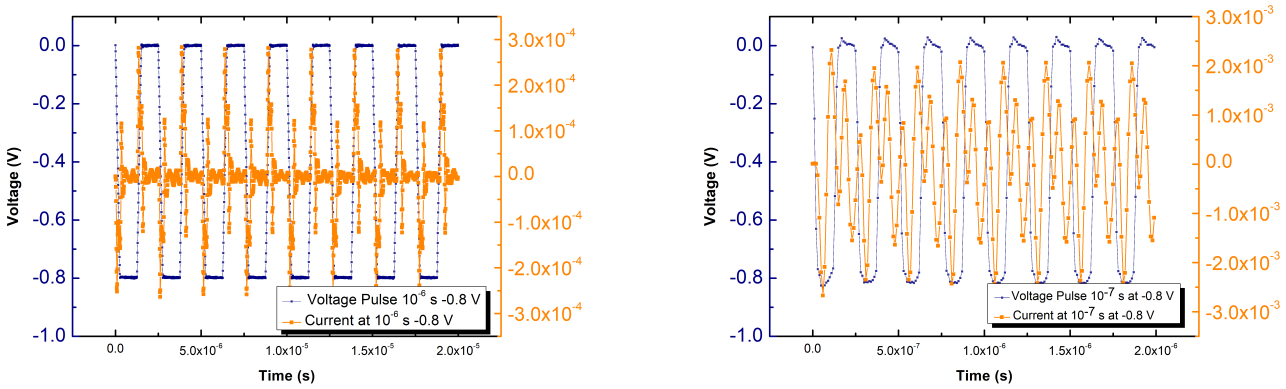
(c) Writing voltage pulse to access the LRS in reverse bias.



(d) Writing voltage pulse to access the HRS in reverse bias.

Figure B.1.2: Writing voltage pulses to access every state before applying a constant voltage.

B.2 Time Range Measurements



(a) Resulting current from voltage pulses in the microsecond time range.

(b) Resulting current from voltage pulses in the 100 nanoseconds time range.

Figure B.2.1: Time range