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Fabrication and Electrical Characterization of Memristive MIS Junctions on Nb:STO

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Contents

Abstract

As traditional semiconductor architectures approach their physical and energy-efficiency limits, alternative computing paradigms are required to address the von Neumann bottleneck characterized by high latency and separate memory-computation pathways. Memristors offer a promising route toward non-von Neumann analog computing by enabling co-location of memory and computing within the same physical unit. This work investigates the fabrication and characterization of a metal–insulator–semiconductor (MIS) memristive device, composed of cobalt as the metal, an ultra-thin plasma oxidized aluminum oxide (Al_2O_3) insulating layer, and a niobium-doped strontium titanate (Nb:STO) semiconducting substrate.
The MIS architecture is designed to mitigate limitations observed in conventional Schottky junctions on oxide semiconductors, such as poor interface reliability and switching ability. A 0.7 nm Al_2O_3 layer is deposited via electron beam evaporation and subsequently plasma-oxidized to ensure a high-quality insulating barrier. This tunnel barrier modulates the electrostatic interface, reducing the effective barrier width. Additionally, device miniaturization reveals a clear edge effect under reverse bias conditions, where electric fields are intensified near the perimeter, leading to improved resistance modulation and tunability of intermediate states.
Fabrication was carried out using UV lithography, including the definition of isolation barriers and metal contact deposition, resulting in ten devices of two distinct micrometer-scale areas. Electrical characterization via current–voltage (I–V) measurements confirms excellent reproducibility within each area, with negligible device-to-device variation. Furthermore, as device area decreases, the resistive states widen due to enhanced edge field effects, demonstrating increased dynamic range and memristive behavior tunability. These results highlight the potential of MIS-based structures on Nb:STO for scalable, energy-efficient memristive computing applications.

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Lastly, I would like to thank Prof. Dr. Ir. Bart Kooi for acting as my second examiner.

Chapter 1

Introduction

1.1 The Limits of Conventional Computing

The rapid evolution of computing systems over the past decades has been driven by the continuous downscaling of electronic components, in line with Moore's Law [1]. This scaling has enabled ever-increasing transistor densities, culminating in powerful, compact computing hardware. However, as transistor sizes approach atomic dimensions, the benefits of further miniaturization are diminishing. Quantum tunneling, thermal noise, and increased leakage currents pose fundamental barriers to continued scaling [2]. Furthermore, the power density of chips has escalated, creating thermal management issues and limiting the clock frequencies of modern processors, which have largely plateaued since the mid-2000s [3].

Another significant limitation arises from the von Neumann architecture, the model used in most traditional computing systems. In this architecture, processing and memory units are physically separate and communicate via a shared bus [4]. This separation introduces a bottleneck in data throughput, as data must be continually moved back and forth between memory and the CPU, creating latency and energy inefficiency. Known as the von Neumann bottleneck, this constraint restricts the overall performance of computing systems, especially in data-intensive applications [5].

The energy cost of data movement has become a primary concern in computing. As reported in recent literature, data transfer often consumes more energy than computation itself [6]. With the growing demand for high-throughput, low-power processing, particularly in artificial intelligence, big data, and mobile computing, overcoming the limitations of the von Neumann paradigm is critical.

One promising approach to addressing these limitations is neuromorphic computing. Inspired by the architecture of the human brain, neuromorphic systems co-locate memory and processing, enabling highly parallelized and energy-efficient information processing [7]. The human brain, for instance, operates at roughly 20 W while managing trillions of synaptic connections and performing complex cognitive tasks [8]. Unlike conventional systems, the brain processes information in a distributed manner, with memory and logic intertwined in the form of synapses and neurons.

Implementing brain-like architectures using standard CMOS technology is prohibitively complex and power-intensive [9]. Thus, there is a immense need to develop novel device technologies that intrinsically combine memory and computation. The most promising candidate to achieve this are memristors, two-terminal resistive switching devices capable of mimicking synaptic behavior with high energy efficiency. These devices form the hardware foundation for next-generation, non-von Neumann computing systems.

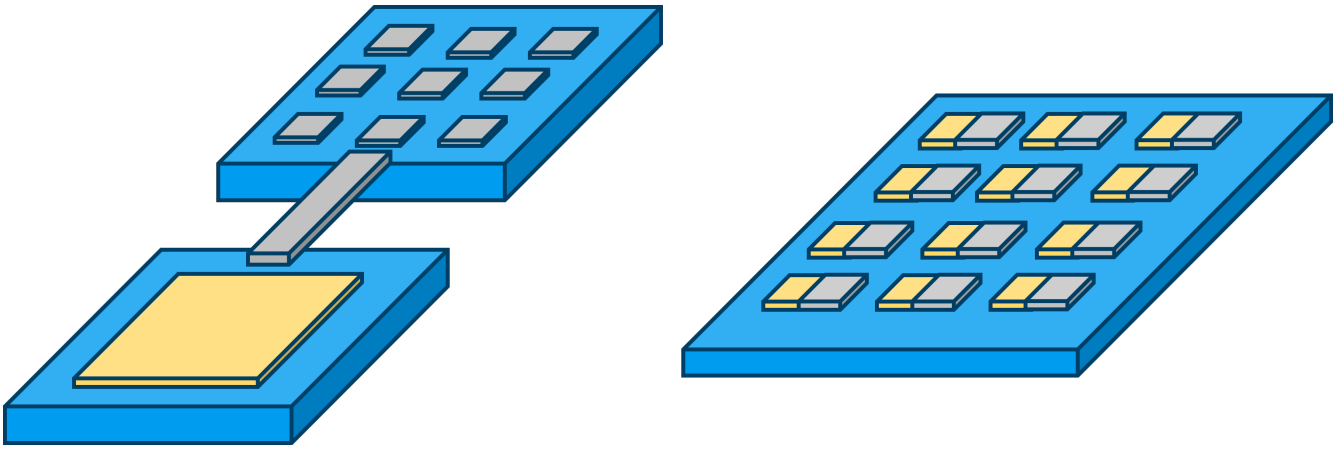


Figure 1.1: Image of the schematics of (left) the von Neumann bottleneck where CPU and memory are seperated and (right) the coexistence of memory and CPU in a memristive device.

1.2 Memristors and Resistive Switching

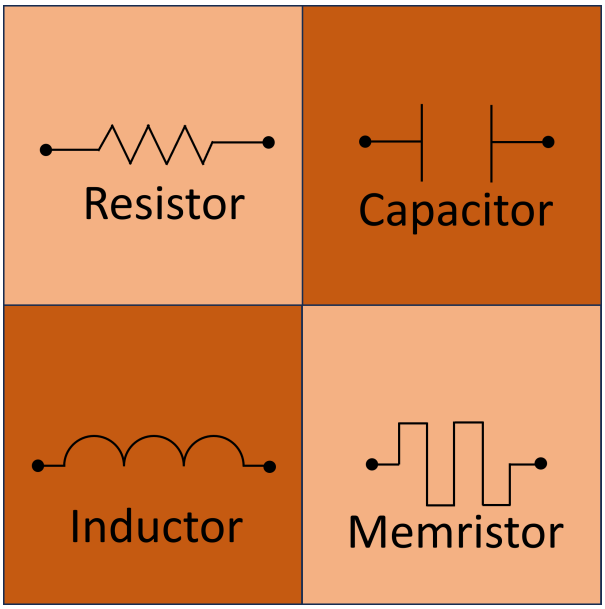
As conventional computing systems face challenges from scaling limits and energy inefficiencies, alternative hardware paradigms are being explored to overcome these fundamental constraints. One of the most promising approaches is the use of memristive devices—two-terminal components capable of storing and processing information through resistance modulation [10, 11]. These devices offer a hardware-level solution to the von Neumann bottleneck by unifying memory and logic operations within a single structure.

Originally conceptualized by Chua in 1971 on symmetry grounds [10], the memristor links electric charge and magnetic flux, completing the family of fundamental circuit elements. Today, it is primarily recognized for its characteristic behavior wherein the resistance depends on the history of the applied voltage. This memory-like behavior allows it to retain a resistive state even after the external power is removed, making memristors inherently non-volatile [11].

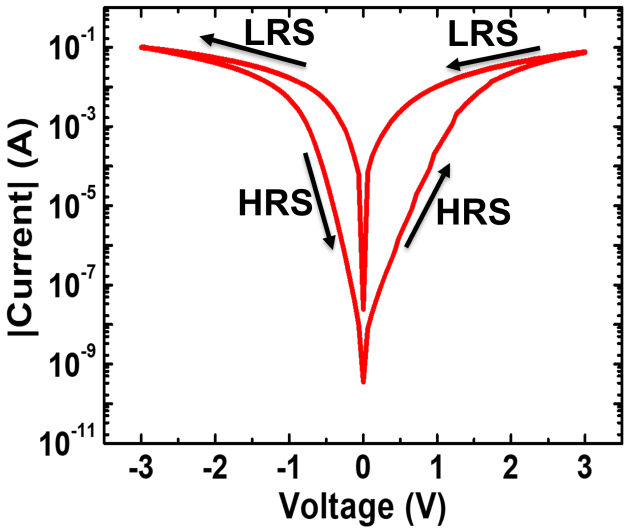
Memristors can be classified as either volatile or non-volatile based on their retention behavior. Non-volatile memristors retain their resistive state even after the external voltage is removed, making them ideal for memory storage applications. Volatile memristors, on the other hand, revert to their original state once the stimulus is removed, behaving more like dynamic switches or selectors. Volatile memristors are attractive for mimicking short-term synaptic dynamics in neuromorphic systems, such as spike-rate adaptation.

Memristive behavior arises from physical mechanisms that modify the internal structure or electronic configuration of the material. A common manifestation is resistive switching, wherein the resistance of a device can be reversibly altered between high-resistance (HRS) and low-resistance states (LRS) by an electrical stimulus [13]. These transitions can be abrupt or gradual, allowing for binary or analog-like state tuning, respectively.

Resistive switching mechanisms can be broadly categorized as filamentary or interfacial, both illustrated in Figure 1.3. In filamentary switching, conductive paths create narrow filaments across an insulating matrix often formed by oxygen vacancies or metal cations. These filaments can be formed or ruptured via electrical pulses, leading to drastic changes in resistance [14]. In contrast, interfacial switching occurs



(a) The four fundamental electrical components; Resistor, Inductor, Capasitor and Memristor, connecting all electrical quantities [12] **Probably different image here**



(b) A memristor shows hysteresis in its I–V curve, switching between high and low resistance states when voltage is applied.

Figure 1.2: Memristors

at the interface between the metal and semiconductor and involves modulation of charge trapping or ion migration in the interface states [15, 16]. Interfacial mechanisms tend to scale better and exhibit more uniform behavior, which is critical for dense device integration and is the method used in this project.

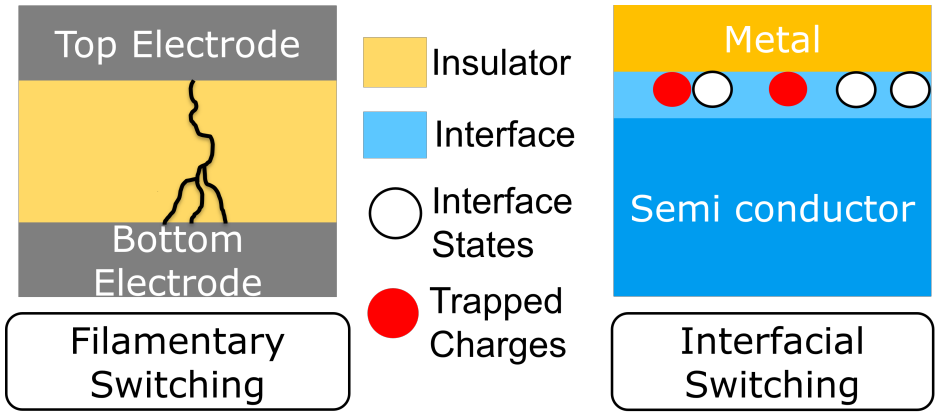


Figure 1.3: Illustration of filamentary and interfacial switching in memristors

The ability of memristors to combine memory and logic functionality makes them ideal candidates for neuromorphic computing architectures. In such systems, memristors can serve as artificial synapses, where the conductance of each device represents a synaptic weight that can be dynamically tuned in

response to electrical stimuli. This imitates biological neural networks, where memory and processing are co-located and operate in parallel manner [6, 7].
Compared to traditional CMOS-based approaches, memristive systems promise significant improvements in power efficiency and scalability. Since data no longer needs to shuttle between separate memory and processing units, the energy consumption for data movement is drastically reduced. Furthermore, their compact two-terminal geometry and compatibility with crossbar arrays enable ultra dense integration and direct hardware implementation of matrix-vector multiplication, an essential operation in machine learning and signal processing [17, 18].
Another compelling feature is the potential for multi-level resistance states, enabling analog computation and in-memory learning capabilities [13]. Such features are essential for developing efficient hardware neural networks that can adapt and reconfigure without the overhead of software-based training. The non-volatility of memristors also ensures that information remains stored without power, making them well-suited for edge computing and low-power applications.
While challenges such as variability, endurance, and integration remain, memristive devices represent a paradigm shift in how information can be stored, processed, and learned. Their ability to alleviate the fundamental inefficiencies of the von Neumann model positions them at the forefront of post-CMOS computing research.

1.3 Scope of this Thesis

This thesis focuses on the fabrication and analysis of a Metal–Insulator–Semiconductor (MIS) junction employing a cobalt top contact, a thin insulating layer of aluminum oxide (Al_2O_3), and a niobium-doped strontium titanate (Nb:STO) substrate, which forms a Schottky junction. The overarching objective is to investigate how introducing a thin isolating barrier between the metal and semiconductor can influence and potentially enhance the electrical behavior of the junction, particularly in the context of interface engineering and charge transport mechanisms.
A key motivation behind this work lies in addressing the limitations associated with conventional Schottky contacts on oxide semiconductors, which often exhibit high leakage currents, poor reproducibility, and interface-related instabilities. By incorporating an ultra-thin Al_2O_3 layer, the MIS structure aims to modulate the electrostatics at the interface, reduce barrier height, and enable a more tunable current-voltage response [19]. This makes it particularly relevant for future device applications that require both high integration density and energy efficiency, such as neuromorphic computing elements and resistive memory cells.
The fabrication process involves a series steps performed in the cleanroom of NanoLab NL, including lithographic patterning for device definition, e-beam evaporation of AlOx (non-oxidated Aluminium Oxide) and subsequent plasma oxidation to form Al_2O_3, and metal deposition for electrical contacts. The fabricated structures are then characterized using current–voltage (IV) measurements to evaluate their electronic properties.
The scope of this work is thus threefold: (1) to establish a reliable method for fabricating MIS junctions with high-quality oxide barriers on Nb:STO; (2) to investigate the memristive behavior of these MIS structures; (3) to analyze how the area of the MIS junctions affects the electronic characteristics of the junction.

Chapter 2

Theoretical Background

2.1 Nb-doped $SrTiO_3$

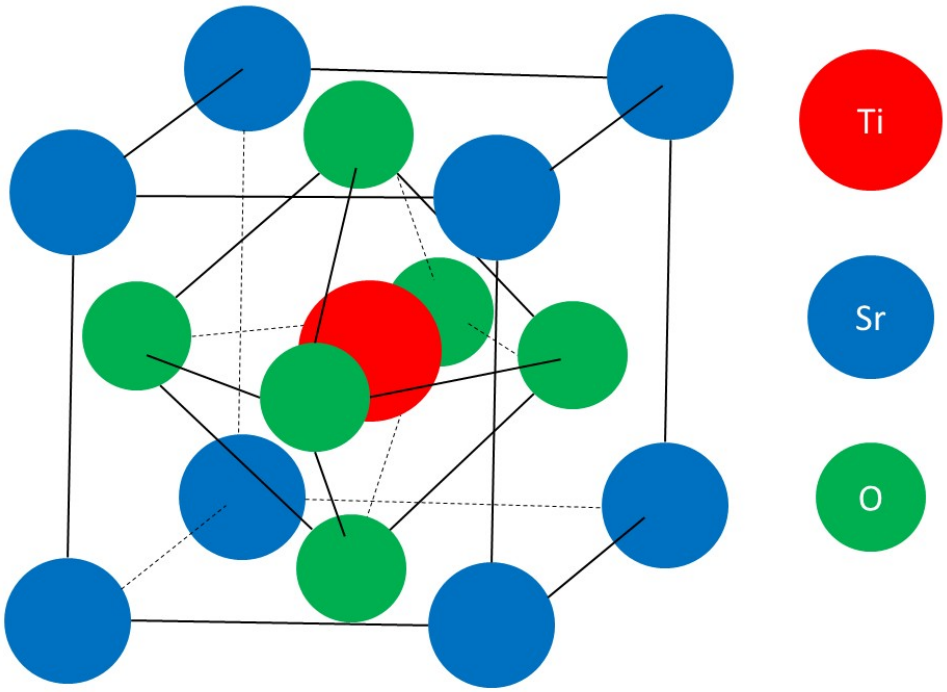


Figure 2.1: Unit cell of STO

Strontium titanate (STO) is a complex perovskite oxide with a cubic crystal structure at room temperature, characterized by the general ABO_3 formula. In this structure, strontium atoms occupy the cubic corners, oxygen atoms are positioned at each face center, and a titanium atom sits at the body center of the cubic lattice. Upon lowering the temperature, STO undergoes a series of structural phase transitions that modify its symmetry and electronic behavior [20].

A particularly remarkable property of STO is its extremely high relative dielectric permittivity (ε_r), which is strongly dependent on both electric field and temperature. This dependence is commonly described by:

$$\varepsilon_r(E,T) = \frac{b(T)}{\sqrt{a(T)+E^2}}$$

where $a(T)$ and $b(T)$ are temperature-dependent fitting parameters. At room temperature ($T = 300\,\mathrm{K}$), typical values are $a = 2.65 \times 10^{15}\ \mathrm{V^2/m^2}$ and $b = 1.42 \times 10^{10}\ \mathrm{V/m}$, yielding $\varepsilon_r \approx 276$ [21–23]. However, at high electric fields, deviations from this model have been observed, suggesting that a more sophisticated treatment is required in these regimes.

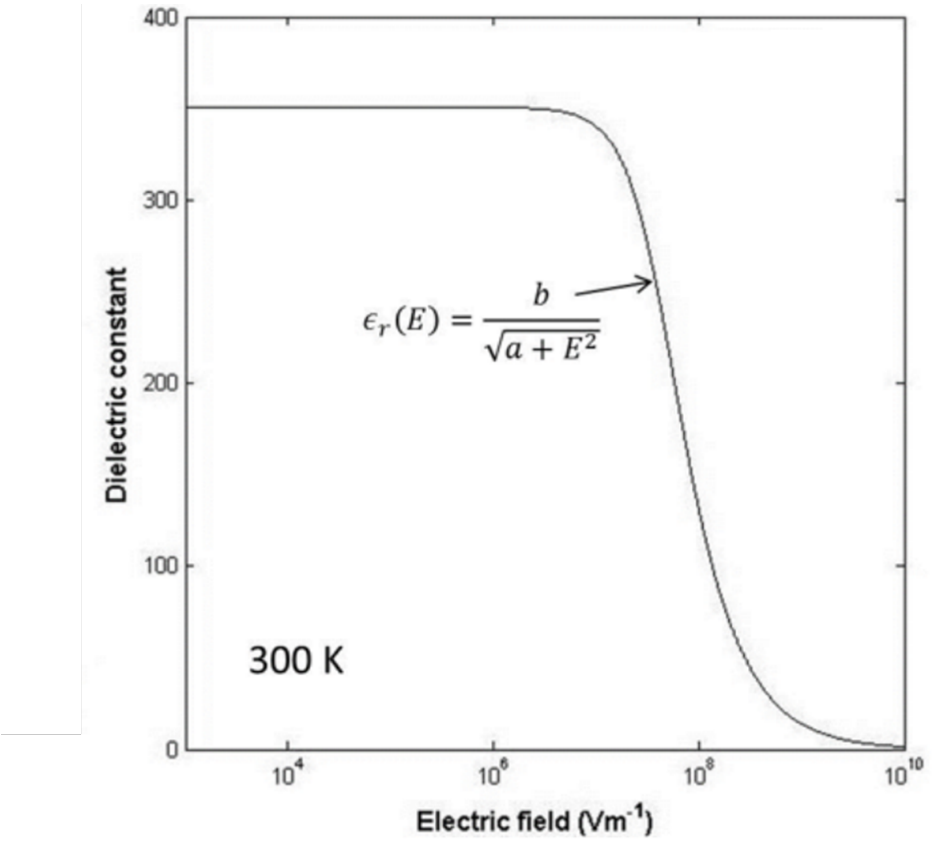


Figure 2.2: The dielectrical permitivity of STO as a function of electric field at 300 Kelvin [24]

In its pristine form, STO is an insulator with a bandgap of approximately 3.2 eV and an electron affinity near 3.9 eV. By substituting a fraction of the Ti^{4+} ions with Nb^{5+}, each dopant contributes an extra conduction electron, rendering the material n-type and significantly enhancing its electrical conductivity. One of the most important features of Nb:STO is its lack of carrier freeze-out at low temperatures. Unlike many conventional semiconductors, where donor electrons become immobile as temperature decreases, Nb:STO maintains an essentially constant carrier concentration down to cryogenic temperatures.
This behavior is well explained by the hydrogenic model of shallow donors, where the donor binding energy is given by:

$$E_D = -13.6\,\mathrm{eV} \cdot \frac{m_e^*}{\varepsilon_r^2}$$

Here, m_e^* is the effective mass of the conduction electrons, and ε_r is the dielectric constant. Due to the very large ε_r of STO, E_D becomes extremely small—on the order of 1.5 meV at 300 K and less than a μeV at 4.2 K. In both cases, these energies are much smaller than the available thermal energy (kT), ensuring that the donor electrons remain ionized over the entire temperature range [25].
At very low Nb doping concentrations, however, some carrier freeze-out can still occur, although the underlying mechanisms remain unclear. At the other extreme, high doping levels push the Fermi level above the conduction band minimum, transitioning the system into a degenerate semiconductor regime with metallic-like behavior.
Overall, the combination of field-tunable permittivity, robust low-temperature conductivity, and compatibility with oxide-based device fabrication makes Nb:STO a compelling platform for research and technological applications, particularly in Schottky junctions and memristive architectures [26].

2.2 Metal-Semiconductor Junction

A Schottky junction is formed when a metal comes into direct contact with a semiconductor, creating a rectifying interface due to differences in their electronic properties. Specifically, the discrepancy in the work functions between the metal (ϕ_m) and the semiconductor (ϕ_s) required charge transfer to equilibrate their respective Fermi levels (E_F). This alinment results in characteristic energy band bending and the formation of a potential barrier at the interface.

2.2.1 Formation of the Schottky Barrier

Initially, when the metal and semiconductor are isolated, their Fermi levels are misaligned. The n-type semiconductor's Fermi level ($E_{F,S}$) lies higher in energy than that of the metal ($E_{F,M}$), due to the lower work function of the semiconductor (ϕ_s), illustrated in figure 2.1. Upon electrical contact, electrons flow from the semiconductor into the metal to align their Fermi levels.
The migration of electrons leaves behind ionized donor atoms, which are immobile and contribute a net positive space charge in the semiconductor. This space charge is balanced by an accumulation of negative charge at the metal surface.
The spatial separation of these charges establishes an internal electric field directed from the semiconductor (positive) towards the metal (negative). This field induces upward bending of the conduction band (E_C) and valence band (E_V) near the interface, creating a potential energy barrier for electron transport. Now the depletion region is formed, which has a width of W. The height of this barrier, ϕ_b, in the ideal Schottky-Mott limit, is given by:

$$\phi_b = \phi_m - \chi_s \tag{2.1}$$

where χ_s is the electron affinity of the semiconductor.
The potential difference across the semiconductor resulting from this band bending, called the built-in potential (V_{bi}), is defined as:

$$V_{bi} = \phi_m - \phi_s \tag{2.2}$$

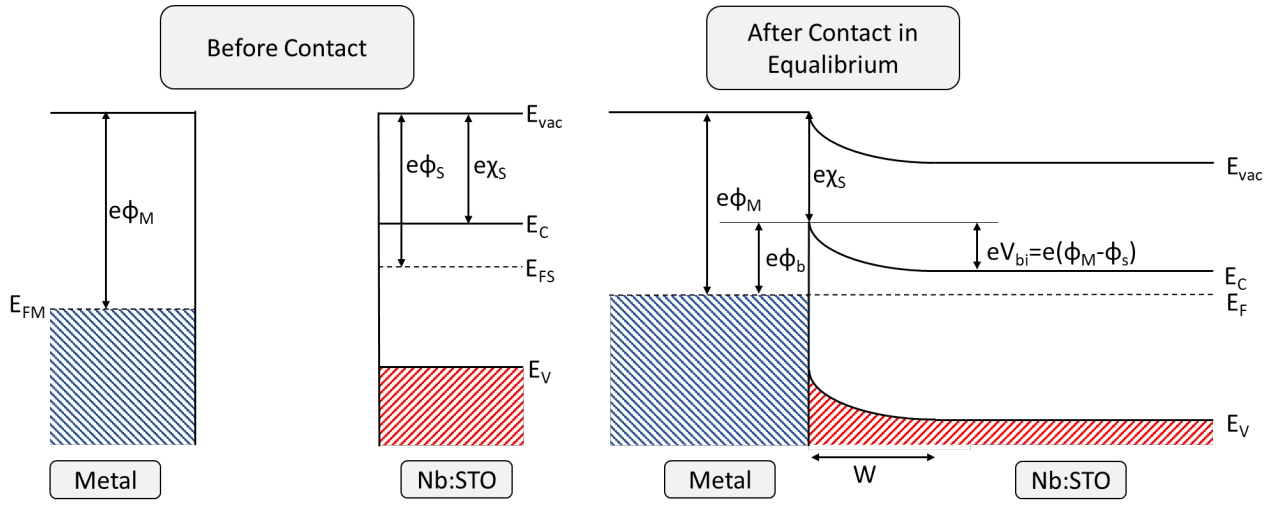


Figure 2.3: Schematic illustration of a Schottky junction before and after contact, with the metal on the left and the Nb:STO on the right.

This built-in potential quantifies the energy difference that must be overcome for electrons to move from the semiconductor into the metal in equilibrium.

2.2.2 Schottky Junction under Bias

When a voltage bias is applied to the Schottky junction, the equilibrium condition is perturbed, altering the potential barrier and depletion width:
Applying a positive voltage to the metal relative to the semiconductor raises the semiconductor's Fermi level with respect to the metal's, called the forward bias. This reduces the effective barrier height, decreases the depletion width, and weakens the internal electric field, illustrated in Figure 2.4. As a result, the diffusion of majority carriers, electrons, from the semiconductor into the metal dominates, leading to a significant forward current. In this regime, the thermionic emission over the barrier dominates and the tunneling is small.
Applying a negative voltage to the metal relative to the semiconductor lowers the semiconductor's Fermi level, increasing both the barrier height and the depletion width, called the reverse bias. This strengthens the electric field and further inhibits electron diffusion from the semiconductor to the metal. The resulting current is primarily due to minority carrier drift from the metal to the semiconductor side. In this regime, tunneling through the barrier from metal to semiconductor is the dominant charge transport.

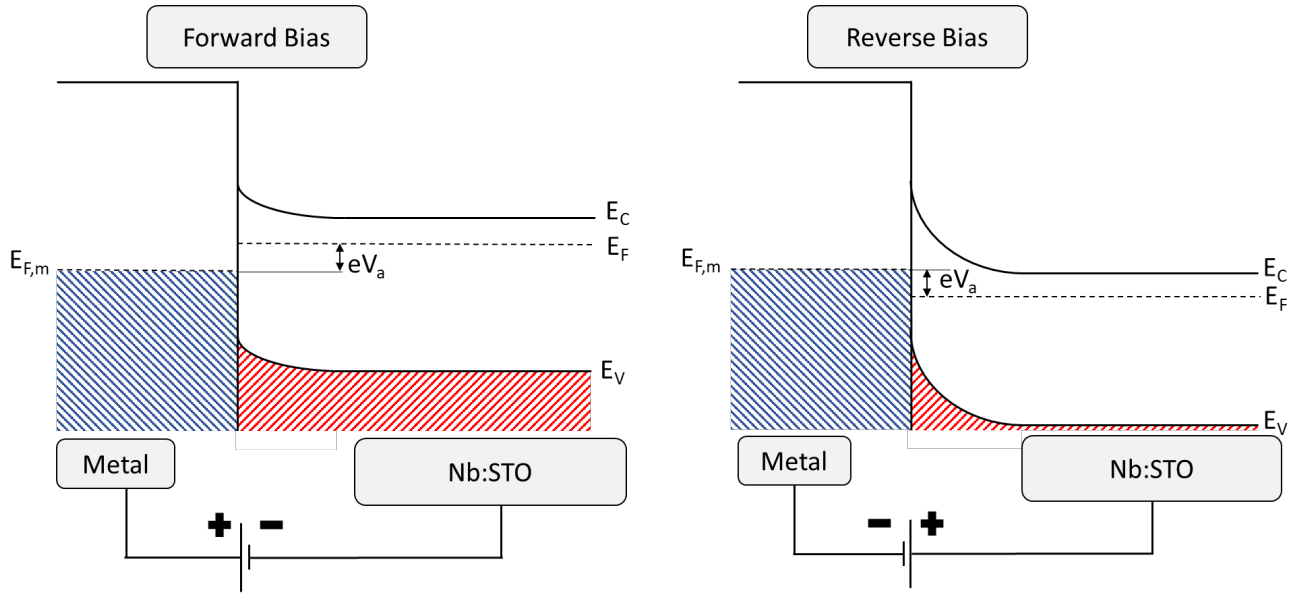


Figure 2.4: Band diagrams of Schottky junction under Forward (left) and Reverse (right) bias conditions

2.2.3 Barrier Height and Width

The width of the depletion region (W) is a crucial parameter in determining the electrostatic properties of a Schottky junction. It depends on the semiconductor's absolute permittivity (ε_s), the donor concentration (N_d), and the applied voltage (V), and is given by:

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V)}{qN_d}} \tag{2.3}$$

where ε_s is the permittivity of the semiconductor material, q is the elementary charge, V_{bi} is the built-in potential, and V is the applied bias voltage. A forward bias ($V > 0$) reduces the depletion width, whereas a reverse bias ($V < 0$) increases it.

The electric field plays a significant role in charge transport across the barrier, particularly through the mechanism of image-force-induced barrier lowering. Due to the interaction between an electron and its image charge induced in the metal, the effective barrier height is reduced as the electric field is reduced. This phenomenon is described by the Schottky barrier lowering:

$$\Delta\Phi = \sqrt{\frac{q^3 N_d}{8\pi^2\varepsilon_s^3}(V_{bi} - V)} \tag{2.4}$$

This shows that the effective barrier height decreases with a positive applied voltage, lowering the total electic field in the depletion region. We also see that the barrier height depends on the electrical permativity of the semiconductor, which plays a crucial role when Nb:STO is used, further explained in Section 2.1.

2.3 Effect of Al_2O_3 Interlayer

Introducing an ultra-thin Al_2O_3 layer between the metal and the Nb:STO substrate fundamentally modifies the electrostatic characteristics of the junction. In a conventional Schottky contact, the full potential drops across the depletion region of the semiconductor. However, in a metal–insulator–semiconductor (MIS) structure, the inclusion of an insulating barrier with a significantly lower dielectric constant ($\varepsilon_r \sim 9$ for Al_2O_3) compared to Nb:STO ($\varepsilon_r \sim 300$) leads to a change in voltage drop [27].
As a result, most of the applied voltage is dropped across the Al_2O_3 layer, leaving only a small portion across the semiconductor. This redistribution reduces the width of the depletion region within Nb:STO and concentrates the electric field in the semiconductor. The thinner depletion width and facilitate enhanced carrier injection, thereby increasing the current under both forward and reverse bias conditions. However, as the width reduction is the most beneficial for the tunneling current, this would have the biggest impact on the reverse current.
In MS junctions on Nb:STO the switching behavior is caused by interface states between the semiconductor and the metal. These states can trap and de-trap charges, causing the high resistance and low resistance states respectively [24]. When introducing the tunnel barrier we add interface states, in the insulator semiconductor interface.

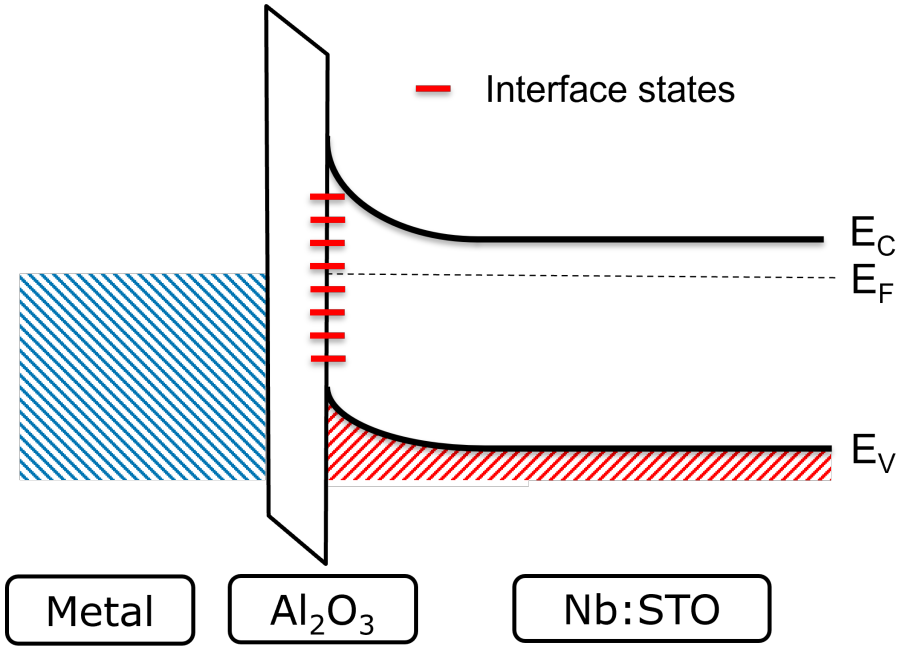


Figure 2.5: Interface states on the insulator-semiconductor interface

2.3.1 Charge Transport Mechanisms

The charge transport in the MIS junction is governed by a combination of mechanisms, depending on the bias polarity. Under forward bias, current primarily flows via thermionic emission (TE) over the reduced Schottky barrier, combined with trap-assisted tunneling (TAT) through defect states within the Al_2O_3 barrier or at the interface. In this bias the TE is the dominant transport.

In reverse bias, the transport is dominated by tunneling processes. Fowler–Nordheim (FN) tunneling occurs through the triangular-shaped barrier under high electric fields. Additionally, Poole–Frenkel (PF) emission contributes, where electrons are thermally excited from trap states into the conduction band, assisted by the electric field lowering the trap potential barriers. Trap-assisted tunneling (TAT) provides a further pathway where electrons hop between defect states across the barrier. Direct tunneling (DT) also contributes, particularly in regions where the tunnel barrier is sufficiently thin.

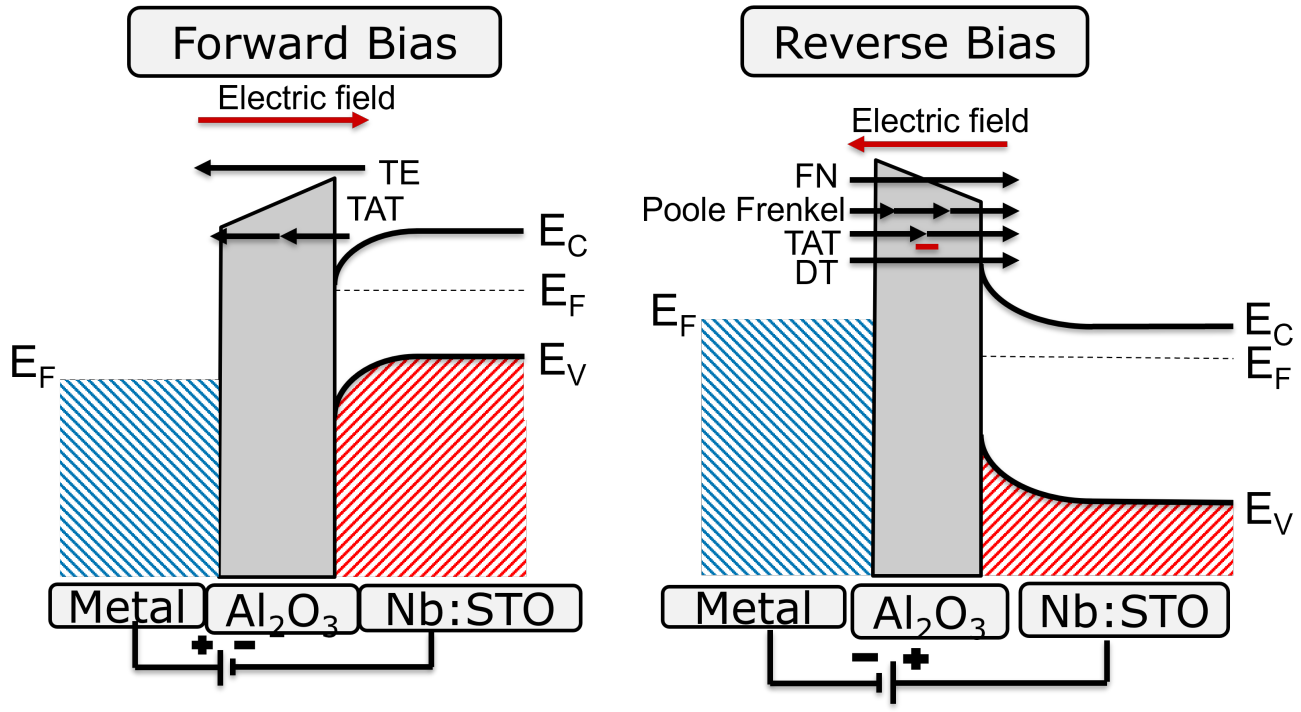


Figure 2.6: Charge transport in MIS junction

Chapter 3

Device Fabrication

3.1 Surface Preparation

The fabrication process of the MIS junction begins with substrate preparation to ensure a clean surface. This involves sequential chemical cleaning steps treatments to remove organic residues and prepare the Nb:STO surface for thin-film deposition. This is achieved by placing the substrate in an ultrasonic bath, acetone and isopropanol (IPA). The goal is to achieve surface suitable for forming high-quality interfaces.

3.2 Spin Coater and Mask Aligner

Following the cleaning process, the substrate is prepared for photolithography by applying a uniform layer of photoresist (PR) through spin coating. Initially, the substrate undergoes a prebake at 90 °C for 60 seconds to evaporate any residual moisture or solvents that may be present on the surface.
Subsequently, the substrate is placed on the spin coater chuck, where it is secured using vacuum suction. One or two droplets of photoresist are dispensed onto the center of the substrate. The spin coater then spins at 4000 rpm for 60 seconds, spreading the photoresist evenly across the surface by means of centrifugal force and producing a uniform thin film.
After spin coating, a postbake is performed at 90 °C for another 60 seconds. This step serves to evaporate remaining solvents within the photoresist and allows any air bubbles formed during coating to rise to the surface, ensuring optimal film quality for the subsequent exposure process.
Once postbaked, the substrate is transferred to the mask aligner for photolithographic patterning. In this step, the photoresist layer is selectively exposed to ultraviolet (UV) light through a patterned photomask. The mask contains alignment markers, which ideally are positioned to match the corners of the substrate. These markers are crucial for multilayer lithography processes, as they enable accurate alignment of successive masks with previously defined patterns on the sample.
Following alignment, the substrate is exposed to UV light for approximately 20 seconds. The UV exposure induces a chemical change in the photoresist, the nature of which depends on the type of resist used. For a positive resist, the exposed regions become more soluble in the developer solution and are subsequently removed during development. For a negative resist, UV exposure causes cross-linking in

the exposed regions, making them more resistant to the developer; in this case, the unexposed regions are removed.
This lithographic process defines the pattern required for the deposition.

3.3 Electron Beam Evaporator

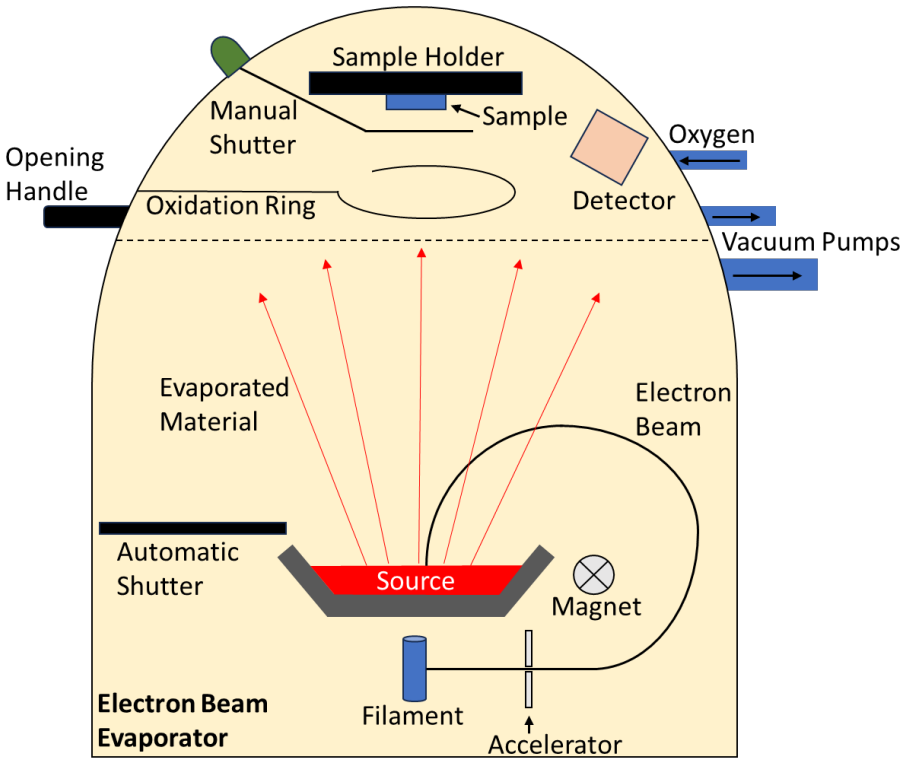


Figure 3.1: Schematic representation of the interior of the electron beam evaporator used during deposition.

Figure 4.3 illustrates the key components of the electron beam evaporator, Temescal Thin Film Coater 2000 (TFC-2000), used for deposition in this project. The system is divided into two main chambers: a high-vacuum deposition chamber and a loading dock, separated by a gate valve (dotted line in the schematic).
During operation, the loading dock is initially pumped down to a medium vacuum of approximately 10^{-2} mbar. Once this pressure is reached, the gate valve is opened, allowing the entire system to equilibrate. The combined chamber is then pumped down to a high vacuum of approximately 10^{-6} mbar. This vacuum level is critical to ensure a uniform and uncontaminated deposition, minimizing interactions between evaporated particles and residual gas molecules.
Once the desired vacuum is achieved, the selected source material is positioned in the crucible. An electron beam is generated by heating a filament which emits electrons via thermionic emission. These electrons are accelerated using electromagnetic fields and focused onto the target material by deflection

magnets. The beam is rastered across the source using a controlled magnetic field oscillation to prevent localized overheating and ensure uniform evaporation.
To initiate the evaporation process, the beam power is gradually increased in two stages—initially to 60% power with a soak period, followed by an increase to 80%, allowing thermal stabilization. After stabilization, an automatic shutter opens, allowing the source material to be evaporated.
Deposition thickness is monitored using a quartz crystal microbalance (QCM). The QCM detects changes in its oscillation frequency as mass accumulates on the crystal. From this frequency shift, the deposited thickness is calculated using the known area of the crystal and the density of the source material.
To allow the deposition rate to stabilize before deposition on the actual sample, an initial buffer layer of approximately 10 nm is evaporated onto a closed manual shutter. Once the rate stabilizes at the desired value, the manual shutter is opened, initiating deposition on the substrate.
For the deposition of the insulating layer in the MIS junction, aluminum oxide is first deposited and then oxidized to form Al_2O_3. This oxidation process is discussed in detail in Section 3.4. The oxidation ring generates an oxygen plasma, which reacts with the aluminum oxide layer on the substrate to form Al_2O_3.
Upon completion of all deposition steps, the gate valve is re-closed to isolate the main chamber. The loading dock is then purged with nitrogen until atmospheric pressure is reached. Finally, the sample is retrieved by opening the dock via the external handle.
After deposition, the entire substrate is uniformly coated with the deposited material, including areas that were previously covered with photoresist (PR). To define the desired pattern, a process known as lift-off is used. During lift-off, the substrate is immersed in warm acetone of 50 °C, which dissolves the remaining photoresist. As the PR dissolves, the material deposited on top of it is also removed, leaving behind only the material that was deposited directly onto the exposed regions of the substrate. This results in a clean and well-defined pattern corresponding to the areas not protected by the photoresist during exposure.

3.4 Plasma Oxidation

The insulating layer in a metal–insulator–semiconductor (MIS) junction plays a decisive role in determining the electrical performance of the device. In this project, aluminum oxide (Al_2O_3) was selected as the insulating barrier due to its high dielectric strength, thermodynamic stability, and large bandgap ($\sim$8.8 eV) [28]. However, when Al_2O_3 is deposited via electron beam evaporation, the resulting film often contains a substantial density of oxygen vacancies, particularly when processed under high vacuum and without a reactive oxygen environment. These oxygen vacancies introduce defect states within the bandgap that can facilitate charge transport through the insulating layer, effectively lowering the energy barrier and causing undesirable leakage currents [29].
To mitigate this, the deposited Al_2O_3 layer is subsequently oxidized using oxygen plasma treatment produced by an oxidation ring, illustrated in Figure 4.3. In this setup, a low-pressure oxygen atmosphere of 1E-1 is excited, creating a plasma in reactive oxygen species. These species have significantly higher reactivity than molecular oxygen and are capable of diffusing into the amorphous Al_2O_3 to fill oxygen-deficient sites, which make the barrier layer of Al2O3 with uniform composition.

3.5 Fabrication Procedure

In this section the steps taken in the fabrication are dicussed in detail, using the methods and equipment described before.

3.5.1 Surface Preparation

Initially, the substrate is emerged in a beaker filled with acetone, which is subsequently placed in an ultrasonic bath for 5 minutes at power 9. After this, a sequence of acetone and isopropanol (IPA) is used to ensure the removal of any organic or particulate contaminants. Directly after the rinse with IPA the substrate is blow dried with a nitrogen gun to ensure a dry surface.

3.5.2 First Lithography and Deposition

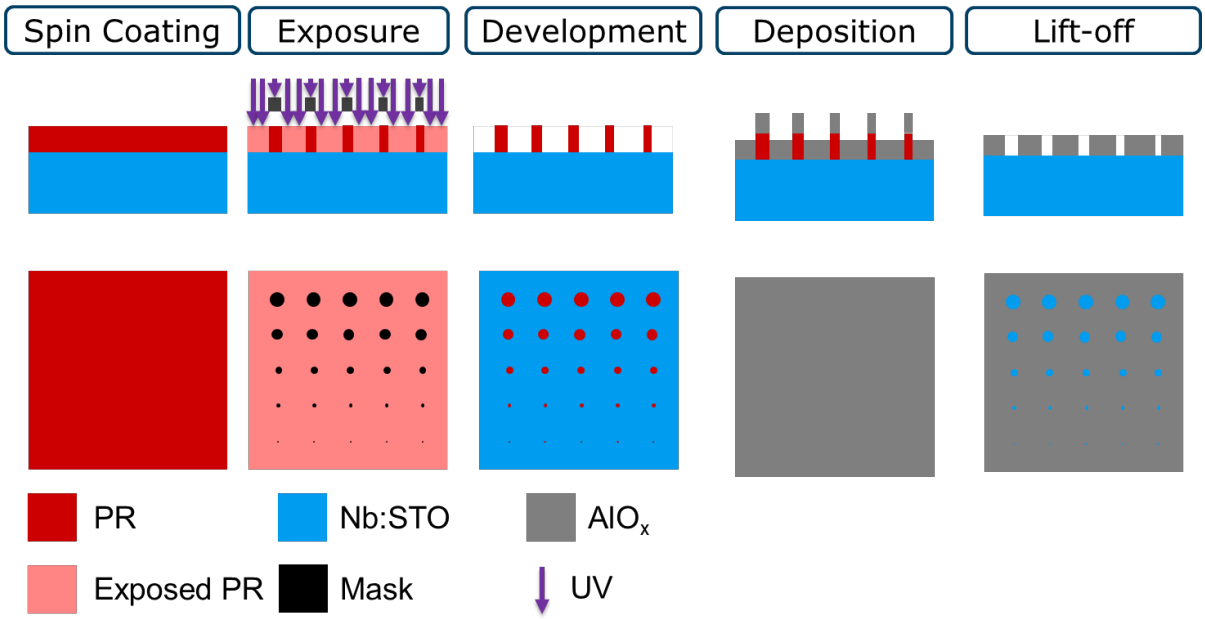


Figure 3.2: Work flow of the fabrication the first lithography and deposition setps, shown in a sectional view (Top) and a top view (Bottom)

After the surface is cleaned, the first step is to isolate the junctions to prevent cross talk from one to the other. This is done by depositing a 50 nm layer of AlOx on the substrate.
First the sample is spincoated with positive PR. After spincoating the sample is transferred to the mask aligner. With this step the area of the junctions is determined. A mask with circular contacts of 5 different areas is used. The radii are 90, 23, 10, 3 and 1 µm. For all the sizes, there are 5 similar devices and this allows us to study the device to device variation.
The photo resist is exposed around the junctions, while the areas of the junctions are covered by the mask. After development there is only PR in the form of the desired junctions. After development the sample is transferred to the electron beam evaporator. Here 50 nm of AlOx is deposited. After the remaining PR

has been lifted off there is a layer of AlOx with holes to the Nb:STO. The MIS pillars will be formed in these holes in the next lithography step

3.5.3 Second Lithography en Deposition

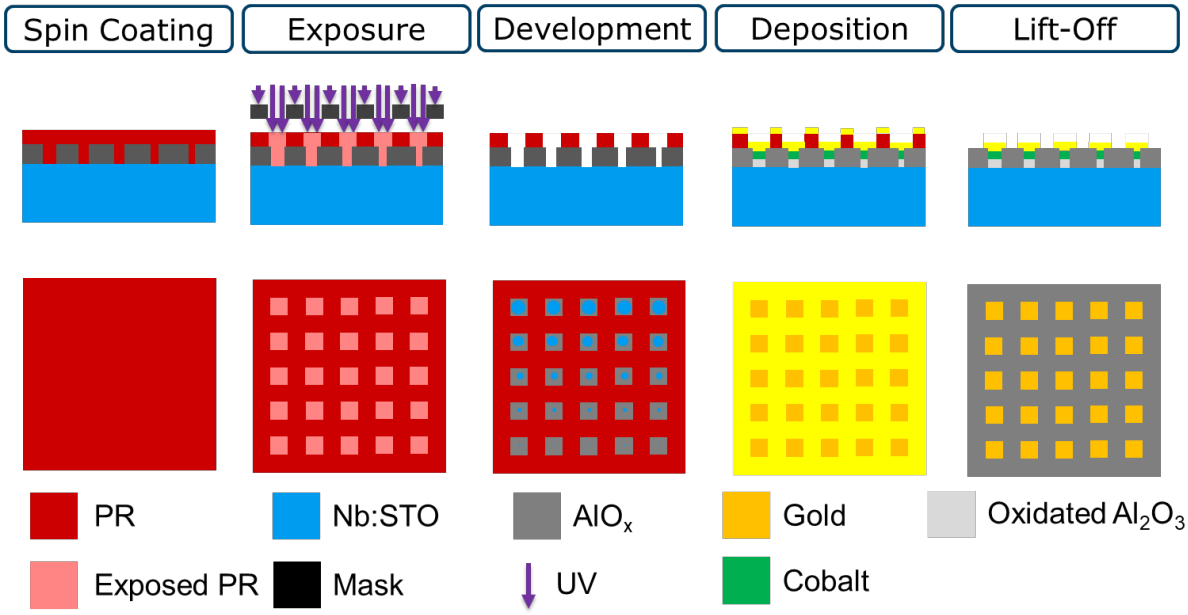


Figure 3.3: Work flow of the fabrication the second lithography and deposition setps, shown in a sectional view (Top) and a top view (Bottom)

After deposition of the isolation layer and patterning of the junctions, the MIS contacts are defined by depositing overlapping the insulating tunnel barrier and the metal. The substrate is spin-coated with photoresist (PR) once more. For this lithography step, a mask featuring square patterns of 400 μm is used, designed to overlap with the previously fabricated openings in the isolation layer. Following development, the PR remains only on the AlO_x regions, while the openings exposing the substrate remain uncovered, allowing direct contact for subsequent deposition.
After the development, the sample is transferred to the electonbeam evaporator. First, a thin layer of AlO_x is deposited, which is 0.7 nm thick. This layer will be the isolator between the metal and semiconductor. After the deposition, the AlO_x is oxidized to ensure a full Al_2O_3 layer, further explained in Section 3.4. For the plasma oxidation, the system is prepared in the following way: The Loading dock is first flushed with oxygen. The oxygen is let into the high vacuum up to 5E0 mbar then pumped down to 2.5E-2 mbar, which is repeated for 2 more times. After flushing the loading dock (LD) if filled with oxygen up to 1E-1 mbar. Due to the low base pressure and repeared flushing we expect this to be pure oxygen. A plasma is ignited by using an oxidation ring and oxygen gas at power 60 W. After 100 seconds the power is turned off and the LD is pumped down again.
After this, a 20 nm thick layer of Cobalt is deposited followed with a 40 nm thick layer of gold, which prevents the Cobalt from oxidizing.

3.6 Final Device

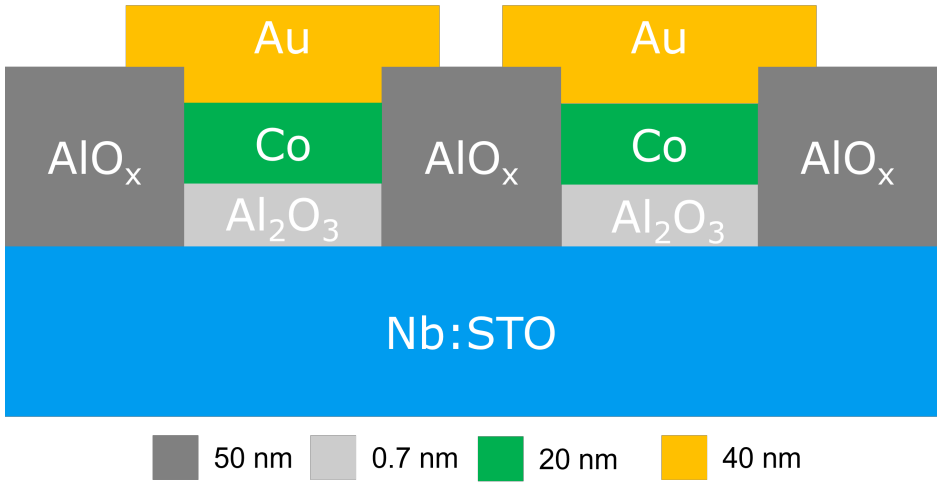


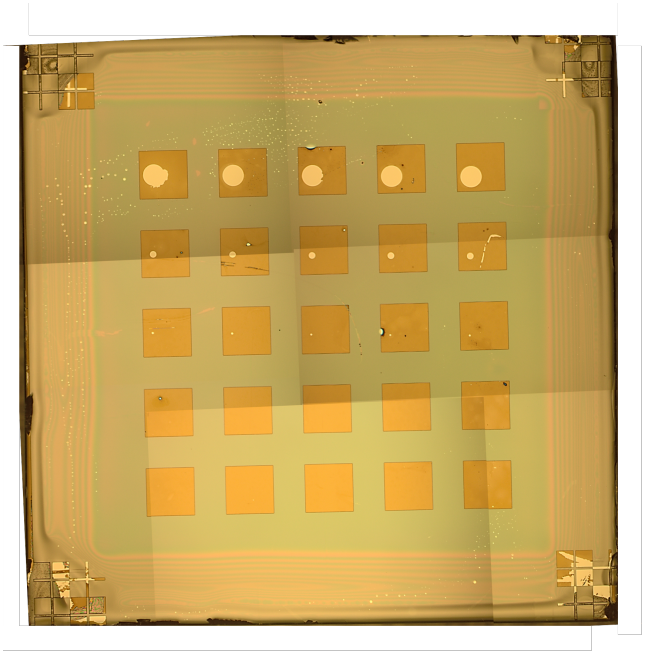
Figure 3.4: Sectional view of the final device structure, zoomed in on 2 devices of similar area (not on scale)

After these steps we have succesfully fabricated 25 MIS junctions with varying areas. Figure 3.4 shows two of the final devices with the same size.
The fabrication proces results in five devices with different areas, all having five devices which allows us to study the device to device variation.

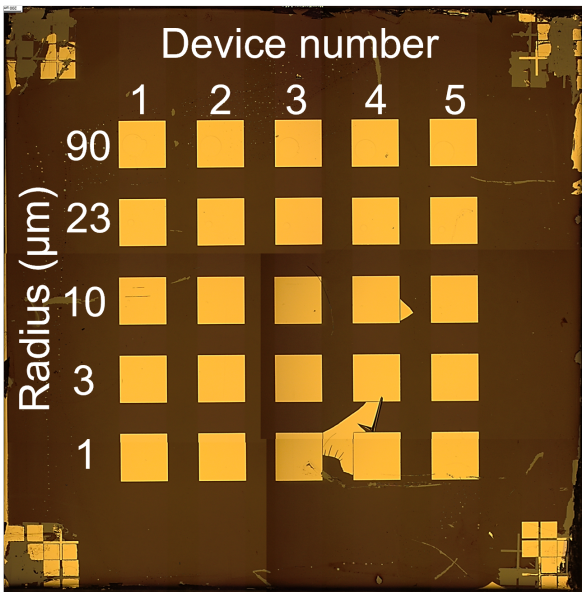
Chapter 4

Results

4.1 Fabrication



(a) Substrate after development of the photoresist (PR) for contact pads. The white areas represent exposed Nb:STO, the brown areas indicate the AlO_x layer, and the green corresponds to the developed PR.



(b) Top view of the final substrate showing five devices per area. Device numbering is used throughout the results section.

Figure 4.1: Results of device fabrication: the substrate before (left) and after (right) the final metal deposition and lift-off.

Prior to metal-insulator deposition, the substrate appeared as shown in Figure 4.1a. In this image, the circular white regions represent the openings to the Nb:STO substrate, surrounded by the brown AlO_x insulating layer. The green corresponds to the patterned photoresist (PR), sitting on the AlO_x. During the

fabrication of the holes in the AlOx, only the 3 biggest junction sizes opened up. The well-defined PR openings and exposed substrate areas indicate successful pattern development for both of the lithography steps shown in Figure 3.2 and 3.3.
The completed device structure is shown in Figure 4.1b. This top-view optical micrograph captures all five device sizes patterned on the same substrate. The brown regions represent the AlO_x insulating layer, which uniformly coats the wafer except where circular junction holes were opened. Square-shaped gold contact pads are visible on top of each junction, forming the metal-insulator-semiconductor (MIS) stack. Each row contains five devices of identical radius, labeled from column 1 to 5, and the radii of the junctions are indicated in micrometers along the row labels (90, 23, 10, 3, and 1 µm), following the mask design.
During fabrication, some issues arose with the smallest devices. As seen in Figure 4.1a, the 3 and 1 um size junctions are not visible, this is likely due to overexposure during the first exposure step. This removes the PR of the smaller area during the development, allowing the AlOx to cover everything. Furthermore, the lift-off process was incomplete in the 1 µm and 3 µm rows in the second litho step, leading to unintended electrical shorts between pads. For example, pads 3 and 4 in the 1 µm row, and pad 4 in the 3 µm row, were not electrically isolated, as seen in Figure 4.1b. These defects are likely due to non-uniform resist coverage during spin-coating or residual resist remaining after development, which impeded proper metal lift-off.
For the remainder of this thesis, device labeling will follow the row-column convention: the row indicates the device radius in micrometers, and the column number identifies the specific device. For example, "90-2" refers to the second 90 µm device. For the remainder of this thesis, we will focus exclusively on the results from the 90 µm and 10 µm devices.

4.2 Electrical Characterization

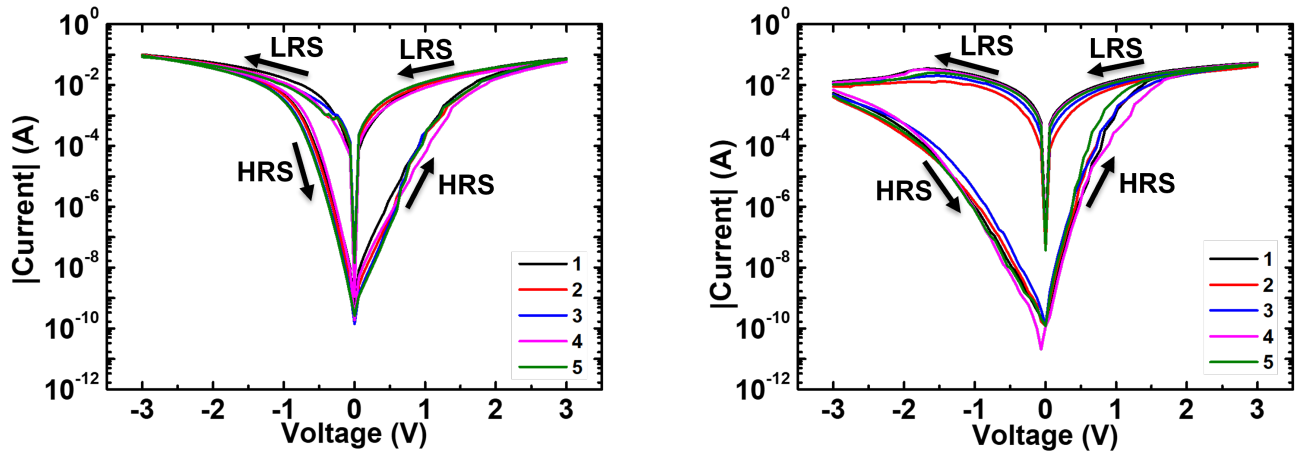
The current-voltage (I–V) characteristics of the $Co/Al_2O_3/Nb:STO$ devices were recorded for two device sizes with radii of 90 µm and 10 µm. The voltage is applied on the top contact and the ground is at the semiconductor. For all measurements a set voltage of 3 V and a reset voltage of -3 V were used, and the current was read. These measurements were done in one continuous sweep without delay time at any point.

4.2.1 Device-to-Device Variation

Figure 4.2 shows the device-to-device variability for both contact sizes. Each subplot contains five nominally identical devices. Both the 90 µm 10 µm devices display high reproducibility, with low variation in current magnitude and switching characteristics.

4.2.2 I–V Characteristics and Hysteresis

Figure 4.4 shows a pronounced hysteresis loop, confirming resistive switching behavior. The I-V sweep begins at $-3\,\mathrm{V}$, where the device is in its high-resistance state (HRS), characterized by low current. As the voltage increases toward $+3\,\mathrm{V}$, the device transitions to a low-resistance state (LRS), evident from a higher current at the same voltage levels, a transition referred to as the set point. When the voltage is



(a) 90 µm devices

(b) 10 µm devices

Figure 4.2: Device-to-device I–V characteristics for 90 and 10 µm contacts. All sizes have 5 devices.

swept back, the device returns to the HRS at the reset point, restoring the original current levels. During the forward sweep, the recovery of the LRS is gradual, again highlighting the characteristic hysteresis loop.

In comparison, the 10 µm devices demonstrate bigger dynamic range, which is defined as the difference between the HRS and LRS. The contrast between the HRS and LRS is well-preserved throughout the full voltage range.

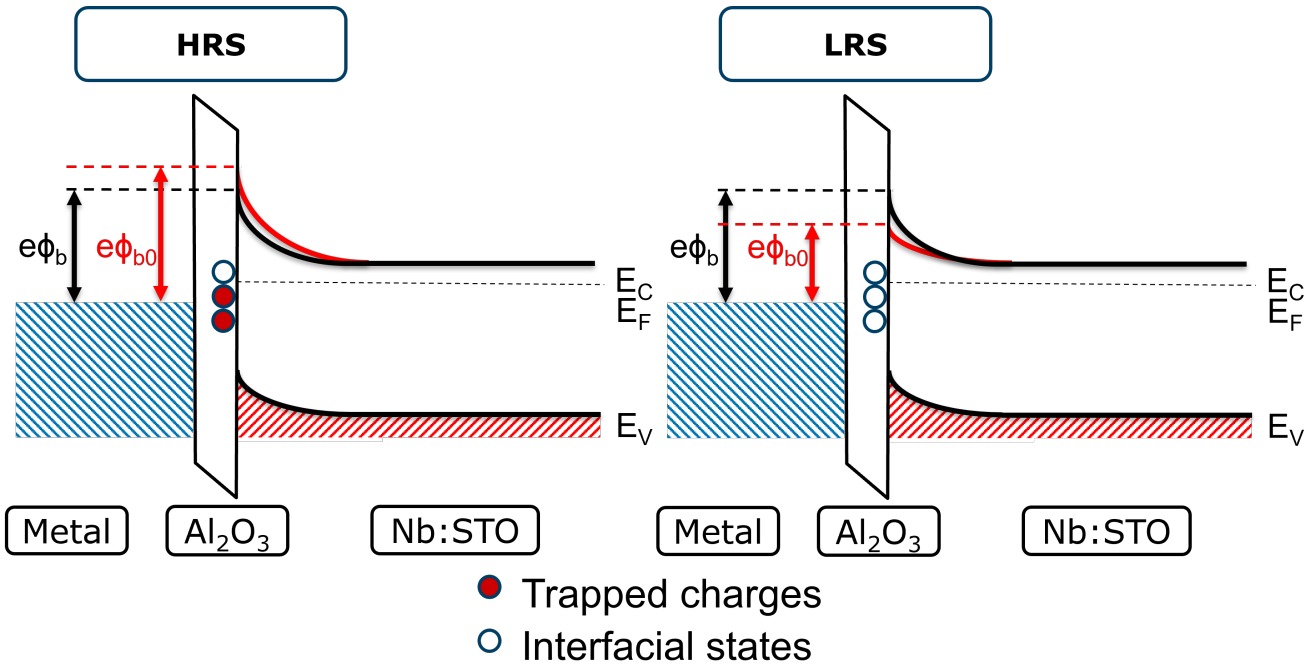
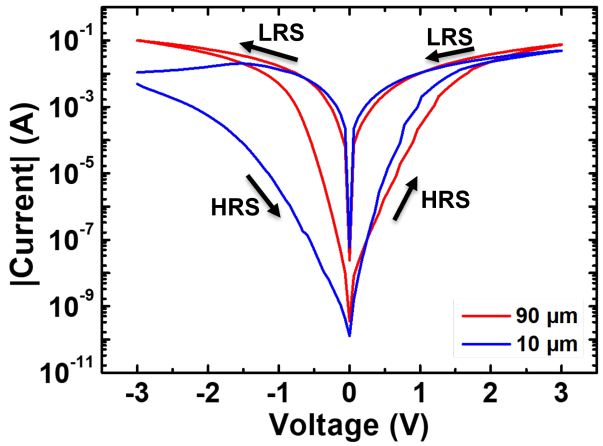
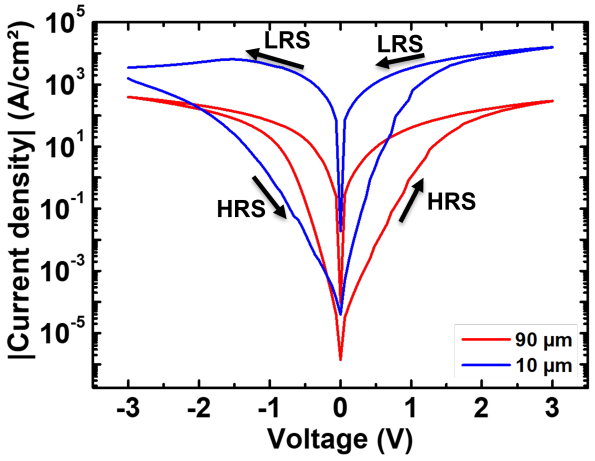


Figure 4.3: Trapped charges in the HRS and LRS state in forward bias

The high-resistance state (HRS) and low-resistance state (LRS) originate from the presence of interfacial trap states located within the Nb:STO and the Al_2O_3 layer. In the HRS, negative charges are trapped in these interfacial states, which increases both the effective barrier height and width at the junction. This elevated barrier suppresses charge transport by reducing the probability of thermionic emission (TE) and tunneling across the interface. As the forward bias increases, the electric field facilitates the release of these trapped charges. Once the set voltage is reached, the traps are sufficiently emptied, and the junction transitions into the LRS. In this state, the reduction in trapped charge decreases the barrier height and narrows the depletion region, which enhances both thermionic emission and tunneling, resulting in a higher current.



(a) Devices of 10 and 90 µm compared in a current-voltage graph



(b) Devices 10 and 90 µm compared in current density-voltage graph.

Figure 4.4: Current (a) and current density (b) as a function of voltage for one of the 90 (red) and 10 (blue) µm devices

To normalize the device response with respect to contact area, the I-V data were converted to current density as shown in Figure 4.4b. An increase in current density is evident as contact radius decreases. The increased dynamic range observed under reverse bias, as well as the elevated current density, can both be attributed to the edge effect.

4.2.3 Effect of Edge Fields

The edge effect results in an enhanced electric field near the device perimeter, leading to a local suppression of the dielectric constant in Nb:STO. This causes a narrowing of the depletion width at the edges, which significantly enhances tunneling probability [24]. In the higher electric field regime, the trapped charge density is higher, causing a bigger dynamic range. This effect is most pronounced under reverse bias, where tunneling is the dominant transport mechanism. Consequently, the reverse current shows a strong dependence on edge-enhanced conduction. In forward bias, thermionic emission remains the dominant process, so the edge effect has less impact on the transport mechanism, aside from an increased current density because of the locally thinner barrier at the edges.

In the presence of an insulating tunnel barrier such as Al_2O_3, the voltage drop is shared between the barrier and the Nb:STO depletion region. Since the tunnel barrier has a much lower dielectric constant and nanometer-scale thickness, it takes up a significant portion of the total voltage drop. This limits the extent to which the depletion width in Nb:STO can narrow under edge field enhancement. As a result, the edge effect has less influence compared to a pure Schottky junction but still contributes to the local barrier thinning in the semiconductor. Therefore, while the Al_2O_3 layer mitigates some of the edge field impact, it does not completely eliminate the enhancement of tunneling at the device perimeter.

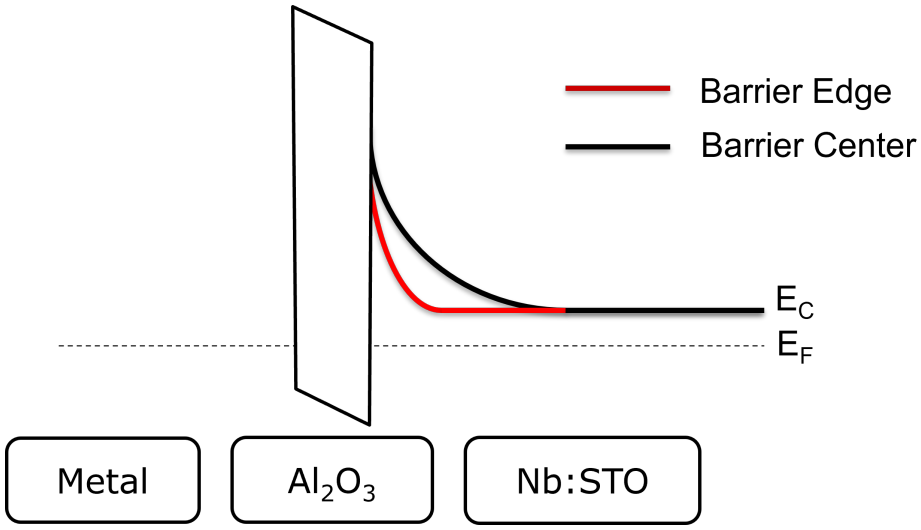


Figure 4.5: Band diagram zoomed in on the barrier at conduction band at the center and edge of the device. [24]

Chapter 5

Discussion and Conclusion

5.1 Discussion

The electrical characterization confirms that the MIS devices fabricated on Nb:STO exhibit resistive switching governed by interfacial effects. Both device sizes, 90 µm and 10 µm, show stable and reproducible switching between high-resistance and low-resistance states, with negligible device-to-device variation, shown in Figure 4.2. However, clear differences in switching characteristics arise when comparing the larger devices to the smaller ones.

The dynamic range (DR), defined as the ratio between the HRS and LRS current, increases significantly as device area decreases. This behavior is consistent with previous findings on Schottky junctions on Nb:STO by Goossens [24], where it was demonstrated that the edge effect plays a dominant role in small-area devices. The edge effect results from the lateral fringing of electric fields, leading to field concentration at the device perimeter. This local enhancement of the electric field causes a reduction in the dielectric constant of Nb:STO near the edge, which in turn reduces the depletion width. A narrower depletion width locally increases the tunneling probability, which is particularly important under reverse bias where tunneling dominates the transport mechanism. As a result, smaller devices exhibit higher current densities and a larger dynamic range in reverse bias.

The impact of the edge effect is most significant in reverse bias, where charge transport is dominated by tunneling. In forward bias, thermionic emission remains the primary transport mechanism, which is less sensitive to the depletion width. Therefore, the edge effect under forward bias mainly manifests as an increase in current density, without significantly altering the switching dynamics. This explains why the DR is less affected in forward bias.

An important consideration is whether the tunnel barrier (TB) formed by the Al_2O_3 layer completely dominates the transport properties, making the edge effect negligible. While the Al_2O_3 barrier indeed takes up a substantial portion of the total voltage drop due to its low dielectric constant and nanometer-scale thickness, the depletion region in Nb:STO still plays a crucial role. The TB and the Nb:STO depletion region act as capacitors in series. This means the electric field drops across both layers proportionally to their capacitance. Because the TB has a lower dielectric constant, it dominates the field drop; however, the Nb:STO depletion region still modulates the overall transport, especially under high-field conditions where permittivity suppression further enhances the edge effect.

The combination of the TB and the Nb:STO depletion region forms a coupled barrier system where both

contribute to the overall transport behavior. The edge effect still leads to localized narrowing of the depletion region underneath the TB, enhancing the tunneling current at the edges. This explains why devices of different areas still show area-dependent current densities despite the presence of the tunnel barrier. Therefore, while the Al_2O_3 layer limits the maximum impact of the edge effect compared to a pure Schottky junction, it does not fully suppress it.
A critical point of consideration is whether the conclusions about DR scaling hold universally or are dependent on the set/reset timing protocol. The current experiments were conducted without delay time at the set and reset points. It is plausible that longer set or reset times could allow for more complete charge trapping or de-trapping, potentially altering the observed resistance states. This means the conclusion on DR enhancement with scaling should be regarded as preliminary. Future work should systematically investigate the impact of set/reset time on resistance states to confirm whether the observed scaling trends are intrinsic to the device physics or influenced by dynamic charging timescales.

5.2 Conclusion

In this project, metal–insulator–semiconductor (MIS) junctions were successfully fabricated on Nb-doped $SrTiO_3$ with a plasma-oxidized Al_2O_3 tunnel barrier and cobalt top contact. The electrical characterization confirms that these devices exhibit stable and reproducible memristive switching behavior governed by interfacial charge dynamics. The resistive switching is attributed to the interplay between the tunnel barrier, the depletion region in Nb:STO, charge trapping at the interface, and localized edge field enhancements.
A key finding of this work is that the dynamic range increases with decreasing device area. This is primarily due to the edge effect, where electric field crowding at the device perimeter leads to a local reduction in the dielectric constant of Nb:STO, narrowing the depletion width and enhancing tunneling probability. This effect is particularly dominant under reverse bias, where tunneling is the main transport mechanism. While the insulating Al_2O_3 tunnel barrier significantly affects the voltage drop distribution, it does not eliminate the impact of the edge effect, which continues to play a significant role in defining the device performance.
For future research, several directions are suggested. First, a systematic investigation into the impact of set/reset times on the resistance states is crucial to determine whether the dynamic range scaling is an intrinsic material property or dependent on measurement conditions. Second, exploring alternative insulating barriers with different dielectric properties may offer further insight into optimizing the balance between tunnel barrier control and edge field effects. Finally, scaling the devices further into the sub-micron regime may reveal whether the edge effect continues to dominate or whether other nanoscale transport phenomena begin to emerge. These insights will be critical for advancing the use of MIS-based memristive devices in neuromorphic computing architectures.

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